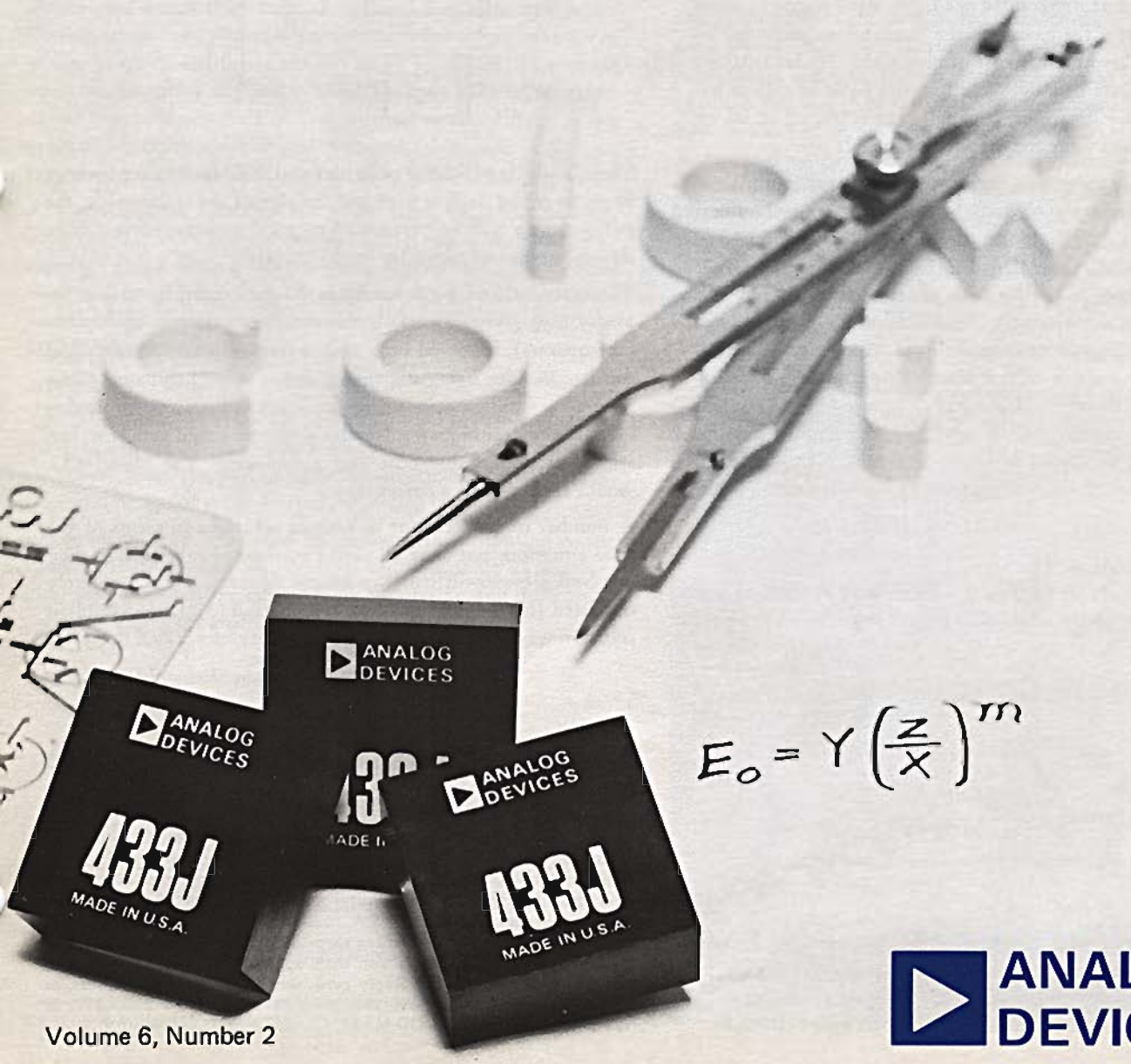
analog dialogue

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete



Volume 6, Number 2

ANALOG DEVICES

Editor's Notes

NEW PRODUCTS

We've never felt the need to apologize for anything that has appeared in *Dialogue*, and we intend to keep matters that way. However, we do think that fans of our "Applications" section deserve an explanation for its truncation in favor of a veritable "raft" of New Products in this issue.

Simply stated, our innovative "boys in the back room" have gone-and-done-it again. There is something about the Spring season (in sway at this writing) that quickens the processes of life: after conception last year (or earlier) and a winter of gestation, the budding and flowering occur with a suddenness and massiveness that is breathtaking. And our creative colleagues, similarly, seem to be graced with this Call of Nature.

And so, we suddenly have an embarrassingly-rich assortment of new products, each of which seems –in its own way– to be the ideal answer to some unheralded need. The significance of some should be obvious, for example, the tremendous potential inherent in the utility and low cost of monolithic 10-bit DAC's*. Many of the others can be "sold" on the basis of salient improvements in specifications, packaging, or price, all of which add up to increased value for the knowledgeable user.

But then there are some that have potentially-great significance that is not immediately obvious because they are unfamiliar: the type 433 $Y(Z/X)^m$ device, the AD2002 2½-digit (0.5%) infra-low-cost DPM, the MDA-11MF fast multiplying DAC; their novelty poses a challenge to the imagination. For this reason, the stories describing them include suggestions for applications that amount to gem-like little "Application Briefs." And that is where much of this issue's "Applications" section is, not in one neat package, but widely dispersed in the context of the products that make the applications possible. Perhaps these ideas, and products, will help *you* now plant the seeds of new uses that may come to fruition by *next* Spring! ▶▶▶

TEASER UNMASKED

In Volume 5, No. 5, we offered this formidable expression and suggested that it had a neat closed-form solution, that could be embodied with a new multi-purpose module, soon to be announced.

$$W = f(U,V) = U + \cfrac{V^2}{2U + \cfrac{V^2}{2U + \cfrac{V^2}{2U + \ldots}}} \qquad (1)$$

The closed-form solution (to dispense with suspense) is

$$W = \sqrt{U^2 + V^2} \qquad (2)$$

and it is achieved with low cost and good accuracy by the Model 433 (described in the adjacent pages) and two op amps. If you solved the problem in the following way, you were inevitably led to the scheme described below:

Recognize that 2U (indicated by the arrow) = U + U, and that consequently

$$W = U + \frac{V^2}{U + W} \qquad (3)$$

This expression is an *implicit* solution for W, containing the key to the use of the 433, which we'll come back to in a moment. The rest of the solution goes:

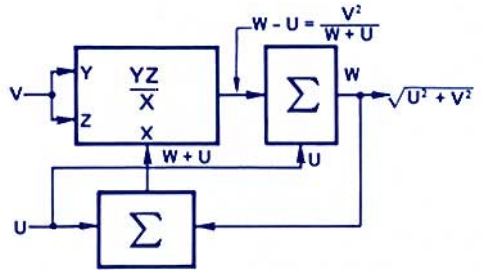
$$(W - U)(W + U) = V^2 \qquad (4)$$

whence

$$W^2 = U^2 + V^2 \qquad (5)$$

and $W = \sqrt{U^2 + V^2}$

Returning to equation (3), it is evident that if you have a device that computes Y·Z/X, and two summing devices (op amps), a configuration that embodies equation (3) can be drawn.



Then, if the input-signal polarities and scale factors are correct, in terms of the devices used and the sign of the square-root, the computation will be performed to good accuracy over a wide dynamic range of either (or both) input(s).

The conventional (and hardly satisfactory) configuration for performing vector summation is simply to use two multipliers (or squarers), followed by a square-root-connected multiplier/divider. Besides being expensive, it has serious dynamic-range problems. Configurations using squarers and rooters employing logarithmic techniques solve the dynamic range problem, but still have undesirable cost and complexity. The Model 433 would appear to be a *better way*.

A number of readers sent us correct solutions in terms of the final equation, but they all used a method of substitution that involved a (more-difficult) quadratic equation that completely obscured the point established by equation (3), i.e., an implicit solution was possible, given the availability of a YZ/X device.

Dan Sheingold ▶▶▶

*Watch for the AD560, to be announced in the next issue of *Dialogue*.

analog dialogue

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VERSATILE NEW MODULE: $Y(Z/X)^m$ AT LOW COST

LOG-ANTILOG TECHNIQUES ARE USED TO MULTIPLY, DIVIDE, EXPONENTIATE
0.5%(FS) ERROR AS A DIVIDER WITH 100:1 RANGE OF DENOMINATOR (NO-TRIM)
0.5%(FS) ERROR AS A SQUARE-ROOTER WITH 10,000:1 INPUT RANGE (NO-TRIM)

by Fred Pouliot and Lew Counts

In Volume 5, Number 5 of *Dialogue*, we predicted the introduction of a new "LAMDE" module. LAMDE is an acronym that implies a set of capabilities: Log, Antilog, Multiplication, Division, Exponentials. However, the new Model 433* has applicability that goes so far beyond even this impressive list, that we decided simply to call it by the unglamorous but apt designation "Programmable Multi-Function Module."

WHAT IT DOES

The equation describing its overall functioning, with appropriate external connections, is (for its 3 inputs, X, Y, Z)

$$E_0 = \frac{10}{9} V_Y \left(\frac{V_Z}{V_X}\right)^m \qquad \begin{array}{l} V_X, V_Y, V_Z, E_0 > 0 \\ 1/5 < m < 5 \end{array}$$

from which one can deduce that it will multiply, divide, raise (or lower) ratios to an arbitrary power. In addition, it can be connected to perform squaring, rooting, and —with a small amount of external circuitry— rms and vector computation. Terminals that are available for manipulation of the exponent m also permit logarithmic outputs to be developed. To provide scale constants for operations involving only pairs of variables, or for operations where a low-drift reference voltage is (in general) desirable, a nominal 9V low-TC reference output is available.

As a multiplier or a divider, maximum error, without trimming, is in the 0.5% (of full-scale output) class, for a wide range of inputs. Typical error is 0.3% of output plus 5mV. (See tabulation on page 5.) Small-signal and large-signal bandwidth tend to be proportional to input voltage, ranging from 50 or 100kHz downward.

WHERE TO USE IT

Typical application areas for the Model 433 are those that involve manipulation of analog voltages in analog data-reduction and computing, pre-processing before digitizing in data acquisition, and design of sophisticated measuring instruments.

Examples include "true-rms" measurements, computing vector sums and differences, and —using the adjustable exponent— ideal gas computations, curve fitting, linearizing, and developing approximations for analog computation.

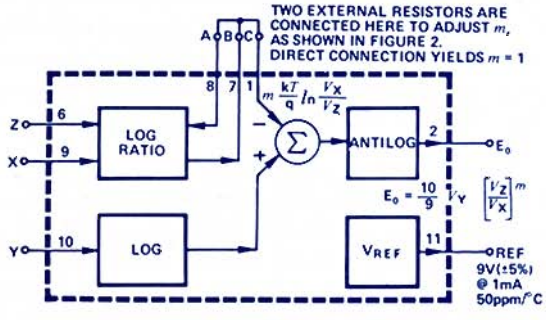


Figure 1. Functional Block Diagram of Model 433

*For complete information on the Model 433, use the reply card. Request G1. Price of Model 433 (1-9) is $75.

Perhaps the most important area of application is a quite prosaic (but hitherto neglected) one: *performing division of analog voltages over wide dynamic ranges.* When conventional analog multipliers are used in feedback configurations for division, errors and noise increase in inverse proportion to the denominator voltage. Even if such a circuit has been arduously trimmed for less than 0.05%(FS) error in one quadrant with 10V denominator, its error will be comparable to the 0.5% guaranteed no-trim maximum error of Model 433 at 1V, and ten times worse at 0.1V. The log/antilog techniques used in Model 433 inherently yield small, nearly-constant errors (without tweaking) that are essentially independent of the denominator level and are well-behaved near zero. This advantage becomes especially significant in such applications as square rooting, when the output is fed back as the denominator input.

continued on page 4

IN THIS ISSUE

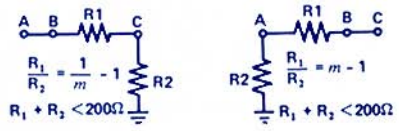
PRINCIPLE OF OPERATION (Figure 1)

Consider first the case where $m = 1$: a log ratio circuit develops a small voltage proportional to the log of the ratio of V_X to V_Z, and makes it available at terminal B. This voltage is connected directly to C and subtracted from another voltage proportional to the log of V_Y. Since $\log (V_Y) - \log (V_X/V_Z) = \log V_Y(V_Z/V_X)$, the subsequent antilog of this difference is proportional to $V_Y(V_Z/V_X)$.

For $m < 1$, a resistive divider having attenuation m is connected between B and C (Figure 2a). The quantity to be antilogged is then $\log(V_Y) - m \log(V_X/V_Z)$, which is equal to $\log V_Y(V_Z/V_X)^m$.

For $m > 1$, a divider with attenuation $1/m$ is connected in the feedback path of the log ratio circuit between B and A (Figure 2b), to provide a gain of m, or $m \log(V_X/V_Z)$ at point B, which is then connected to C, etc.

The antilog circuit has a sensitivity of q/kT, which compensates exactly the kT/q terms associated with the input ratios, giving the circuit first-order independence of temperature. The output scale factor is 10/9. For computing ratios, the built-in 9V(±5%, 50ppm/°C) voltage reference is connected to the Y input, the gain of which is pre-trimmed to impart a 10V scale factor. The reference voltage (@ 1mA) is available for the user's convenience and may be used externally or as a constant at any of the input terminals.



a. $m < 1$ b. $m > 1$

Figure 2. Resistance Connections and Ratios as a Function of m.

BENEFITS OF LOG/ANTILOG TECHNIQUES

Log modules can accept unipolar inputs that vary over wide dynamic ranges, and they have the valuable property that log-mode errors of a given magnitude correspond to a fraction (e.g., %) of the actual input signal regardless of its relationship to full scale. One can infer from this that an accurate divider can be designed, using log techniques, that will hold its accuracy over a wide dynamic range. To illustrate the differences between the conventional approach of implementing division, using a multiplier in a feedback loop, and the 433 approach, error analyses for both techniques are developed and compared.

CONVENTIONAL APPROACH TO DIVISION (Figure 3a)

The multiplier, M, has the transfer equation

$$E_1 = \frac{V_X V_Y}{10} \pm V_{ERROR},$$

where V_{ERROR} represents such cumulative errors as drift, nonlinearity, offset, and noise. Ignoring errors attributed to the amplifier, A1, and summing currents at the inverting input of A1,

$$\frac{V_Z}{R} + \frac{E_1}{R} = 0, \qquad V_Z = -E_1$$

$$-V_Z = \frac{V_X V_Y}{10} \pm V_{ERROR}$$

Solving for V_Y,

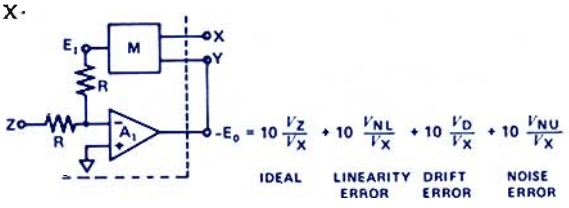
$$E_0 = V_Y = -\frac{10V_Z}{V_X} \pm \frac{10V_{ERROR}}{V_X}$$

Since V_Y is equal to E_0, the expression clearly shows that the magnitude of the error contribution is inversely proportional to the denominator, V_X.

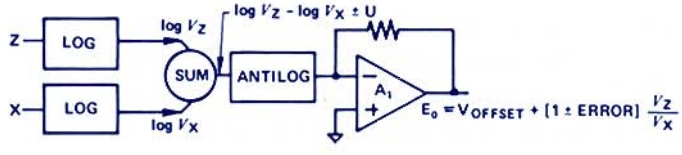
LOGARITHMIC APPROACH TO DIVISION (Figure 3b)

The output of the summing node is $\log V_Z - \log V_X \pm V_{ERROR}$, where V_{ERROR} again comprises those components contributed by the log circuits, the summer, and the antilog module (referred to its input). Since an additive log error corresponds to an incremental multiplicative linear error*, the antilog of the log-mode error can be expressed as $A(V_Z/V_X)$, where $A = \log^{-1}(V_{ERROR}) = (1 \pm \text{ERROR})$. The output amplifier's offset adds an error term, V_{OFFSET}.

Overall error, then, is in the form of a scale-factor error (which can be expressed as a fraction of the signal) and a small dc offset, which is not affected by the denominator V_X.



a. Multiplier in Feedback Loop. Errors are Multiplied by $1/V_X$



b. Simplified Logarithmic Divider. Error is a Constant Plus a Constant Fraction of Output.

Figure 3. Comparison of Division Techniques

For a well-designed unit, such as the 433, this circuit model is valid over a 100:1 range of denominator voltage, and accounts for maximum output error less than 50mV (0.5% of 10V(FS)), and typically 5mV plus 0.3% of the output.

PERFORMANCE COMPARISON—DIVIDERS

Judging from the brief error analysis, one would expect some rather impressive improvements in performance when applying the Model 433 as a divider. And indeed, this is the case. Figure 4 illustrates the dramatic difference in performance between a high-accuracy multiplier-divider, which has been externally trimmed for full-scale error of 0.05%, and a Model 433 with no trimming.

It should be noted that the 433's linearity, offset drift, and noise performance are all virtually independent of the denominator level. For $V_X = 0.1V$, the 433 has 1/10 the error of the 0.05% multiplier-divider. This performance is achieved without external trimming and at less than one-half the typical cost of high-accuracy multiplier-dividers.

*A comprehensive discussion of errors in log circuits can be found in the Model 755 technical bulletin. Use the reply card. Request G2.

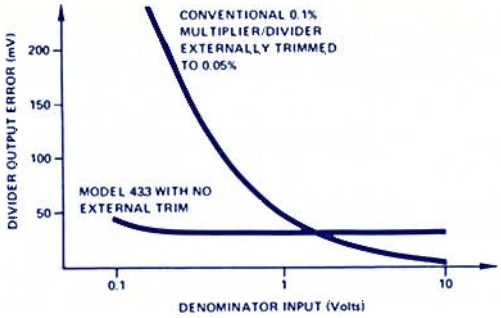


Figure 4. Comparison of Divider Error vs. Denominator Level, Model 433 vs. a Conventional Multiplier/Divider.

SQUARE-ROOT PERFORMANCE

When connected as shown in Figure 5, the Model 433 performs as a divider, with the denominator equal to the output voltage, which must then be necessarily proportional to the square-root of the input.

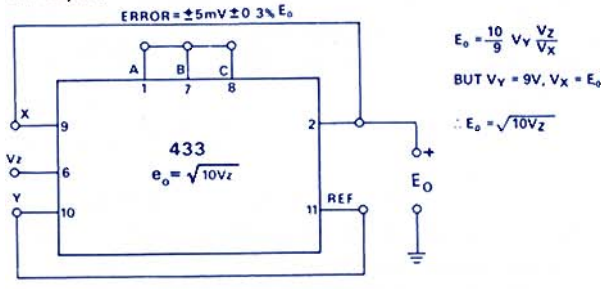


Figure 5. Square Root Circuit Using Divider with Feedback

Everything that has been stated about divider performance is similarly true for the square-root connection, but the dynamic range of input can be increased. The minimum denominator for specified accuracy is 0.1V. For square-root operation, the denominator becomes 0.1V when the input is about 1mV: $(10V:0.1V)^2 = (10V:1mV)$. Below this level, noise and drift errors become significant.

Figure 6 shows the difference in performance between a conventional multiplier/divider connected for square-rooting, and the 433. Since the conventional circuit utilizes feedback, it suffers a degradation of performance as feedback is removed at low levels. In contrast, the 433's error actually decreases as the input decreases, a marked improvement.

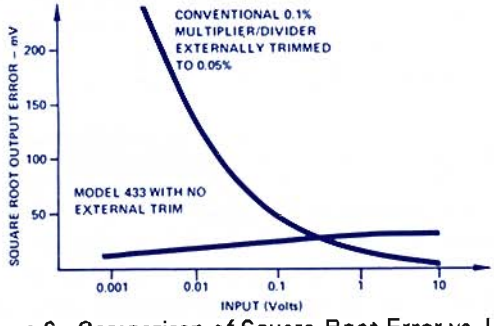


Figure 6. Comparison of Square-Root Error vs. Input Level for Model 433 and a Conventional Mult./Div.

ADJUSTMENTS

Although the initial tolerance of the reference is ±5%, the scale factor (gain) of the 433 is internally trimmed for less than 0.5% overall error when connected for division, i.e., $E_0 = 10(V_Z/V_X) \pm 0.5\%$ max, for m = 1, and $V_Y = V_{REF}$.

continued on page 6

MODEL 433 PERFORMANCE CHARACTERISTICS

(Typical @ +25°C unless otherwise noted)

General Expression	$E_0 = +\frac{10}{9} V_Y \left(\frac{V_Z}{V_X}\right)^m$
Rated Output[1]	+10.5V @ 5mA
Input	
Signal Range	$0 \leq V_X, V_Y, V_Z \leq +10V$,
Max. Safe Input	$V_X, V_Y, V_Z \leq \pm 18V$
Resistance	
X terminal	100kΩ±1%
Y terminal	90kΩ±10%
Z terminal	100kΩ±1%
External Adjustment of the Exponent, m	
Range for m < 1 (Root)	$1/5 \leq m < 1$, $m = \frac{R_2}{R_1 + R_2}$
Range for m > 1 (Power)	$1 < m \leq 5$, $m = \frac{R_1 + R_2}{R_2}$
	$(R_1 + R_2) \leq 200\Omega$
Reference Terminal Voltage[1]	
V_{ref} (Internal Source)	+9.0V ±5% @ 1mA
vs Temp (0°C to +70°C)	±0.005%/°C
Power Supply Range	
Specified	±(14.7 to 15.3)VDC @ 10mA
Operating	±(12 to 18)VDC
Temperature Range	
Specified	0°C to +70°C
Storage	-55°C to +85°C
Package Outline	FA-7
Case Dimensions	1⅛" x 1⅛" x 0.62"
Price (1-9)	$75.
(10-24)	$69.

MULTIPLIER/DIVIDER PERFORMANCE CHARACTERISTICS:

	DIVIDE	MULTIPLY
Transfer Function	$E_0 = +10(V_Z/V_X)$	$E_0 = \frac{+V_Y V_Z}{10}$
Accuracy[2,3], Total Output Error @ +25°C (for specified input range)		
Typical (RTO)	±5mV±0.3% of output	*
Max. Error (RTO)	±50mV	*
Input Range ($V_Z \leq V_X$)	0.01V to 10V, V_Z	0.01V to 10V, V_Z
	0.1V to 10V, V_X	0.01V to 10V, V_Y
vs Temp.	±1mV/°C	*
Output Offset Voltage (Not Adjustable)		
Initial @ +25°C max	±10mV	*
Offset vs Temp.	±1mV/°C	*
Noise, 10Hz to 1kHz		
V_X = +10V	100μV rms	*
V_X = +0.1V	300μV rms	*
Bandwidth, Small Signal (-3dB)[4],		
$V_Y = V_Z = V_X$ = 10V	100kHz	*
$V_Y = V_Z = V_X$ = 1V	50kHz	*
$V_Y = V_Z = V_X$ = 0.1V	5kHz	*
$V_Y = V_Z = V_X$ = 0.01V	400Hz	*
Full Output (V_Y or V_Z = 5VDC ±5VAC)	(V_X) x (5kHz)	*

*Same as for divide mode.

[1] Terminals short circuit protected to ground only.

[2] Multiplier scale factor must be trimmed at Y terminal using a 25kΩ trim pot.

[3] Total errors defined as the difference between the measured output and the theoretical output voltage for any given pair of specified input voltages.

[4] Small-signal measurements are conducted with $V_X = V_Y = V_Z = V$ at a fixed DC level, and v_Y or v_Z a superimposed sine wave of amplitude 10%V.

All active components hermetically sealed.

Specifications subject to change without notice.

continued from page 5

For other interconnections or for different scale factors in the divide mode, the user can adjust the scale factor by inserting a 25kΩ variable resistance in series with the Y input, or by using an adjustable external reference at the Y terminal. No offset adjustments are required.

LOWER NOISE USING LOG TECHNIQUES

Figure 7 is a plot of output noise as a function of signal level in a 10Hz–1kHz bandwidth with V_Y constant and $V_X = V_Z$. It should be noted that, with V_X at 0.1V, the effective gain for V_Z is 100. Curves are plotted for $m = 1$ and for the two specified extremes. Noise values may be interpolated for intermediate values of the exponent.

Again, the value of the 433 as a divider, compared to other approaches, is manifested. In changing by only 3:1, over a 100:1 range of input, the noise level is essentially independent of signal level; compare this with the 100:1 change over the same range experienced with circuits using multipliers with feedback for division.

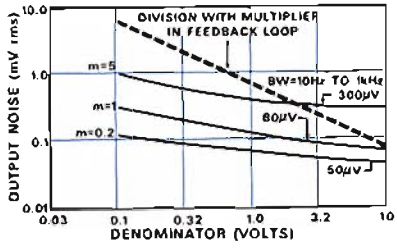


Figure 7. Model 433 Noise vs. Denominator for Various Values of the Exponent, m (Log Scales).

EXPONENTS

Figure 8 shows the variety of curve shapes provided by the continuous range of exponents from $m = 1/5$ to $m = 5$, for possible use in function fitting and curve linearizing.

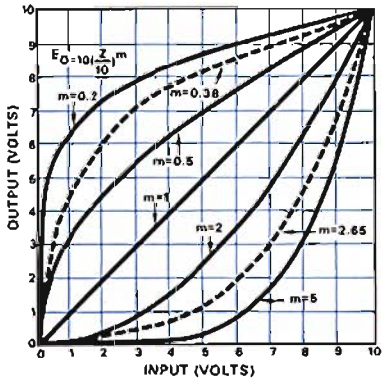


Figure 8. Varying the Exponent, m.

LOG OF VOLTAGE RATIO

If an output is taken from terminal B, with the device connected for $m > 1$, it will be equal to $0.06\ m \log_{10}(V_X/V_Z)$ at 27°C, i.e., 0.06 m volts per decade. Since the temperature compensation provided by the antilog is not used, the coefficient will be sensitive to temperature in the ratio T/300°K. Though the circuit will work with higher values of m, the maximum recommended value is 5, which corresponds to a sensitivity of 0.3V/decade. The maximum output swing at B is about ±1V.

TRUE-RMS COMPUTATION (Figure 9)

If a simple unit-lag averaging filter is connected between the 433's output and the square-root feedback point, the output of the filter is constrained to be the square-root of the average squared input, or the rms. The averaging time constant is adjusted by the choice of R and C. For long time constants, a low-cost FET-input amplifier, such as the AD540*, may be desirable. Unlike specially-calibrated linear averaging devices, that produce the true rms only for sine waves, this low-cost approach produces true rms of any stationary waveform, be it noise, pulses, sine waves, or square waves. Error (relative to full-scale) is virtually independent of a non-saturating signal's "crest factor" (peak to rms). If bipolar signals are to be applied, the absolute value should be taken first.

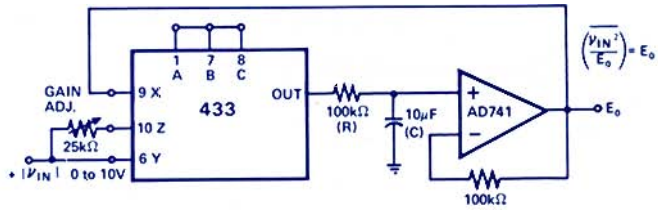


Figure 9. "True" RMS Circuit: $E_O = \sqrt{V_{IN}^2}$

VECTOR SUMMATION

This technique is described in the "Teaser Unmasked" on page 2, an implicit solution of an identity that gives the square-root of the sum of the squares as a result. Though the identity used in Figure 10 is slightly different, the results are the same. In order to avoid saturation, the maximum tolerable value of $(V_W + V_U)$, in any combination, is 10V (e.g., $V_U = 0$, $V_V = 10V$, $V_W = 10V$; or $V_U = 4.1V$, $V_V = 4.1V$, $V_W = 5.8V$). This circuit is capable of high accuracies, typically 0.1% of reading. For this reason, matched resistance pairs having low TCR should be used. ▶▶▶

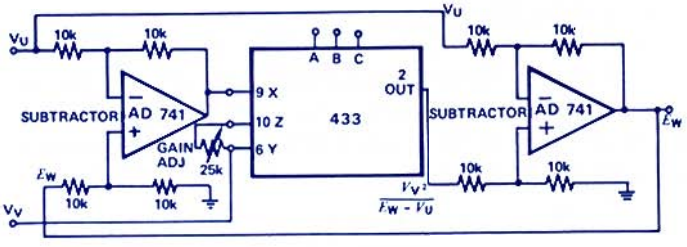


Figure 10. Vector Sum $E_W = \sqrt{V_U^2 + V_V^2} = \frac{V_V^2}{E_W - V_U} - V_U$

THE AUTHORS

Fred Pouliot, a graduate of Northeastern U. (TBΠ and HKN), and a key member of ADI's analog-module marketing staff, has had solid experience as designer and engineering manager, with specific nonlinear-device accomplishments.

Lewis Counts, Manager of Analog Product Engineering, has an S.B. from M.I.T. and a broad spectrum of successful analog and digital circuit-design experience, ranging from picosecond TDR systems to chopper-stabilized op amps.

*For information on the AD540, use the reply card. Request G3.

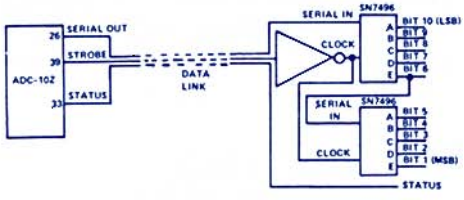
TWO LOW-COST HIGH-LINEARITY A/D CONVERTERS

10-BIT ADC-10Z IS MONOTONIC (NO MISSED CODES) FROM 0°-70°C
LOW-COST CONVERTER HAS 20μs CONVERSION TIME

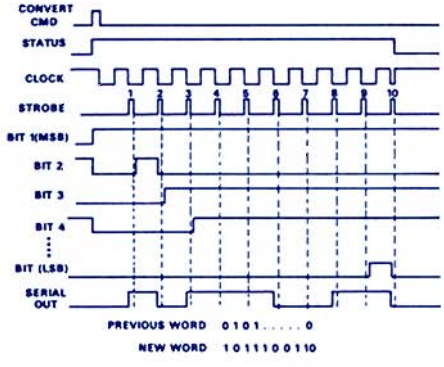
The ADC-10Z* sets a new standard of value for low-cost 10-bit successive-approximation A/D converters. Encapsulated in a compact 2" x 4" module, it offers a conversion time of 20μs (50kHz rate), a gain-temperature coefficient of ±40ppm/°C, and guaranteed monotonicity (i.e., *no missing codes*) over its full operating temperature range.

In addition to these basic characteristics, it includes some features and a degree of versatility that have until now have available only in more expensive units. For example, the user can select any of 4 programmed input ranges (0 to +5 or +10V, ±5 or ±10V) by choice of external connections and jumpers; he can also choose an arbitrary range by using an external scaling resistance of appropriate value.

Since an important application for low-cost 10-bit general-purpose ADC's is in early conversion in noisy environments



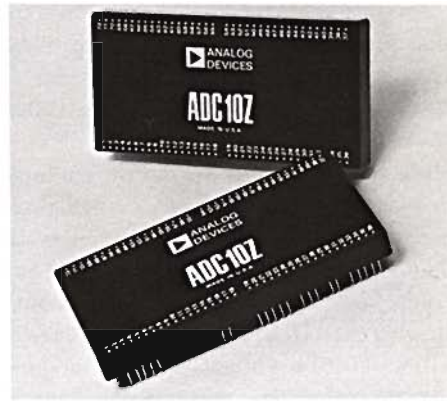
Serial Data Transmission



ADC-10Z Timing Diagram

where analog signals would be degraded in transmission, the ADC-10Z features a *good, workable* serial data output. A latched serial output with non-return-to zero (NRZ) format is available at the output of a TTL flip-flop. A strobe output is available to clock the serial data into a receiving shift register. A status output changes level only when the conversion is *really* complete. A timing diagram and typical serial data transmission configuration are shown.

The parallel data outputs are positive-true binary for unipolar inputs and either 2's complement or offset binary for bipolar inputs. The standard unit is specified for the 0 to +70°C range. Units are also available with input buffer follower, and/or for



operation over extended temperature ranges (-55° to +125°C). Price of the standard unit is $67 in 100's, $99 for 1-9. ▶▶▶

*For complete data on the ADC-10Z, use the reply card. Request G4.

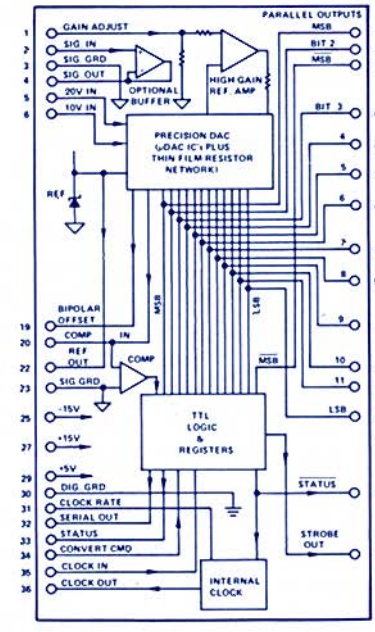
12-BIT A/D IS A "BEST BUY"!
HAS EASY-TO-USE SERIAL OUTPUT

The ADC-12QZ* is a 12-bit successive-approximation general-purpose A/D converter that offers moderate speed and good all-around performance at very low cost, less than $100 in 100's.

The excellent value created by this combination of low cost and solid performance (10ppm differential-linearity TC, better-than 25kHz conversion rate, 30ppm gain TC) is achieved by a combination of factors that is probably unique to Analog Devices:

- Our own proprietary monolithic quad switches are used for excellent linearity and low cost (for both parts and testing).
- Years of production of many thousands of DAC's and ADC's have resulted in the techniques and know-how to manufacture 12-bit devices that retain many of the extra features of the more-expensive units at very low cost in large quantity.

The extra features include choice of four input ranges by jumpering: ±10V, ±5V, 0 to +5 or +10V. All logic is *fully* TTL/DTL compatible. Both 2's-complement and offset-binary coding are available for bipolar-input devices. And the same clean logic design that is used for the ADC-10Z results



Block Diagram of the ADC-12QZ

in a *workable* serial output from a latched TTL flip-flop, with accompanying strobe for clocking data into a receiving shift register. Price is $92 in 100's, $129, (1-9). ▶▶▶

*To receive complete information on the ADC-12QZ, use the reply card. Request G5.

3 SAMPLE-HOLDS: ECONOMY, SPEED, PRECISION

SHA-2A SETTLES TO 0.01% IN < 500ns

The SHA-2A*, a very fast sample-hold module, has both speed and accuracy appropriate for applications with 12-bit A/D converters characterized by total conversion times of the order of microseconds. It is ideal for use with such converters as the ADC-10F, which performs 10-bit conversion in 1μs.

Since such converters are most-often used to acquire data from rapidly-changing signal sources, the dynamic parameters of the SHA-2A were designed to provide excellent performance in such applications. Slewing rate is 100V/μs; settling time to within 0.01% is <500ns. The aperture uncertainty of 0.25ns means that an input signal slewing at 200mV/μs will be acquired to well-within 1LSB uncertainty for 12-bit conversion.

Maximum droop rate of 100μV/μs means that the input to a fast converter, such as the ADC-10F, will change considerably less than 0.1LSB during conversion. Since the droop rate is typically much less than this maximum figure, the SHA-2A is entirely suitable for use with most 12-bit high-speed converters.

Important applications of the SHA-2A (besides "ordinary" high-speed data-acquisition circuits) are in data acquisition for signal analysis and for simultaneous sample-hold systems. The former relies on the low aperture jitter for uniformity of sampling, the latter for minimal time skew between "simultaneously" acquired samples.

One additional feature of the SHA-2A that tends to increase its flexibility and versatility (if not performance) is the availability of its open-loop input terminals. The user can connect it in the usual way, as a unity-gain follower, as a follower-with gain, as an inverting amplifier, or even differentially. The specifications are for operation as a unity gain follower, and are of course degraded with increased closed-loop gain, or the use of externally-connected circuit elements.

Price of the SHA-2A is $225 (1-9). ▶▶▶

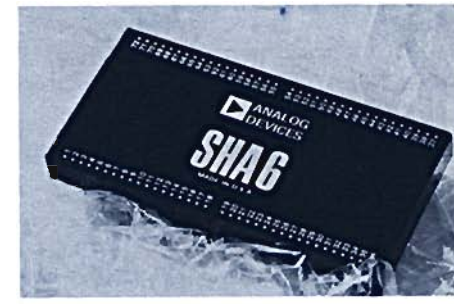
*For further information on the SHA-2A, use the reply card. Request G6.

SHA-6 ENHANCES 16-BIT CONVERSION IDEAL MATCH FOR ADC-16Q'S PRECISION

The SHA-6* is a sample-hold module designed as a companion to the high-resolution ADC-16Q† converter, introduced earlier in these pages (Vol. 6, No. 1). The sample-hold is designed to acquire an input signal to 16-bit accuracy, and to hold that signal stable during the time required by the ADC-16Q to convert it. For the ADC-16Q to realize its full accuracy for signals varying at rates in excess of about 375mV/s, a precise sample-hold, such as the SHA-6, is essential.§

Systems that require 16-bit conversion impose severe burdens upon the designer. Not only must a sample-hold be used to limit the slewing rate of the input to the ADC; it must also have adequate accuracy and stability for 16-bit applications; and it must be capable of rejecting common-mode voltages as small as 150μV (1LSB for the ADC-16Q). The SHA-6 was specifically designed to meet these needs, and at present, it is the only known commercially-available sample-hold that does.

The key to success is careful design and layout, and the use of an instrumentation amplifier-type buffer at the input. AD504L‡ low-drift IC op amps, and high-



stability resistor networks with excellent tracking TCR's, are used. The result is stability within 2ppm/month and per °C. The SHA-6 settles to within 7.5ppm in 5ms (at unity gain) and recovers from 10x overvoltage within 150μs. As seems appropriate for devices designed for use in high-accuracy applications, input bias current is only 80nA maximum, and input impedance is $10^9\Omega$ and 5pF. Aperture time is -1.7μs with 10ns jitter due to switching (because of delay in the buffer, the switching to *hold* occurs 1.7μs "early"). The most salient applications of the SHA-6 and ADC-16Q will be found in the measurement of voltages that require precise (to 16 bits) characterization at a specific instant of time. Price of SHA-6 (1-9) is $375. ▶▶▶

GENERAL-PURPOSE SHA-5 HAS 12-BIT PERFORMANCE AT LOW COST

The SHA-5☆ is a very low-cost sample-hold module designed for general-purpose use in data acquisition, data distribution, sampling synchro-to-digital conversion, and in other applications where sample-hold is necessary or desirable. Desirability is increased by its low cost, $39 (1-9, less in quantity).

Although the SHA-5 was designed with the primary design goal of low cost, the amplifier technology is so advanced that even a low-cost product has surprisingly good performance (compared with what might have been available even 1 or 2 years ago). Gain error is less than 0.01%, settling time to 0.01% (of 20V input step) is well below 15μs, and aperture jitter is about 4ns, allowing a 12.5V/ms signal to be stopped with less than 1LSB uncertainty in 12-bit conversion.

Droop rate in *hold* is 5mV/s (or 5μV/ms), making the SHA-5 suitable for either the short holds normally required in data acquisition or the somewhat longer holds needed for data distribution and simultaneous sample-hold systems. ▶▶▶

*For information on Model SHA-6, use the reply card. Request G7.

†For information on Model ADC-16Q, request G8.

§For further information on the need for sample-holds to speed the acquisition of varying signals, see the *A-D Conversion Handbook*, pp. 1-17-23 and II-160-162. (See p. 15, this issue.)

‡For information on AD504L op amps, request G9.

☆For information on the SHA-5, request G10.

A DPM THAT REALLY CHALLENGES ANALOG METERS !

2½ DIGIT AD2002 SNAPS INTO PLACE ; AVAILABLE FROM STOCK. $50 IN 100'S

The AD2002* digital panel meter may well pose the first important threat to the "high-accuracy" analog panel meter because of its small size, readability, and speed, as well as its low cost and data-acquisition-system compatibility.†

The second member of the Analog Devices DPM family to be made available, it has a number of advanced features, including availability of filter surface for silk-screened user graphics (such as company logos, application designations, physical units, etc.); a rugged new 1.8"H x 3"W x 1.5"D aluminum case that allows tool-free insertion and removal; and definitive out-of-range indication: two dashes replace the data digits.

WHAT IS THE AD2002?

It is a 2½-digit panel meter that operates from a 5V supply. It is designed specifically as a replacement for 0.5–1.0% analog meters in equipment and systems. Besides a maximum error rating of 0.5% ±1 digit, with temperature coefficient of 1/20 digit per °C, other characteristics include simultaneous test for all filament segments and optional data-processing interface capability. The unit provides stable readings of unipolar signals over a full-scale range of 0 to 1.99V, with automatic overload indication. The reading can be held indefinitely upon command (optional).

BRIGHT, SHARP DISPLAY

With a green filter (other colors optional) for the RCA Numitron display, the AD2002 is well-matched to the optical response of the human eye. The perceived result is a bright, sharp, highly-readable, non-fatiguing display, over a wide range of ambient light. The unambiguous digital display has the advantage (over analog meters) that the operator needs only the ability to read numbers.

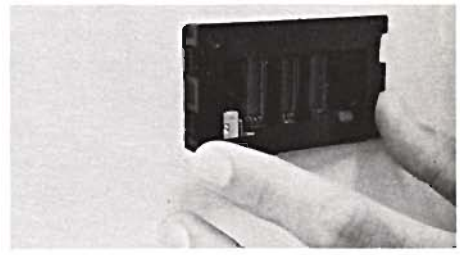
COUNTER-COMPARATOR CONVERTER

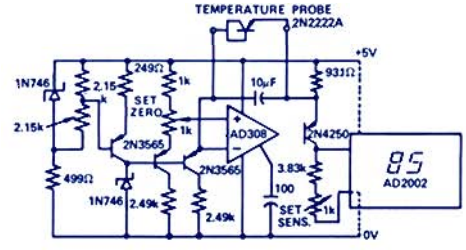
The figure shows a block diagram of the AD2002 circuit. The leading edge of the trigger pulse (external or internal) resets the counter and complements the *status* (i.e., "in process") line. The trailing edge starts the counter (100kHz, 200 counts maximum). The counter output is converted to voltage and compared with the input. When it exceeds the input, the comparator switches, stopping the count and changing the *status* polarity.

The counter output is decoded to illuminate the appropriate digit segments. Nothing further happens until a new trigger pulse arrives, normally after 250ms. Since the typical conversion time is 2ms, the appropriate segments are illuminated 99% of the time, resulting in a flickerless display. Optionally, a rate of up to 200Hz is available for data acquisition.

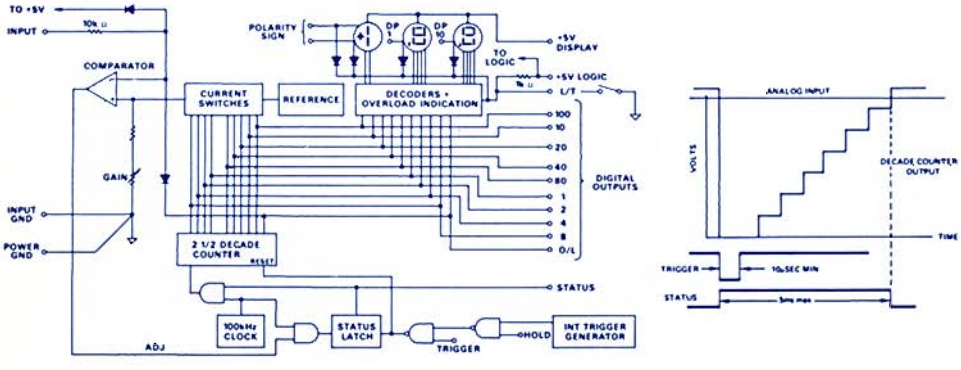
APPLICATIONS

The AD2002 is especially useful in meter applications, where clear, sharp, unambiguous readout is desired, where conversion as well as readout is necessary, where readings indicating a given state must be "frozen," or where rapid full-scale changes must be read accurately without "bounce" or interpretation. It is especially useful in measuring changes in physical variables, such as power, temperature, or pressure.





The circuit shows a scheme for measuring temperature, typically calibrated in °C, using the 5V meter supply. A constant current of about 1mA flows through a diode-connected transistor probe, which develops a voltage change of about -2.2mV/°C. The voltage is amplified and scaled to (for example) 10mV/°C. If the output is set to zero at 0°C, the meter will read °C directly, from 0°C to beyond +125°C. ▶▶



Block Diagram and Conversion Timing

*For complete information on Model AD2002, use the reply card. Request G11.

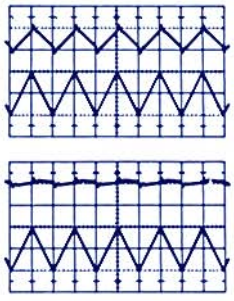
†Optional. For display-only applications, the user also avoids the cost of a mating connector.

FAST MULTIPLYING DAC FOR DISPLAYS

MDA-11MF HAS < ½LSB FEEDTHROUGH FOR 10V/μs INPUT

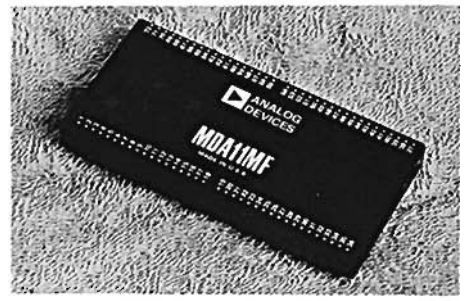
Model MDA-11MF* is a multiplying digital-to-analog converter designed for high-speed applications, such as graphic-display generation; digital coefficient-setting for automatic testing, adaptive control, or signal processing; and manipulation of trigonometric quantities. Its response is extremely fast. For example, output-current settling time in response to a full-scale analog step (0 to -10V) is 0.8μs to 0.05% and 1.0μs to 0.01%. With a full-scale analog voltage applied (-10V), settling time in response to a full-scale digital code change is 0.4μs to 0.05% and 1.0μs to 0.01%. With 0V at the analog input, settling time for a full-scale digital step disturbance is 0.2μs to less than 5mV and 0.5μs to 1mV (with Model 48).

Analog frequency response is excellent: 2MHz full-power bandwidth and 5MHz small-signal -3dB bandwidth. More important, *feedthrough* of analog signal at zero digital gain (all "0"'s) is truly negligible: -80dB for sinewaves to beyond 100kHz, and ½LSB for triangular waves with 10V/μs slope. This is shown graphically in the Figure.



In both photographs, the lower trace is a 500kHz, 10V/μs triangular wave that is driving the analog input. The upper photograph shows the magnified response with a digital input of 1LSB (least-significant bit, 1/2048). This establishes the calibration of the lower photograph, which shows the response with zero digital input, clearly demonstrating that the feedthrough under these conditions is less than ½LSB.

In addition to its speed the 11-bit resolution (1:2048), with commensurate linearity, allows precise handling of both analog and digital signals. A fixed dc reference is also available for applications in which the analog input is either constant or requires a stable (passively) added constant.



The analog input range is 0 to -10V, and the output is a current, ranging from 0 to +4mA:

$$i = -4N_D\frac{v_{IN}}{10}\ \text{mA}$$

where i is the generated current and N_D is the fractional digital number.

Though best performance is obtained in single-quadrant multiplication, the MDA-11MF can be used for two-quadrant multiplication, with offset binary input, and an output range of ±2mA, by the use of jumpers. (All necessary components are contained within the unit.)

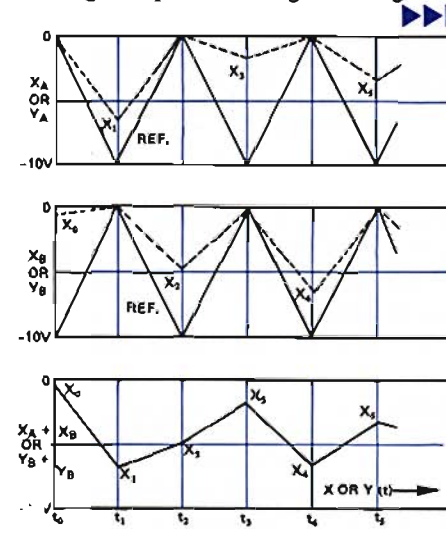
The output current (600Ω unipolar source resistance) may be used directly, or to develop up to 1V across a load resistor; however, the most usual application is to drive the inverting input of a fast operational amplifier such as the Model 48 (see page 11, this issue).

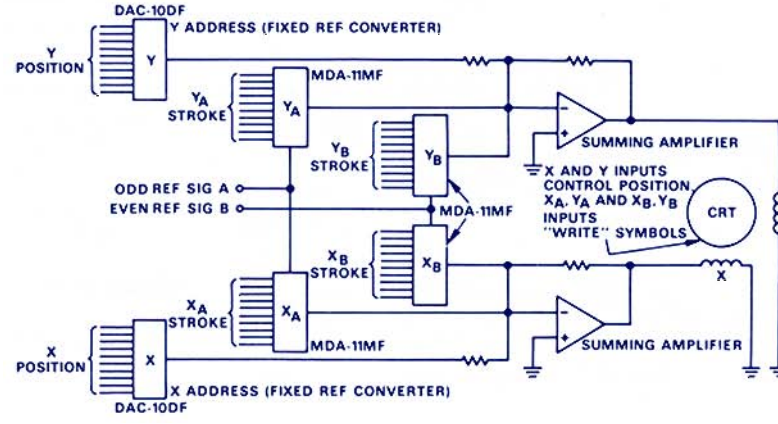
DISPLAY APPLICATION

The Figure shows 2 pairs of MDA-11MF's generating computer graphics using straight-line segments. The excellent resolution allows them to provide full-scale deflections. However, they may also be used with positioning DAC's, as shown, for character generation.

For each axis, two out-of-phase constant-amplitude triangular waves are digitally-modulated alternately, in proportion to the next end value. The sum of the increasing and decreasing waves provides linear interpolation between adjacent values. Since gains are switched at zero amplitude, disturbance is minimal. The figure shows the time history of several X-values. Y is varied similarly, and the resulting X-Y plot has straight-line segments.

▶▶▶





Application of MDA-MF's in Highly-Flexible Display.

*For further information on the MDA-11MF, use the reply card. Request G18. Price is $150 (1-9).

TWO NEW AMPLIFIERS

LOW-DRIFT INSTRUMENTATION AMPLIFIER HAS ±0.5μV/°C DRIFT, >94dB CMR

Model 605* is a new instrumentation amplifier that combines excellent performance and low cost, while retaining the advantages of single-resistor gain adjustment, for gains from 1 to 1000. Its overall error for a 20° temperature range is typically less than 0.03%, with 0.5μV/°C drift and better than 0.01% nonlinearity. It has an unusually low cost, $59 (605J) to $80 (605L).

The low drift and nonlinearity, plus the high 94dB of common-mode rejection (G = 1000), make the Model 605 especially useful for precision processing of low-level signals in noisy environments or reduced-interference reception of low-level signals from remote locations. The low total error (0.03% typical, 0.1% maximum) over a ±10°C range is useful in a wide range of transducer, bridge, or pre-amplifier applications in medical, industrial, and aerospace data-acquisition applications.

In addition to its single-resistor gain programming, the Model 605 also has terminals available to permit remote sensing and arbitrary output reference. Remote sensing is used to obtain precise output from a booster follower, arbitrary reference can be used for output biasing or zero suppression, and both terminals may be used for current drive of floating or grounded loads.

Other features include 300kHz gain-bandwidth, ±100nA (1nA/°C) bias current, $10^9\Omega$ input resistance, and 0.5μV noise (peak-to-peak, referred to the input, 10Hz bandwidth).

MODEL 605 FEATURES

- **Low Drift: ±0.5μV/°C(605L) to 3μV/°C(J)**
- **Adjustable gain (single resistor): 1 to 1000**
- **Low nonlinearity: ±0.01% (G = 100)**
- **High CMR: >94dB (±10V, G = 1000)**
- **Small Size: 1½" square x 0.4"H**
- **Low Cost: $59(605J) to $80(L), 1-9**

*For complete information on Model 605, use the reply card. Request G16.

COMPARISON WITH OTHER INSTRUMENTATION AMPLIFIERS

	Precision Low-Drift	Precision Wideband	Economy FET
Model	605K	604K	603K
Characteristics			
Offset Drift[1] (RTI, μV/°C)			
G = 1	±150	±1000	±500
G = 1000	±1	±1	±15
Nonlinearity, max (%FS, G = 100)	±0.01	±0.01[2]	±0.2
CMR, min (G = 100, dB, 1kΩ unbal.)	94	100	80
Bandwidth, -3dB (kHz, G = 100)	3	50[2]	10
Settling time (0.1%) μs, G = 1	130	15[3]	40
Price (1-9)	$65	$170	$45

[1] See page 14 for drift computation at other gains
[2] Independent of gain, 1 to 1000.
[3] 25μs settling to 0.01%, G = 10.

OP AMP SETTLES TO 0.01% IN 300ns

MODEL 48 IS IDEAL FOR DISPLAY APPLICATIONS

Model 48's* small settling time (300ns typical, 500ns *max* to 0.01%), fast slew rate (125V/μs), and low cost, plus excellent common-mode rejection (80dB @ ±10V) make it an ideal general-purpose high-speed operational amplifier for use as a unity-gain buffer, fast current source, or high-speed integrator. In data acquisition, it can be used in sample-hold and multiplexer circuits. And in data-distribution and displays it is an ideal partner for high-speed current-output DAC's to obtain voltage output.

In particular, it is an excellent mate for the MDA-11MF fast multiplying DAC described on page 10. A circuit board is even available to house this compatible couple in applications calling for high-speed voltage output.

Its fast settling is also *smooth* and stable due to 6dB/octave rolloff at frequencies exceeding 15MHz. It can drive up to 750pF of capacitance without oscillating.

The table compares it with other members of Analog's family of fast FET-input op amps. Model 48, in a 1 1/8" square x 0.4"H package, tends to run especially "cool" because of its low(9mA) quiescent supply drain. (A typical supply to power it is the Model 904: ±15V at ±50mA.)

*For complete information on Model 48, request G17.

KEY SPECS COMPARED

Specs \ Model	48J	46J	44J	45J
Settling time, max (to 0.01%, ns)	500	300[1]	1000	1000
Slew rate (V/μs, min)	110	1000	75	75
Bandwidth (MHz, small signal)	15	40	10	10
Output current, min (mA max at 10V)	20	100	20	20
Drift (μV/°C, max)	50	75	50	50
CMR (dB min @ ±10V)	80	72	80	74[2]
Gain (open loop, min)	100k	25k	100k	50k
Price (1-9)	$49	$75	$42	$37

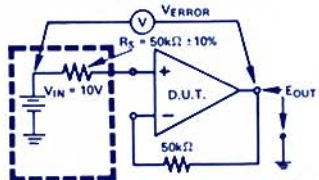
[1] 100ns settling to 0.1% for Model 46
[2] Rated at +5, -10V for Model 45

NOT BY DRIFT ALONE . . .

by Stan Harris

Voltage offset drift is commonly considered to be the most important factor limiting op amp accuracy at low frequencies, with drifts due to current bias and offset closely vying for second place. Recognizing (and perhaps overreacting to) the importance of low drift specifications, IC op amp manufacturers (and purveyors) have offered such popular devices as the SSS725E, the LM208A (and the BB3500E), which feature either low offset or bias current or low voltage drift. Analog Devices has recently (*Dialogue*, Vol. 6, No. 1) introduced the ultra-stable monolithic AD508K*, which not only has a 0.5μV/°C offset drift and super-β input transistors, but also includes minimum gain of 10^6 and CMR of 110dB, to minimize *total error*, rather than simply win a drift-specification contest.

It has not been well-recognized that once drift (of both kinds) is greatly reduced (to the order of 1μV/°C), there are other sources of error that can no longer be neglected, particularly for high-accuracy non-inverting applications, and especially if ambient temperature varies over a reasonable range. These include finite-gain and common-mode errors.



BASIC CIRCUIT. DOES NOT SHOW POWER SUPPLY, COMPENSATION, OR ZEROING CONNECTIONS.

A particularly nasty transducer application that illuminates the problems of optimization is shown in the Figure: a unity-gain follower is driven by a 10V source with 50kΩ (±10%) internal resistance. The objective is to reproduce the source voltage and its variations at low impedance with the best possible accuracy, but at the low cost of a monolithic op amp, and with a minimum of external circuitry and "tweaking." The circuit in the Figure shows a model of such a source, in which the amplifier output can be directly compared with the open-circuit voltage.

To determine the major sources of error in the circuit and arrive at a basis for estimating worst-case error, an error budget is tabulated, based on specified (or estimated) worst-case amplifier parameters, for each of the amplifier types mentioned above, and for a representative low-cost amplifier, the AD741K.† Performance is considered over two ranges of temperature, +24°C to +45°C and 0 to +70°C. The amplifiers are nulled using their zero-adjust terminals (where provided), and are allowed a ±5% power-supply variation.

The results of this exercise tend to speak for themselves. The AD508 comes off quite well because of its balanced design; there is no single substantial source of error. The LM208AH is handicapped by lack of an offset adjustment terminal, but even so, gain, common-mode, and voltage drift errors make the overall sum at least twice that of the AD508. SSS725E is "done in" by its high bias and offset currents, as is the BB3500E, which is also beset by substantial gain, common-mode, and power-supply-sensitivity errors. The AD741K, despite its low price, is surprisingly not the worst performer, and should be considered seriously as a "best buy" for applications of this type in the 0.03% performance class.

FET-input IC's,§ while not listed here, should be mentioned, because their current errors are negligible, and they might seem an intuitive choice. Low drift-voltage types are costly, however, and high gain, CMR, and PSR, if available at all, would be quite expensive. The reader may wish, as an exercise, to compare performance of the AD508 with his favorite IC FET in the AD508's price class. ▶▶▶

I.C. OP AMP ERROR BUDGET ANALYSIS

Error Parameter (min or max)	T_A = +25°C to +45°C					T_A = 0°C to +70°C					
	AD508KH	LM208AH	SSS725EJ	BB3500E	AD741KH	AD508K	LM208A	SSS725E	BB3500E	AD741K	
GAIN	(10⁶) 10μV	(80k) 125μV	(10⁶) 10μV	(100k) 100μV	(50k) 200μV	(500k) 20μV	(Est 60k) 167μV	(800k) 12.5μV	(Est 70k) 143μV	(25k) 400μV	SPEC ERROR
I_b x ΔR (5kΩ)	(10nA) 50μV	(2nA) 10μV	(80nA) 400μV	(50nA) 250μV	(75nA) 375μV	(15nA) 75μV	(Est 2.5nA) 12.5μV	(100nA) 500μV	(Est 75nA) 375μV	(120nA) 600μV	SPEC ERROR
I_{OS} x R (50kΩ)	(1nA) 50μV	(0.2nA) 10μV	(5nA) 250μV	(30nA) 1500μV	(10nA) 500μV	(1.6nA) 80μV	(Est 0.3nA) 15μV	(7nA) 350μV	(Est 45nA) 2250μV	(15nA) 750μV	SPEC ERROR
V_{OS}	(trim to 0) 0	(500μV) 500μV	(trim to 0) 0	(trim to 0) 0	(trim to 0) 0	(trim to 0) 0	(Est 730μV) 730μV	(trim to 0) 0	(trim to 0) 0	(trim to 0) 0	SPEC ERROR
$\Delta V_{OS}/\Delta T$ (see note)	(0.5μV/°C) 10μV	(5.0μV/°C) 100μV	(0.6μV/°C) 12μV	(1.0μV/°C) 20μV	(15μV/°C) 300μV	(0.5μV/°C) 35μV	(5.0μV/°C) 350μV	(0.6μV/°C) 42μV	(1.0μV/°C) 70μV	(15μV/°C) 1050μV	SPEC ERROR
CMR	(110dB) 32μV	(96dB) 160μV	(120dB) 10μV	(Est 96dB) 160μV	(90dB) 320μV	(100dB) 100μV	(96dB) 160μV	(115dB) 18μV	(Est 90dB) 320μV	(90dB) 320μV	SPEC ERROR
PSRR	(10μV/V) 30μV	(16μV/V) 48μV	(5μV/V) 15μV	(Est 50μV/V) 150μV	(15μV/V) 45μV	(15μV/V) 45μV	(16μV/V) 48μV	(7μV/V) 21μV	(Est 60μV/V) 180μV	(15μV/V) 45μV	SPEC ERROR
NOISE	Difficult to estimate because of specification non-uniformity. Range approximately from 2μV to 10μV, not a significant % of the total.										
TOTAL	182μV	953μV	697μV	2180μV	1740μV	355μV	1482μV	944μV	3338μV	3165μV	
PRICE (100 pcs)	$20.00	$14.95	$16.30	$20.00	$2.25	$20.00	$14.95	$16.30	$20.00	$2.25	

NOTE: $\Delta V_{OS}/\Delta T$ for the AD508K and SSS725E are specified with V_{OS} nulled. Nulling the BB3500E and AD741K may degrade $\Delta V_{OS}/\Delta T$ beyond the maximum spec.

*For complete information on the AD508, use the reply card. Request G12.

†For data on the AD741K, request G13.

§For information on FET-input IC's from Analog Devices, request G14.

10-BIT BINARY TO 3-DIGIT BCD CONVERSION USING THE ADC-10Z AS A 3-DIGIT BCD CONVERTER

by Jim Fishbeck

Three-digit BCD* analog-to-digital conversion (1000 codes) at moderate-to-high speeds is usually performed by a 12-bit binary successive-approximations converter with rescaled interquad coefficients, somewhat less-rigorous testing, and wanton wastage of 3096 perfectly-good (possibly) codes.

It can also be performed by a 10-bit binary A/D converter (1024 codes) and binary-to-BCD decoding. Such decoding used to be rather arduous, involving counters and great expenditure of time. However, with the advent of such low-cost devices as the SN74185A 5-bit binary-to-BCD converter, the decoding by the A/D-converter user becomes quite practical, with often-negligible time delay. There are several good reasons for using 10-bit converters:

1. If the data is to be processed, but BCD is desired for visual monitoring from time to time (via numeric readouts in one or more locations), binary A/D conversion, followed by binary/BCD, will provide both the binary input needed by the processor and the BCD for the readout. If the data is acquired and converted to binary at some distance from the readout and processor, only 10 data lines are needed, instead of 12.

2. 10-bit conversion is, in general, less costly than 12-bit conversion, since less board area and fewer connectors, flip-flops, switches, and resistors are used. (However, it is only fair to note that the requirements on 12-bit conversion for BCD coding are not stringent, since the resolution is only 1:1000 instead of 1:4096; also, the cost of additional logic for binary/BCD conversion is low, but not negligible.)

3. If speed is important, a successive-approximations converter will probably be used. It will require less time to convert 10 bits than is needed for 12 bits.

4. If data is transmitted serially, two fewer bits are required for each 10-bit binary word than for the corresponding BCD word.

5. The 1024 binary codes are a close (but conservative) match to the 1000 codes inherent in 3 BCD digits.

THE SCHEME

Figure 1 shows the connections for economical analog to BCD conversion, via 10-bit binary, using five SN74185A binary/BCD converters. The logic converter functions as a read-only memory, directly decoding each 10-bit binary number into its 3 BCD equivalent. There are no counting schemes involved, which means that the logic converter's speed is limited only by the propagation delay through 4 IC's, about 100ns in the worst case. When the ADC-10Z† is appropriately calibrated, a BCD display connected to the BCD outputs will read directly in volts for an analog input range of 0 to +10V.

IMPLEMENTATION

When using the ADC-10Z as a BCD-output converter, the 10-volt input range (pin 5) is used. However, since nominal full-scale is calibrated for 1024 codes, the gain must be modified slightly by connecting a 75kΩ resistor between pins 15 and 23 (direct input and ground). The unit is externally jumpered for *unipolar* operation (pin 16 to pin 19). Operation in this connection does not adversely affect scale factor or coding for ADC-10Z's supplied with the optional input buffer follower.

Zeroing and scale-factor (gain) adjustment are performed in the same way as for binary, except that the input test voltage for zero adjustment is 5.00mV (transition from 00...00 to 00...01), and the gain is adjusted for the BCD transition from 9.98 to 9.99 (1001 1001 1000 to 1001 1001 1001) at 9.985V.

OVERVOLTAGE

If the analog input is 10.00 volts or more, the most-significant digit will have an "illegal" BCD code of 1010 (800 + 200). As shown in Figure 1, a simple *and* gate will detect this state and furnish a "1" to indicate out-of-scale operation.

OUTPUT LOADING AND TIMING

Maximum output load is 7 TTL unit-loads for each bit, except for the LSB (pin 52 of the ADC-10Z), which is limited to 4 unit-loads. Because successive-approximations is used, and the LSB (the last bit to be converted) is not involved in the binary/BCD conversion, all the delay through the digital conversion occurs before the ADC-10Z finishes the A/D conversion. Hence, the BCD output is valid on the "1" to "0" "end-conversion" transition of the ADC-10Z's status output, allowing clocking of data on that edge, if desired.

The scheme described here can be extended to develop "3 ¾-digit" BCD from 12-bit binary, using 4000 of the 4096 available codes. In the reverse direction, SN74184 BCD-to-binary devices may be used, e.g., to permit 3 ¾ BCD-to-analog conversion with a 12-bit binary D/A converter. ▶▶▶

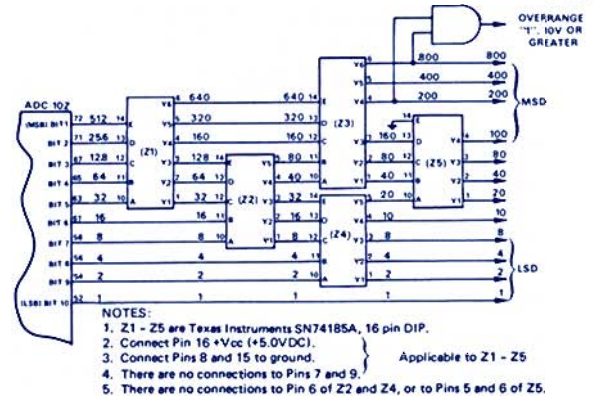


Figure 1. 10 Bit Binary-to-BCD Converter.

THE AUTHOR

Jim Fishbeck is Converter Product Marketing Specialist at Analog Devices. Armed with degrees in both E.E. and Marketing from Michigan State University, he has designed flight control equipment for jet aircraft at Collins Radio Company, and marketed electromechanical control components at Texas Instruments.

*Binary-coded decimal (e.g., 396 → 0011 1001 0110)

†See page 7, this issue.

RTI vs. RTO
HOW TO COMPUTE THE DRIFT OF INSTRUMENTATION AMPLIFIERS

THE PROBLEM

An instrumentation amplifier's offset drift is typically specified at two values of gain, for example, 150μV/°C at unity gain and 0.5μV/°C at gain of 1000, referred to the input. How does a user determine the drift at a gain of 100? What is the difference between "referred to the input" and referred to the output?

THE BACKGROUND

Operational-amplifier offsets and drifts are always "referred to the input" (RTI), as though they were produced by voltage sources in series with one of the input terminals, and would have to be balanced, in feedback circuits, by output self-adjustment. The predicted magnitudes of offset and drift at the output are computed by multiplying the RTI specifications by the closed-loop gain of the feedback circuit. On the other hand, offset or drift of a given device is deduced from a measurement of the output offset or drift at a known value of closed-loop gain (with impedances low enough for current effects to be negligible).

The reason offset and drift in op amps are always specified as RTI is that, while the amplifiers' high open-loop gain allows them to be used in a wide variety of connections yielding a wide range of closed-loop gains, the feedback circuit also maintains the input voltage at the RTI value, allowing the output drift (RTO) to be readily calculated as a function of gain.

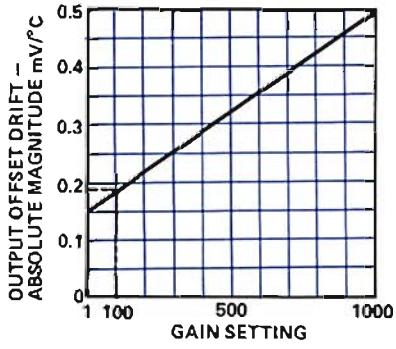


Figure 1. Output Offset Drift vs. Gain for Model 605L.

Fixed-gain instrumentation amplifier users don't care whether the specification is RTI or RTO, since the one can be computed from the other by simply multiplying or dividing by the gain.

With *adjustable-gain instrumentation amplifiers*, it might be thought useful to consider offset and drift in the same way it is done for op amps, i.e., RTI, then to simply multiply by the gain.

But... there is a catch. Many types of instrumentation amplifiers have more than one significant source of offset, with differing influence for each at different values of gain. Usually, there is a term that is constant, added to one that is proportional to gain. For this reason, manufacturers of these devices usually specify the offset (or drift) at a minimum of two values of gain. However, there is little agreement among manufacturers as to whether to specify the drift referred to the input or at the output, and there has been precious little analysis published as to how to predict the maximum drift at *intermediate* values of gain, depending on whether the spec is RTI or RTO.

THE SOLUTION

The simplest favor a vendor could do his customers would be to provide a specification in the form of a plot of maximum output drift as a function of gain (Figure 1). Next best, or in addition, would be an equation specifying the drift as a function of gain. Finally, if you have neither plot nor equation, you can develop both quite easily from the available specs, if the drift vs. gain can be considered a linear function.

Plot

The plot of output drift vs. gain in Figure 1, based on the given example, is a straight line between the end points established at gains of 1 and 1000. At unity gain, RTO and RTI drift are the same. At gain of 1000, use either the RTO specification or the RTI spec multiplied by the gain (1000). Hence, the end points in the example are 0.15mV/°C at unity gain and 0.5mV/°C (i.e., 1000 x 0.5μV/°C) at gain of 1000. The straight line is the locus of the magnitude of offset drift vs. gain. Thus, at a gain setting of 100, the maximum drift would be about 0.18mV/°C at the output, or 1.8μV/°C, referred to the input.

Equation

An equation of the form $y = mx + b$, where m is the slope and b is the intercept, can be easily derived. The slope is the drift change divided by the gain change (0.5 – 0.15)/(1000 - 1)mV/°C, or about 0.35μV/°C, and the intercept is, to a very good approximation, 0.15mV/°C. Thus, at gain 100, the output drift is (100 x 0.35μV/°C) + 150μV/°C, or 185μV/°C (or 1.85μV/°C, referred to the input).

The approximate equation for output drift is

$$\text{Drift}\Big|_{G}^{\text{RTO}} = \left[\text{Drift}\Big|_{1000}^{\text{RTO}} - \text{Drift}\Big|_{1}\right] \cdot \frac{G}{1000} + \text{Drift}\Big|_{1}$$

To refer drift to the input, either divide the above equation by the gain, or use the approximation

$$\text{Drift}\Big|_{G}^{\text{RTI}} = \text{Drift}\Big|_{1000}^{\text{RTI}} + \text{Drift}\Big|_{1} \cdot \left[\frac{1}{G} - 0.001\right]$$

▶▶▶

3 RECENT BOOKS ON OP AMPS AND CONVERTERS

MODERN OPERATIONAL CIRCUIT DESIGN

by John I. Smith, published by Wiley-Interscience, 1971

This unusual book, which contains a number of novel circuit applications, is a good philosophical introduction to operational amplifiers. Its author, who is obviously in love with his subject, writes fluently, if a little self-consciously. It is profusely illustrated (258 illustrations in its 256 pages) and printed in a highly readable type face on paper having a slightly-tinted semi-matte finish.

Introduced on the jacket as a "cohesive collection of essays about the application of the modern operational amplifier," it (in the Preface) "addresses the practicing technologist who is not conversant with electronics". Further, "some electrical knowledge is presupposed, but it is thought to be of the axiomatic kind that is difficult to avoid in an electrified culture ... half-serious thought was given to the subtitle 'Ohm's law with applications'".

Within, the author begins with inverting circuits, both static and dynamic, goes to followers (non-inverting circuits), symmetric (differential) circuits, and precise diode (basic nonlinear) circuits. He then takes up bridge and meter circuits (both voltage and current), devotes two chapters to static and dynamic errors, and then, in the remaining half of the book, discusses circuits for use in instrumentation, computation, switching, and operational systems. The book ends with a (too-short) chapter: "Recommended laboratory practice".

The book is a highly-personal one; in fact, the jacket states that *"all circuits illustrated in this book have been successfully built and tested by the author"*. Its style is reminiscent of the efforts of writers for the old "Lightning Empiricist" in its heyday (when the author and ourself were colleagues).

If it has weaknesses, there are at least two: an excessive fascination with the lever analogy ($-V_1G_1 = V_2G_2$), and an insufficiency of guidance for the serious designer in the areas of specifications and selection criteria. But, on the other hand, the book succeeds in its quest "to be practical by providing the most practical of all commodities – insight."

D.H.S. ▶▶▶

OPERATIONAL AMPLIFIERS

Design and Applications

by Gene Tobey, Jerald Graeme, and Lawrence Huelsman, Ph.D., published by McGraw-Hill Book Company, 1971

This book is a welcome addition to any library on op amp circuits. Its strong suit is the 200-or-so pages devoted (for the first time) to the internal design of op amps. With op amps available for pennies, engineers are unlikely to design their own; nevertheless, an understanding of design is important to getting the best performance out of an op amp consistently in real applications.

There are about 245 pages on applications. 45 of these are devoted to an in-depth treatment of active filters. The rest of the applications, depicted in some 159 numbered illustrations, include linear, nonlinear, switching (A/D, D/A, sample-hold) waveform-generation, and modulation circuits, many of which are familiar. Though largely limited to "how it works," discussion of the applications includes occasional design tips.

The philosophical and the practical (op amp circuit theory and some notes on definition and measurement of performance characteristics) are presented briefly in a small appendix.

Any criticisms of the book must necessarily be considered minor, in the light of its importance. Nevertheless, the circuit designer may find himself craving more "flesh-and-blood" information in the Applications section, including some guidance (perhaps in tabular form) as to the classification of and selection among the most common op amp families to meet the needs of specific applications. It was difficult to find some relevant topics via the index, which might impair its accessibility as a reference (there's more to be found than meets the eye). It should prove near-ideal as an academic textbook. *D.H.S.* ▶

PUBLICATION NOTICE:

A D CONVERSION HANDBOOK

Analog Devices, Inc., has just published the *Analog-Digital Conversion Handbook*, written by our engineering staff and edited by Dan Sheingold. It has 400 pages, more than 250 illustrations, and 17 tables, bibliography, and index. Its price, postpaid, is $3.95 in the United States and Canada. *To obtain a copy*, send your check or money order to Analog Devices, Inc., P.O. Box 796 (*important!*), Norwood, Mass. 02062.

Since reviewing one's own book might be considered inappropriate, we list here a brief nonpartisan Table of Contents:

▶▶▶

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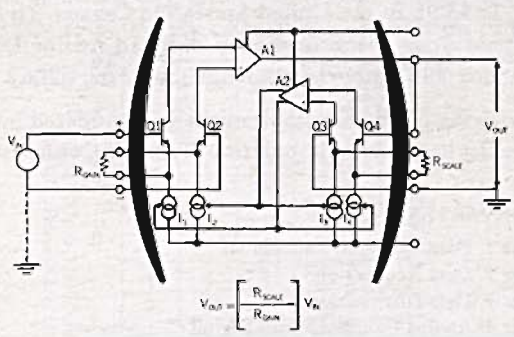

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