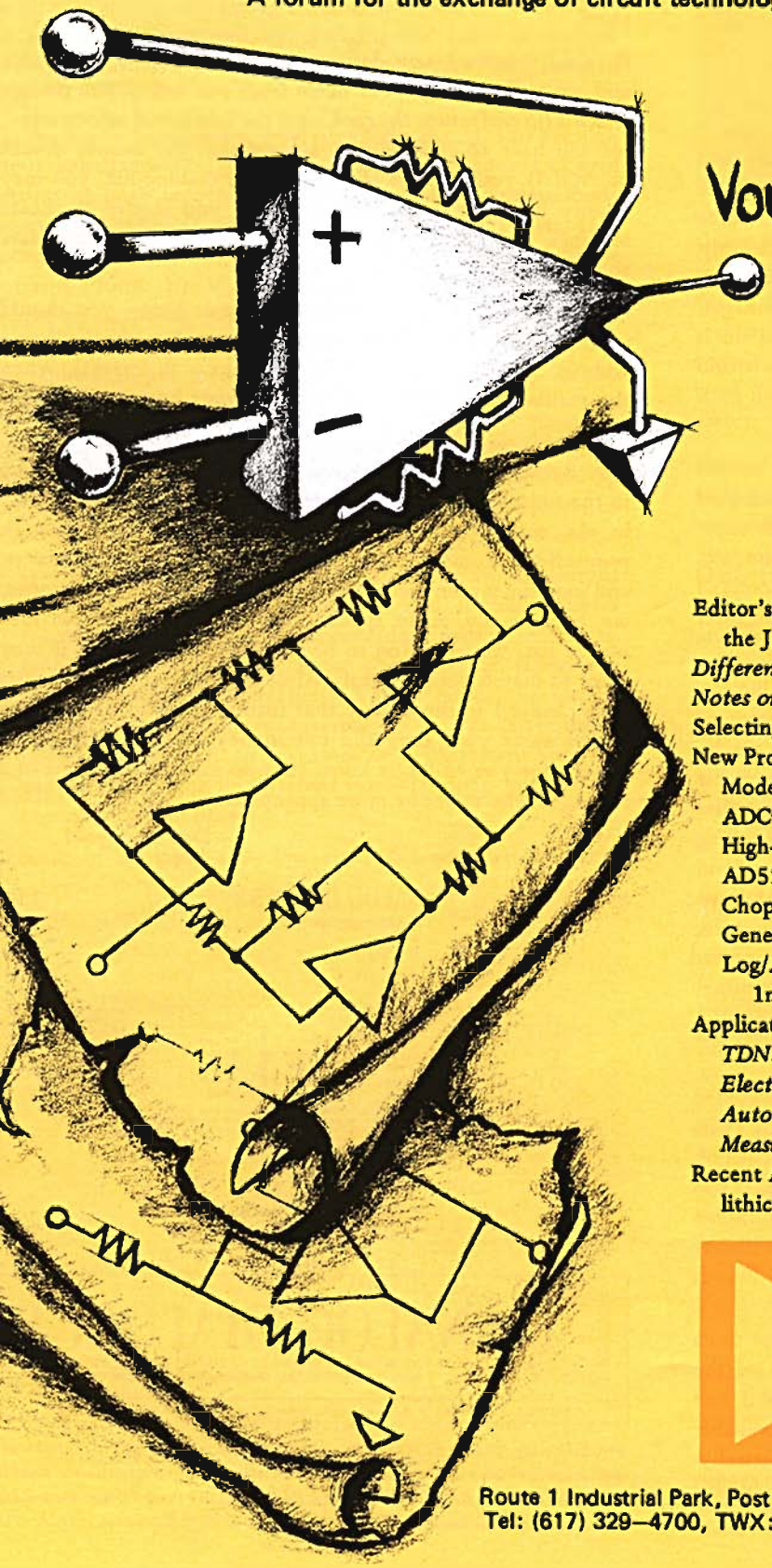
ANALOG DIALOGUE

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete



$$V_{OUT} = K(V_1 - V_2) + V_{REF}$$

MONOLITHIC DIFFERENTIAL INSTRUMENTATION AMPLIFIER
See Page 3

Contents: Volume 6, Number 1, Spring, 1972

ANALOG DEVICES
Circuit Specialists

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Editor's Notes

BETTER CIRCUITS COMING

We report here on two new corporate developments of importance to our customers and readers of *Dialogue:*

Late in October, Analog Devices acquired Nova Devices, Inc., an IC manufacturer in Wilmington, Massachusetts. This acquisition surprised no dedicated Analog-watchers, since we had furnished the major portion of Nova's financing, and Nova had furnished the major portion of Analog's integrated circuit production. The acquisition of Nova Devices continues a plan initiated three years ago to enable Analog Devices to maintain its leadership in the circuits business by utilizing any technology necessary to provide high-performance, reliable devices, in small packages, at low cost. Where it can be done monolithically, we do it monolithically; if a hybrid technique is necessary, so be it; and if discrete modules are still the most practical way, we'll do it that way, unabashedly.

In short, with all technologies at hand, our customers benefit by our not having to conform to anybody's morphological prejudices. We can (and do) even make our own monolithically-matched transistors for use in our input stages, log units, etc. (And we also put them at the disposal of our customers.) There are few companies in the circuits business that can offer *that* kind of service!

Recently, we have taken another step toward broadening our technological base. Heinrich Krabbe, of late our Director of Engineering, has been appointed General Manager of a newly-established operation in "Silicon Valley," California, to enable Analog to benefit from new developments in CMOS and junction FET processing technology. The first products are just rolling out of the ovens: matched junction FET's made by a silicon nitride process that lowers gate currents, increases breakdown voltage, and provides more-linear drift with temperature. Additional products are just behind them and will be reported on in these pages in future editions. A promising beginning!

DUAL FET's AND THE JAUNDICED EYE

Our engineering department in Norwood, long a user of matched transistors in unbelievably large quantities, has over the years developed a thick hide and a hard-bitten cynical outlook when it comes to matched FET's and suppliers of same. It was therefore with considerable gratification that we stumbled upon a communication so unusual that we've taken the liberty of reprinting it in its entirety, with only the names of brands X and Y omitted (See the adjacent column).

The answer to the question in paragraph 3 is that these units are typical in every way of our volume production of the 0.1pA-leakage-current AD830's. With our AD3954-8 and AD5905-9 series of dual-FET's (see page 13), they are available from stock, compactly packaged in TO-71-8 hermetically-sealed metal cans.

SUBSCRIPTION RENEWAL:

DO YOU WANT TO RECEIVE *ANALOG DIALOGUE?*

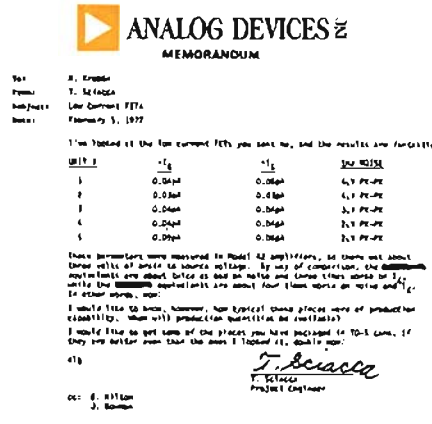
The time has come to bring our mailing list up-to-date and "requalify" our readership. Since we want to send *Dialogue* to readers who want to receive it, it makes sense to call for an affirmative act: *If you wish to remain on our mailing list, please check YES on the enclosed card,* add the information pertaining to your job and interests, note any address changes or corrections needed, and return the postpaid card to us.

If (alas) you no longer desire to receive *Dialogue,* check *NO,* and we will expunge your name from our list. *If you do not check YES and return the card, with the additional information,* we will have to (reluctantly) assume that the answer should be *NO!* If you are not already on our mailing list, you may qualify by using the enclosed card. If you receive duplicate mailings, please attach the label from the unwanted duplicate to the card for removal.

If you wish to receive *Analog Dialogue* at home, *you should still indicate your job title and company,* but check "home address" (and make sure that the address is correct). When the mailing labels are made up, only your home address will appear.

Why Requalify? Our readers, whom we like to think of as being in the most-rapidly-growing interest-area in the industry, may in the course of several years change jobs (often through promotion), companies, addresses, areas of product interest, and sometimes even their names. Since, in addition to *Dialogue,* we occasionally make special mailings to selected portions of the list, we want you to be sure of receiving them if they seem to match your interests. Also, of course, if your interests have changed so thoroughly that further mailings of *Dialogue* would waste your time and our money, it is to our mutual benefit for you to let us know (but *do* include the name of a colleague who might be more appropriate).

Dan Sheingold



ANALOG DEVICES

MEMORANDUM

To: H. Krabbe
From: T. Scacca
Subject: Low Current FETs
Date: February 3, 1977

I've looked at the low current FETs you sent me, and the results are favorable.

Unit #	$-I_G$	$+I_G$	Low Noise
1	0.04pA	0.06pA	4.1 nV-√Hz
2	0.03pA	0.03pA	4.1 nV-√Hz
3	0.04pA	0.04pA	3.9 nV-√Hz
4	0.02pA	0.04pA	3.9 nV-√Hz
5	0.01pA	0.05pA	3.9 nV-√Hz

These parameters were measured in Model 42 amplifiers, at room and about [illegible] volts of source voltage. By way of comparison, the equivalents are about twice as bad on noise and three times worse on [illegible] only the [illegible] equivalents are about four times worse on noise and I_G. In other words, wow!

I would like to know, however, how typical these pieces were of production capability. What will production quantities be available?

I would like to get some of the pieces you have packaged in TO-5 cans, if they are better than the ones I tested it, double wow!

ajb

T. Scacca
Project Engineer

cc: G. Hilton
J. Gordon

ANALOG DIALOGUE

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Monolithic Data Amplifier

DIFFERENTIAL INSTRUMENTATION AMPLIFIER ON A SINGLE CHIP HAS HIGH INPUT IMPEDANCE, SINGLE-RESISTOR GAIN ADJUSTMENT, ADJUSTABLE OUTPUT BIAS, OUTPUT-CURRENT SENSING

by Heinrich Krabbe, Director of Operations, Analog-California

The AD520* is a differential instrumentation amplifier on a single silicon chip, employing a thin-film-on-silicon technology. Its gain can be adjusted by changing the value of a single external resistor (or, more properly, its ratio to a fixed external resistor).

Unlike conventional operational amplifiers, the AD520 has high input impedance ($2 \times 10^9 \Omega$), essentially independent of gain setting, at both inputs, and it maintains high common-mode rejection (80dB @ G = 1, 110dB @ G = 1000, @ 100Hz, 1kΩ source unbalance). In addition, it has low bias and offset currents (30nA, 10nA), low linearity error (0.02%), excellent frequency response (60kHz both small-signal and full-power at G = 500), and it is short-circuit protected. It is housed in a convenient 14-pin hermetically-sealed ceramic dual in-line package.

This kind of performance is characteristic of reasonably-good instrumentation amplifiers; to obtain it with conventional op amps would require a minimum of 2 amplifiers and 4 precision resistors. The AD520 has some additional interesting features:

- It has an output *Reference* terminal that allows the output to be biased independently of the gain setting, a useful feature for positioning chart-recorder writing elements.
- It has a high-impedance *Sense* terminal that allows the circuit's feedback to be derived from either the output terminal or an arbitrary external point. The latter mode allows the AD520 to be used as a "constant"-current generator, or with an external inside-the-loop booster for increased output power.

Because of its small size, low cost, and complete-on-a-chip

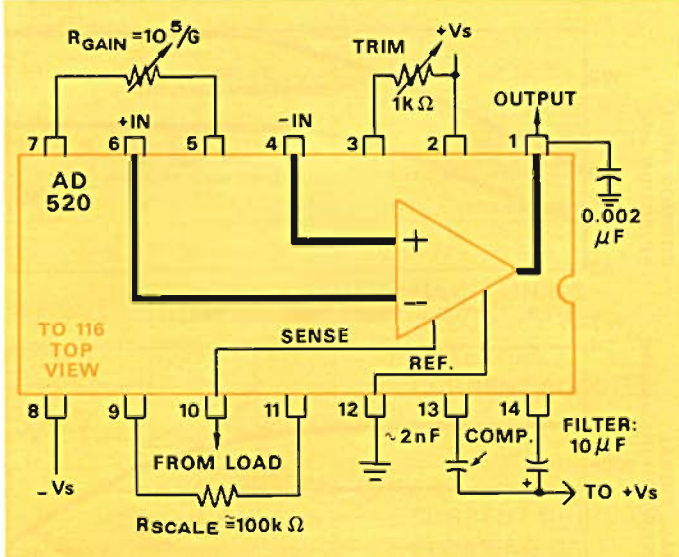
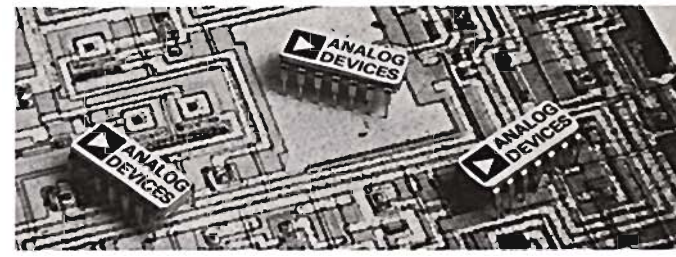


Figure 1. The AD520, in Typical Connection for Adjustable Gain, Zero Reference, and Direct Sensing

*For further information on the AD520, use reply card. Circle F1



simplicity, the AD520 offers the circuit designer an attractive alternative to both modular instrumentation amplifier packages and user-wired collections of IC op amps* and high-precision external components, for inputs to instruments, equipment, and data-acquisition systems. It can be used with thermocouples, bridges, and other balanced transducers, or as a ground-level "shifter" (within its ratings) to minimize ground-loop effects with unbalanced sources.

Figure 1 shows the connections required to use it as a simple differential amplifier with adjustable gain. Other typical application circuits appear on the following pages.

DESIGN (Figure 2)

A closed-loop system consisting of two differential amplifiers and four controlled-current sources forces a current proportional to the differential input voltage to be equal to a current developed by the output voltage. The resulting equation (1) is:

$$\frac{V_{sense} - V_{reference}}{V_1 - V_2} = \frac{R_{scale}}{R_{gain}} = G \qquad (1)$$

If the *Sense* terminal is connected to the output,

$$V_{out} = V_{reference} + \frac{R_{scale}}{R_{gain}} (V_1 - V_2) \qquad (2)$$

The relationship of equation (1) is determined as follows:

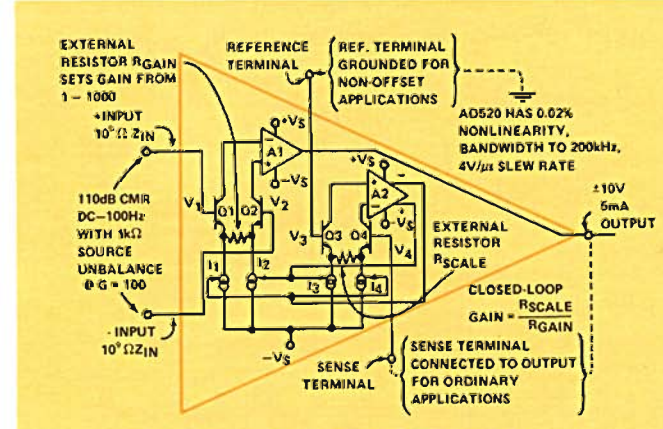


Figure 2. Basic Circuit of the AD520 Instrumentation Amplifier

*For information on Analog Devices modular instrumentation-amplifier packages, Circle F2. For information on instrument-grade IC op amps, Circle F3

Both A1 and A2 work to maintain their input differences at zero, A1 by manipulating the output voltage, and A2 by manipulating the current sources. A differential voltage applied between the input terminals produces a voltage across R_{gain}, which, in turn, produces a difference current in the collectors of Q1 and Q2. A1 seeks to null this current by increasing the output voltage. The increase in the output voltage, appearing as a difference between the *Sense* and the *Reference* voltages, produces a voltage across R_{scale}, which, in turn, produces a different current in the collectors of Q3 and Q4. A2 seeks to null this current by manipulating I_3 and I_4. Since I_2 and I_1 track I_3 and I_4, the difference current in the collectors of Q1 and Q2 is reduced. Since the currents track, equilibrium occurs when A1 adjusts the output to make ($V_{sense} - V_{reference}$) equal to the input difference voltage, multiplied by the ratio of R_{scale} to R_{gain}.

Expressed mathematically, at equilibrium,

$$I_1 - I_2 = I_4 - I_3 \text{; also, } I_1 = I_4 \text{ and } I_2 = I_3 \qquad (3)$$

The currents flowing in the collectors of Q1 and Q2 are,

$$I_1 + \frac{V_1 - V_2}{R_{gain}} = I_2 - \frac{V_1 - V_2}{R_{gain}} \qquad (4)$$

or,

$$I_1 - I_2 = 2\,\frac{V_2 - V_1}{R_{gain}} \qquad (5)$$

The currents flowing in the collectors of Q3 and Q4 are,

$$I_4 - I_3 = 2\,\frac{V_{ref} - V_{sense}}{R_{scale}} \qquad (6)$$

Whence,

$$\frac{V_{sense} - V_{ref}}{V_1 - V_2} = \frac{R_{scale}}{R_{gain}} = G \qquad \text{(Eq. 1)}$$

There are, of course, a number of well-founded tacit assumptions: that all currents and V_{BE}'s track, that the amplifiers have sufficient gain, that the current sources are modulated linearly, that all voltage swings are within ratings, etc., etc., *and* that the circuit is stable (i.e., that active equilibrium exists).

Figure 3 is a complete schematic diagram of the AD520. The amplifier is designed to give best results with a nominal value of $10^5\,\Omega$ for the external resistor R_{scale}, which corresponds to a current sensitivity of 10μA/V of output difference ($V_{sense} - V_{ref}$), or ±100μA for a ±10V output swing. The choice of nominal quiescent current (I_1, I_2, I_3, I_4) is a compromise between higher values for better linearity and bandwidth, and lower values for decreased input admittance and bias current. The design value of 200μA for each current source allows a full worst-case variation of ±100μA for $V_{sense} - V_{ref}$ = ±10V, with 100% margin of safety.

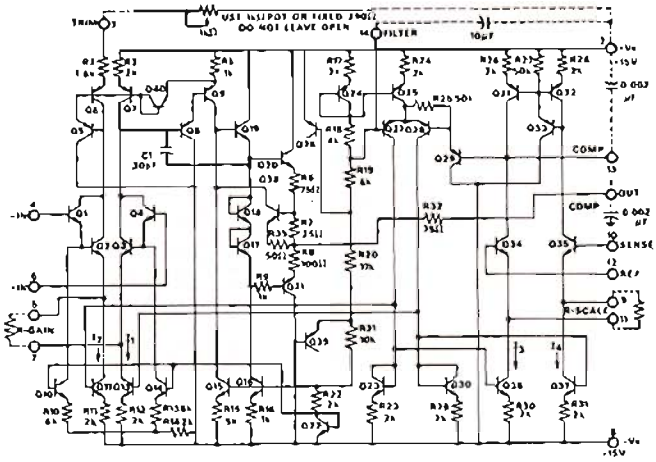


Figure 3. Complete Schematic of the AD520

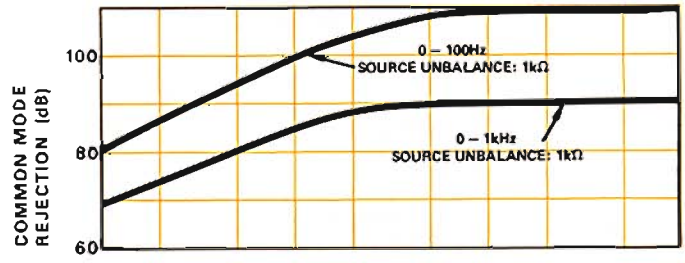
Dynamic stabilization is achieved by the connection of two external compensating capacitors, as shown in Figures 1 and 3. Thin-film resistors, deposited on the chip, are used in all critical locations to gain a 10:1 improvement over diffused-resistor performance in tracking with temperature. An additional benefit of thin-film resistors is conservation of chip area, because of their tenfold increase in sheet resistance. The chip requires an area of about 63 x 68 mils (about 2.8 square mm), a practical size to obtain good yields. A photomicrograph of the chip can be seen in Figure 5.

PERFORMANCE

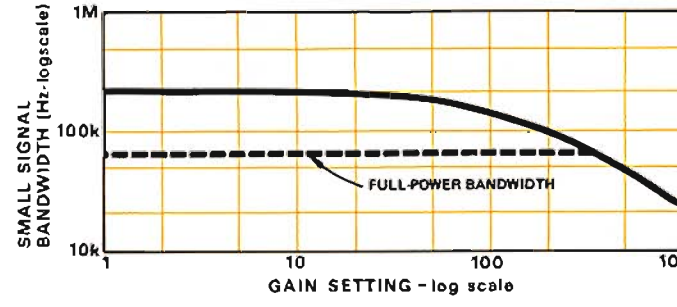
The gain linearity is inherently excellent (nonlinearity typically less than 0.02%), because of the near-perfect β-tracking of the transistors used in the four current sources over the prescribed current range. This advantage is unique to monolithic circuitry. Once the gain is calibrated for an initial unity ratio of R_{scale}/R_{gain}, it will track changes of R_{gain} within about 0.1% over a range of gains from 1:1000.

Common-mode rejection is very good, ranging from 80dB at unity gain to 110dB at gain-of-1000, with 1kΩ source unbalance, at frequencies from dc to 100Hz. At 1kHz, and gain-of-1000, CMR is 86dB. A plot of typical CMR vs gain can be seen in Figure 4.

Frequency response of the AD520 is also quite good, with full-power response to 150kHz, and small-signal bandwidth (−3dB) ranging from 250kHz at unity gain to 35kHz at gain-of-1000. Slewing rate is typically 8V/μs.



a. Common-Mode Rejection vs Gain



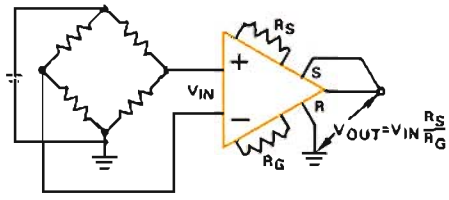
b. Small-Signal Bandwidth vs Gain

Figure 4. AD520 Performance vs Gain Setting

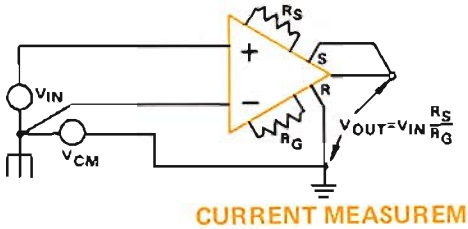
APPLICATIONS

The AD520 is a new kind of amplifier, with versatility analogous to that of the operational amplifier. It will do many jobs that would require op amps in pairs or triplets. It will perform differential measurements, both balanced and unbalanced, with good precision and the added benefits of adjustable output reference and load sensing. The few suggestive applications depicted here are intended principally as a creative stimulus to the circuit designer.

VOLTAGE MEASUREMENT



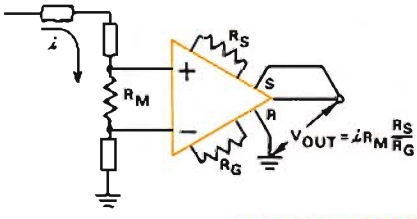
BRIDGE AMPLIFIER



GROUND-LOOP ELIMINATOR

Line Receiver

CURRENT MEASUREMENT



AMPLIFYING CURRENT MONITOR

USES OF OFFSET

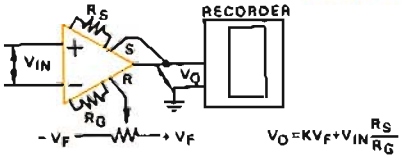
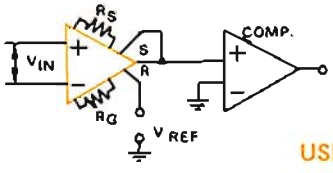


CHART POSITION BIASING

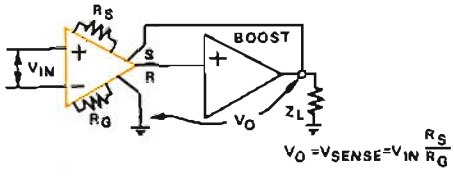
Normal-Mode Bias Compensation



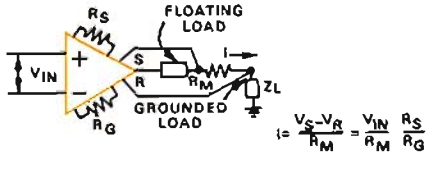
ADJUSTABLE RELAY OR COMPARATOR TRIP POINT

Control-System Set Point

USES OF SENSING



MAINTAINING ACCURACY WITH EXTERNAL CURRENT BOOSTER



CURRENT DRIVE TO FLOATING OR GROUNDED LOAD

AD520 CHARACTERISTICS

(Typical @ 25°C and ±15V supply unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max	Units
Gain					
Initial[1]	$R_{scale} = R_{gain} = 100k\Omega$	0.95	1.00	1.05	V/V
Adjustment Range	$V_o = \pm 10V$	1		1000	V/V
Nonlinearity	$V_o = \pm 10V$		0.02		%FS
Output					
Voltage Range	$I_L = \pm 5mA$	±10	±11		V
Impedance	f = 100Hz		2		Ω
	G = 100				
Response					
Small-signal	G = 1		200		kHz
Bandwidth	G = 10		175		kHz
	G = 100		125		kHz
	G = 1000		25		kHz
Full-power	G = 1 - 500		60		kHz
Slew Rate			4		V/μs
Common-Mode					
Rejection	f = dc to 100Hz				
	R_i imbalance = 1kΩ				
	G = 1		80		dB
	G = 10		100		dB
	G = 100		110		dB
	G = 1000		110		dB
	G = 1000 f = 1kHz		86		dB
Power-Supply Rejection	G = 1000		95		dB
Input Characteristics					
Impedance	Either input		2×10^9		Ω
Bias Current	Either input		20		nA
Offset Current			10		nA
Voltage Drift	0° - 70°C, G = 1		0.01		%FS/°C
	G = 100		0.05		%FS/°C
Noise (p-p)	dc to 10Hz		0.01		%FS
Absolute Maximum Ratings					
Supply Voltage				±18	V
Power Dissipation				500	mW
Differential Input Voltage				±10	V
Input Voltage, Either Input				$\pm V_s$	
Storage Temperature Range		-65		+150	°C
Operating Temperature Range		0		70	°C
Output Short Circuit Duration				Indef.	
Lead Temperature (Soldering, 60 sec)				+300	°C

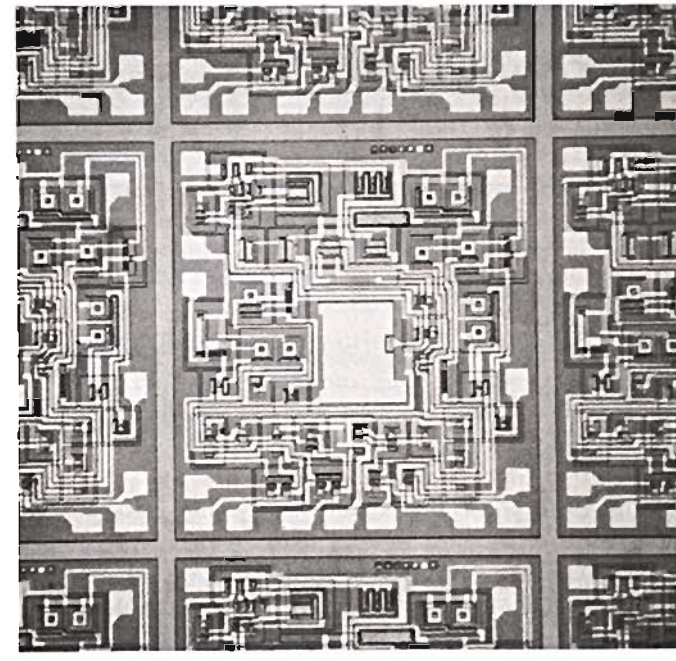


Figure 5. Photomicrograph of AD520 Chip

[1] When R_{scale} is trimmed for G = 1, gain formula is $G = 10^5/R_{gain}$.

Notes on Converter System Component Selection

by Cy Brown, Marketing Manager — ADI Converter Products

LET THERE BE LIGHT!

The applications for digital data-handling equipment, and for its rapidly-growing handmaidens, the products of the conversion-and-data-acquisition industry, have spawned a terrifying multiplicity and diversity of companies, product lines, and products. We find it sobering (though not a little gratifying!) to discover that, as a major manufacturer, with a reasonably-complete line, we can deliver some 250 distinct D/A converter types, and that that line alone is growing by 75 types per year.

Thus, the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence of standardized definitions of specifications among the manufacturers. To remedy this situation, and attempt to make the system-designer's job a little easier, we list here some of the steps a user can take to help him "home in" on a near-optimum selection. On the opposite page, we show how one engineer made a choice and confirmed its efficacy. (Ed.)*

TWO BASIC FACTORS

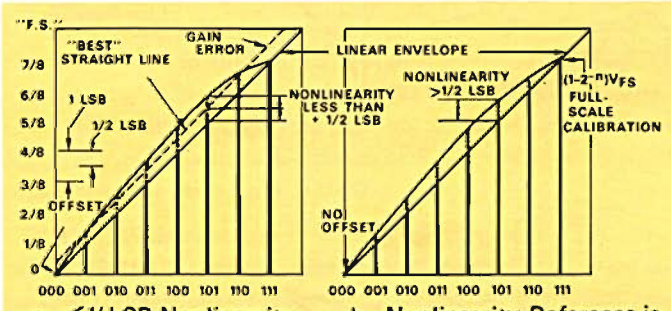
The two key factors in choosing the right device are:

- **Completely define the design objectives.** Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interface, environmental conditions and space factors, anticipated budgetary limitations that may force performance compromises.

- **Understand what the specs mean.** It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed that any two manufacturers mean the same thing when they publish identical numbers defining a given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. For example:

D/A Converter Linearity. The conventional definition of nonlinearity of a device is deviation from a "best straight line." To determine whether a device meets the stated linearity specification, the shape of the nonlinearity and its amplitude have to be known so that the end points (e.g., the zero and full-scale points for a unipolar device) can be offset by a "best" amount to minimize linearity error. As Figure 1a shows, by the use of this criterion, a bowed nonlinearity may be specified as ½ the worst case deviation from the straight line obtained by calibrating the end points. This is fine if you're a vendor and want to prove that the device meets its specs, but it's of little help to the user, who needs the specified linearity for a unit that has been calibrated for zero and scale factor.

For this reason, even though it makes our design and Q.C. jobs twice as hard, Analog Devices specifies nonlinearity of converters as the *maximum* deviation, at any point, from the calibrated linear relationship (Figure 1b). The user now needs only to set the two end points, according to the standard calibration procedure. The normal limit used is ±½LSB (least significant bit). This then means that the sum of positive errors or the sum of the negative errors of the individual bits must not exceed ½LSB, which means, further, that the errors of the bits themselves must be considerably less than ½LSB.



a. <½LSB Nonlinearity Achieved by Arbitrary Location of "Best Straight Line"

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of Fig. 1a

Figure 1. Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification

APPLICATION CHECKLISTS

General Considerations

A. Accurate description of input and output
   1. Analog signal range, source or load impedance
   2. Digital code needed: Binary, 2's Complement, BCD, etc.
   3. Logic-level compatibility: TTL, CMOS, etc., logic polarity

B. Data throughput rate

C. Control interface details

D. What does the system error budget allow for each block?

E. What are the environmental conditions: temperature range, supply voltage, recalibration interval, etc., over which the converter should operate to the desired accuracy?

Besides these general considerations, there are specific items to consider when choosing each block in a system.

Considerations for D/A Converters

A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted. To what degree of accuracy, linearity, etc.?

B. What logic levels and codes can be provided to the DAC? The most popular logic system is TTL, and the most-frequently-used codes are binary, 2's complement, offset binary, BCD, and their complements.

continued on page 8

*This article is based on material in the Converter-Product Selection Guide, to be found in the 1972 full-line catalog from Analog Devices, available in March. If you are on the mailing list for *Analog Dialogue*, your copy has either arrived or is about to arrive. Otherwise, Circle F4

SELECTING COMPONENTS FOR A SYSTEM — A BRIEF EXAMPLE*

THE PROBLEM

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers ±10V full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is +25°C to +55°C. Sufficient power at both ±15V and +5V is available, but the regulation of the ±15V supply is 150mV.

The objective: Specify a set of conversion components having appropriate accuracy and speed.

FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with compatible multiplexer and sample-hold.

Reviewing the available A/D converters, we find the ADC-12Q and ADC-12QM to be possible choices. If the entire system is to be built on a single card, the ADC-12QM, a 2" x 4" x 0.4" encapsulated module would be a convenient choice.

The ADC-12QM completes a conversion in 25μs. For sample-hold, the compatible SHA-1A is chosen, adding 5μs of settling time. Thus, the combination appears to be amply capable of meeting the 50μs/channel scanning requirement. Since the multiplexer will scan sequentially, its settling time is inconsequential. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least 25μs to settle before a measurement is called for. For convenience, one may use the MPX-8A; the small 2" x 2" x 0.4" module fits into the packaging concept, and the built-in complete binary-address decoding makes it easy to work with.

ERROR ANALYSIS

It's clear that the MPX-8A, the SHA-1A, and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst-case situation is within the allowable 0.1% system error.

Multiplexer (MPX–8A)†

The switches of the MPX-8A, being MOSFET's with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.
   Leakage current @ 25°C 10nA
   Source impedance 10Ω
   Error voltage = $10 \times 10 \times 10^{-9} = 10^{-7}$ V (negligible)
2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the SHA-1A:
   ON resistance 1000Ω maximum
   SHA-1A R_{in} $10^{12}\Omega$
   Divider ratio attenuation error: 10^{-9} (negligible)

Sample-Hold (SHA-1A)†

1. Nonlinearity is 2mV over the 20V range, or 0.01%
2. Gain error of 0.05% maximum (and other similarly small initial gain errors in the system) may be compensated for overall when calibrating the system by setting the scale constant of the ADC. Gain T.C. of a follower-type Sample-Hold, as used in this example, is insignificant.
3. Input bias current of 10nA (max) causes an offset error voltage in the source resistance.
   Source resistance = $10\Omega_{(source)} + 1k\Omega$ (MPX switch)
   Offset error = $10^{3} \times 10^{-8} = 10\mu V$ (negligible)
4. Offset vs temperature = 25μV/°C

Since the temperature inside the housing may change by as much as 30°C, the total change over the range will be
25 x 30 = 750μV, or 7.5ppm of ±10V

An offset adjustment is provided for initial trimming.

5. Offset vs power supply = $100\mu V/\%\Delta V_S$

Since the supply may vary by 150mV, or 1% of 15V, the error contribution is 100μV, or 0.01% of full scale.

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate- and settling-time allowances. However, the components selected for this example have better-than-adequate settling time, even for 0.01% operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Converter (ADC-12QM)†

1. Specified linearity error (relative accuracy) ½LSB, or 0.0125%.
2. Quantizing uncertainty: ½LSB, or 0.0125%. This is a resolution limitation, not normally considered in the error budget.
3. Temperature errors
   a. Gain temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150ppm, or 0.015%
   b. Zero temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150ppm, or 0.015%
4. Power supply sensitivity error: $0.002\%/\%\Delta V_S$
5. Differential nonlinearity temperature coefficient, 3ppm/°C. For 30°C temperature change, error is 90ppm, less than ½LSB. Therefore, 12-bit monotonicity can be maintained, with no missing codes.

CONCLUSION

The worst-case arithmetic sum of these errors is 0.07%, and the rms sum is 0.03%. Since these values are reasonably conservative for a system with specified error of 0.1%, the designer may either rest with these choices and go on to the more-difficult hardware, software, interface, and wiring problems, or — if absolute-minimum cost of conversion hardware is an important objective — seek to reduce cost by considering a more marginal design.

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*For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the less-salient sources of error have been intentionally omitted. If there are any that you're concerned about for your application but don't see here, we invite you to communicate with the author.

†For technical data on these 3 products, use reply card. Circle F5

continued from page 6

C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier. Voltage-output DAC's are the more convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μs and sub-μs settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators, e.g., A/D converters, or where fast amplification is to be provided externally, e.g., via CRT deflection amplifiers.)

D. What are the speed requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy . . . for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed within the DAC?

E. Over how wide a temperature range (at the module – i.e., ambient plus temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment?

F. How stable are the terminal voltages of the power supplies that will power the DAC? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits?

Considerations for A/D Converters

The process of selecting an A/D converter is similar to that involved in the selection of D/A converters. The following considerations are typical:

A. What is the analog input range, and to what resolution must the signal be measured?

B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?

C. To what extent must the various sources of error be minimized as environmental temperature changes? Are missed codes tolerable under any conditions?

D. How much time is allowed for each complete conversion?

E. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system?

F. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter. (A/D converters are designed according to several different circuit philosophies: e.g., successive approximation, dual-slope integration, counter-and-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively-slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1MHz. Counter-comparator types provide lowest cost, but may be both slow and noise-susceptible.)

Considerations for Multiplexers and Sample-Holds

When a sampled-data system is to be assembled, in which one A/D converter is time-shared among many input channels by using a multiplexer and a sample-hold, the contribution of these accessory devices to system performance errors must be taken into account.

Multiplexers

A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?

B. What kind of addressing scheme is to be used?

C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?

D. How much ac crosstalk error between channels is allowable? At what frequencies?

E. What error is produced by the leakage current flowing through the source resistance?

F. What will be the multiplexer "transfer" error, produced by the voltage divider formed by the *On* resistance of the multiplexer and the input resistance of the sample-hold. Is multiplexer active or passive? (Does it have an output amplifier?)

G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test and calibration purposes?

H. Is there danger of damage to active signal sources when the power is turned off? MOSFET multiplexers are inherently "safe," since the switches open when power is removed. JFET multiplexer switches usually close when power is removed, making it possible to interconnect, and therefore damage active signal sources. (MOSFET's are used as switches in *all* ADI multiplexers.)

Sample-Holds

A. What is the input signal range?

B. Considering the slewing rate of the signal and the multiplexer's channel-switching rate, what is the sample-hold's allowable acquisition time to within the desired error band?

C. What accuracy is needed (gain, linearity, and offset errors)?

D. What aperture delay and jitter are allowable, going into *Hold?* The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, 1V/μs produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance, but jitter modulates the sampling rate.

E. How much "droop" in *hold* is allowable?

F. What are the effects of temperature, time, and power supply variation?

G. What offset error is caused by the flow of the sample-hold's input bias current through the series resistance of the multiplex switch and the signal source?

SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of successive approximations: Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy. If its performance seems far in excess of that needed (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember that in a maturing industry, costs can be expected to decline. *It is often less costly in the long run to go for better performance rather than lowest possible cost in the initial stages of design.*

Wideband Precision Instrument Amplifier

MODEL 604L HAS 0.5 μV/°C DRIFT 25μs SETTLING TIME TO 0.01%

Model 604* is an instrumentation amplifier that combines excellent small-signal handling capability with fast response speed. Its gain, programmed by a single external resistor, can range from 1 to 1000. Maximum drift rates are as low as 0.5μV/°C (604L) and 0.1nA/°C, with 1.5μV wideband rms voltage noise (gain-of 1000), referred to the input.

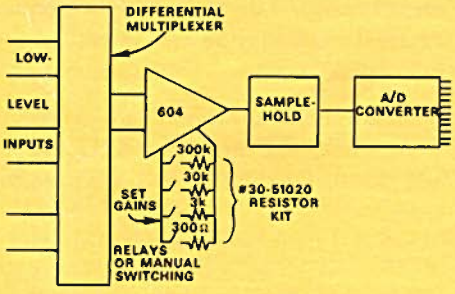
Essentially independent of gain setting, full-power and small-signal (−3dB) bandwidth are both about 50kHz, and settling time to 0.01% is well below 50μs at gain of 1000. DC CMR is 120dB at gain of 1000; maximum nonlinearity is 0.01%.

Its applications include accurate pre-amplification of small signals from transducers, differential-to-single-ended buffer amplification, and amplification of multiplexed input signals in data-acquisition systems.

Instrumentation amplifiers typically available on the market tend to be specialized: they are either very fast, or very slow and accurate; very "cheap-and-dirty," or very good, large, and expensive. The design objective of the 604 was to approach the best attributes of these amplifiers, whilst avoiding their less attractive features. To be, in short, a "universal" amplifier at reasonable cost.

DATA ACQUISITION

The figure shows an example of a typical application of the 604 in a multiplexed data-acquisition system. A group of low-level input signals with slow voltage variations, are to be converted to digital form.



*For further information on Model 604, use reply card. Circle F6

Low-level multiplexing and the 604 eliminate the need for many amplifier channels, with their cost and space requirements.

Because of the 604's short settling time, the multiplexer may switch channels quite rapidly. If, for example, 8 channels are switched at an 9kHz rate, 1000 samples of each input can be acquired in one second, allowing a 1.75Hz sine wave to be reproduced with less than 1.0% phase error.

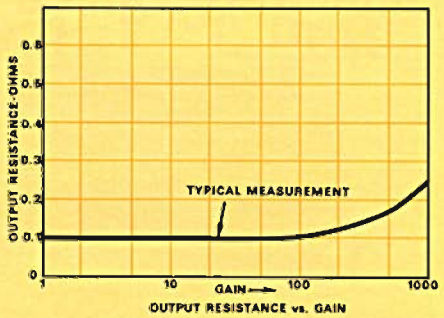
For this application, the 604 is used as a semi-programmable-gain amplifier. The gain setting applies to all channels equally. Therefore, it is desirable that signals having similar amplitude ranges should be applied to a given 604.

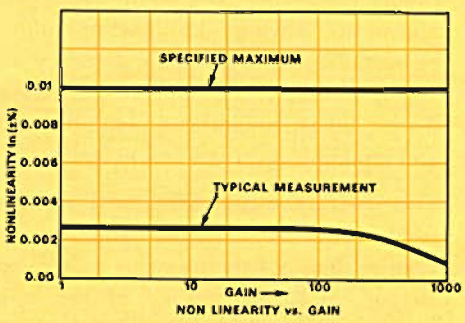
SENSE AND REFERENCE

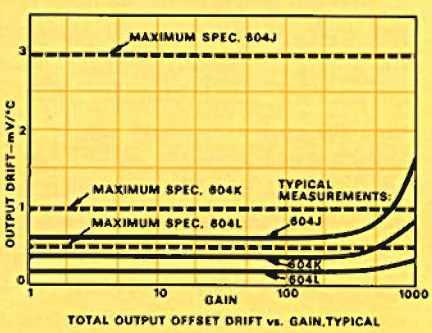
Like the AD520 (page 3 *et seq.*), Model 604 has *sense* and *reference* terminals, which serve comparably to those of the AD520: The *sense* terminal is used as the actual feedback point, allowing a booster to provide output in excess of the rated ±10mA at ±10V, without loss of accuracy; the *reference* terminal can be used to add a constant to the output, independently of the gain setting.

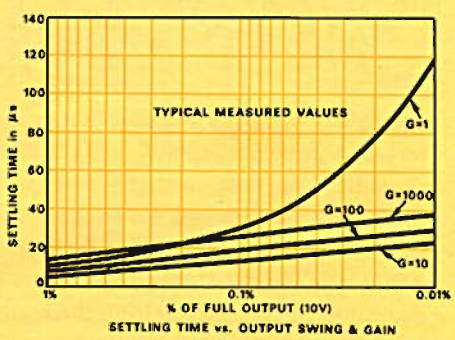
The adjacent curves illustrate some of the typical performance aspects of the Model 604.

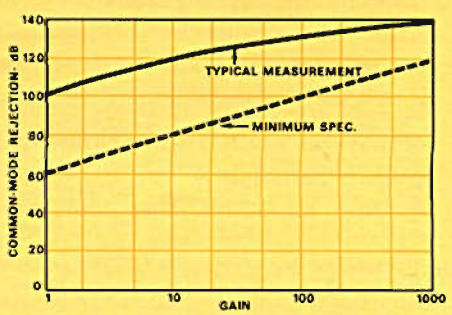
Housed in a 2" x 3" x 0.4" epoxy module, the Model 604 is available from stock. Price (1–9) is $155 for 604J (3μV/°C), to $205 for 604L (0.5μV/°C), less in quantity. ▶▶▶





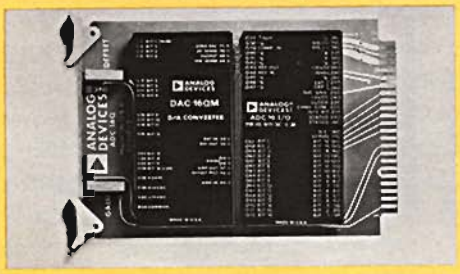






Two New A/D Converters

ADC-16Q: For Supreme Resolution, Moderate Speed



Model ADC-16Q* is a 16-bit binary A/D converter having 15 part-per-million resolution, and comparable accuracy and stability. Differential input circuitry allows 3-wire input, minimizing common-mode and ground-loop errors and noise.

The successive-approximations scheme results in quick conversion: maximum conversion time is 4ms following a 20V step change, *including settling of the input differential amplifier to within 8ppm of full scale.* If the converter is measuring small (e.g., millivolt) changes about a constant or slowly-changing level, the time for each conversion can be as little as 400μs, or less.

WHY 16-BIT RESOLUTION?

As yesterday's state-of-the-art becomes tomorrow's modest performance, data-acquisition systems and test instrumentation continually require higher levels of performance, in order to stay one jump ahead.

For example, 12-bit A/D and D/A converters are now commonplace, being available at quite low cost, and 13- and 14-bit converters have ceased to be laboratory curiosities. 16-bit converters, such as the ADC-16Q and the DAC-16QM† have become useful tools for testing them automatically by exercising each and every bit within a reasonable time, without introducing appreciable measurement error.

In data acquisition, there are a number of ways in which 16-bit converters can prove to be useful:

- Most obviously, they can resolve signal fine structure with a large number of quantized levels: 65,536, to be exact, or 15ppm.
- They can accurately measure signals having wide dynamic range without the added cost and delay of automatic gain-ranging amplifiers.
- They can measure small deviations accurately at any level, a useful feature for production testing of drift in batteries, power supplies, regulators, zener diodes, etc.

SIZE, SPEED, AND RESOLUTION

The ADC-16Q is built on a compact, 4½" x 6" plugin card, designed specifically for the equipment and system designer. Unlike the large, DVM-type boxes, it has fast operating speed, absolutely no frills, and will work from standard +5V and ±15V system power supplies.

Unlike some other 15-bit cards (we are not aware of any compact 16-bit units), it combines 16-bit resolution with commensurate linearity, accuracy, and stability.

- Nonlinearity is less than ±15ppm locally (individual bits) and 5ppm over the input range, for temperatures from 20° to 30°C, with monotonicity guaranteed. From 0° to 70°C, maximum nonlinearity is ±50ppm.
- Temperature coefficients of scale factor and zero are ±8ppm/°C and ±2ppm/°C (±2½ppm/°C for the buffer), respectively.
- Linearity, scale factor, and zero are stable within, respectively, ½, 3, and 2ppm for 24 hours; 5, 30, and 20ppm for 30 days.

The ADC-16Q, as befits a device designed for equipment and system, rather than DVM applications, uses binary coding. It may be connected for offset-binary or 2's-complement coding for bipolar applications. The user may also connect the unit: to accept a variety of input full-scale ranges; to bypass the buffer amplifier; for a range of clock rates; and for a choice of lesser resolutions (and greater speed).

ADC-16Q is available from stock, at $1,350. ▶▶▶

*For complete information on the ADC-16Q, use the reply card. **Circle F7.**

†For complete information on the DAC-16QM, **Circle F8.**

ADC-12QU: High Performance, Low Drift

The ADC-QU* series of A/D converters, encapsulated in compact 2" x 4" modules, offer excellent linearity, fast conversion speed, low temperature coefficients, high input impedance, and versatile connections. Besides the 12-bit ADC-12QU, 10- and 8-bit units are also available.

Analog Devices' proprietary AD551† monolithic quad switches and matched resistor networks are used, resulting in maximum differential nonlinearity T.C., for the 12-bit unit, of only 3ppm/°C. Response is monotonic, with no missed codes, over the entire 0° to 70°C range. Extended-temperature-range versions are also available.

Scale factor and zero T.C.'s are ±5ppm/°C and ±50μV/°C. The ADC-12QU performs a complete conversion in 15μs; the 10- and 8-bit units, somewhat faster, perform complete conversions in 6.5 and 4μs. Either binary or BCD coding is available.

A built-in unity-gain buffer follower is available to minimize loading of the signal circuitry, and to serve in either passive or active filtering. Other built-in options include: parallel and serial outputs; choice of scale factors; unipolar or bipolar inputs (offset binary or 2's complement coding). If desired, an asynchronous external clock may be used instead of the internal clock.

Standard ADC-QU types are available from stock, and priced at $315, $290, and $260, for 12, 10, and 8-bit resolutions. ▶▶▶

*For further information on ADC-QU converters, use the reply card. **Circle F9.**

†For further information on IC converter components, **Circle F10.**

Three New I.C. Op Amps

AD523 <1 pA I_{BIAS}, Fully Compensated

The AD523* is a J-FET-input operational amplifier designed for near-electrometer applications. Three choices of maximum bias current: ¼, ½, and 1pA, are available, with the designations AD523L, K, J.

Analog's depth of experience with devices for low-current measurement (our readers may recall the Model 310K† parametric op amp, with its 10fA I_b) now includes IC's in an improved TO-99 case.

There are at least *3* major differences between the AD523 and FET-input IC's typically available from other sources.

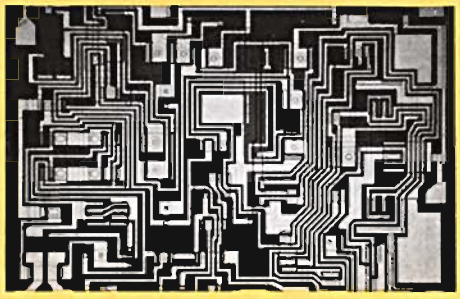
- The bias current is specified for *fully-warmed-up* units at 25°C ambient. IC op amps, handled at high speeds and tested automatically, are given little time to warm up. Since junction temperature can normally rise as much as 20°C, such devices, operating in the user's circuit, may exhibit 4x the specified I_{BIAS}. Not so the AD523! The "fully-warmed-up" spec gives you what you pay for.
- I_{BIAS} is specified for the worse of the two inputs, rather than the average, protecting the user against finding 0.1 and 1.9pA at the inputs of a "1pA" unit.‡
- The TO-99 package, manufactured with high-resistivity-glass insulation, has a guard terminal connected to the can to minimize surface leakage currents, power-supply-induced noise, and capacitive pickup.

The AD523 is short-circuit protected, offset-voltage-nullable, and compensated for full feedback. Maximum voltage drift is 30μV/°C (AD523K); and impressive *min* specs for CMR (80dB), gain (40,000), and slew rate (3V/μs) complement the excellent leakage specs.

Prices (1–24) are $28, $25, and $21, for the L, K, and J versions, dropping to $18.75, $16.75, $14., for 100+. You can buy an evaluation package of 5 units at the 100's price: mention *Dialogue*.

*For further data on the AD523, Circle F11
†For data on the Model 310, Circle F12
‡Murphy's Law tells us that the 1.9pA will always appear at the *signal* input.

AD508: Monolithic Chopperless Op Amp Super β Inputs, <1μV/°C Drift



The AD508* design is an improvement on that of the highly-successful AD504† low-drift operational amplifier. It adds the advantages of super-β processing for the input stage to increase differential input impedance to 5MΩ, and to reduce bias current to 20nA (max) and offset current to 5nA (max). Performance vs temperature is improved, too. From 0°C to 70°C, maximum offset voltage (AD508L) is reduced to 0.9mV, offset TC to 1μV/°C trimmed (and 2μV/°C untrimmed) I_{BIAS} to 30nA, and maximum offset current to 10nA.

Besides the many improved input specifications, the AD508 retains the many basic advantages of the AD504 design. These include single-capacitor compensation, fully-protected inputs, capability of driving up to 1000pF load capacitance, and virtual immunity to (and rapid recovery from) thermal transients, whether generated on the chip, externally, or at turn-on.

With gain >10^6, CMR >110dB, and offset less than 0.9mV (adjustable to zero), it is ideally suited for numerous low-level applications in precision measurement, telemetry, and data acquisition. Typical circuits for which it is an ideal choice include preamplifiers for thermocouple and bridge outputs, stable voltage sources, and buffering of passive circuitry.

It has unusual dynamic properties for amplifiers of this type: slew rate of 0.12V/μs, 20μs settling time to 0.01%, and choice of bandwidth with a single external capacitor: with 3.9pF, the response is down 3dB at 100kHz.

The AD508 is available from stock in three grades, depending on offset and drift spec: J – 2.5mV, 5μV/°C; K – 1.5mV, 3μV/°C; L – 0.5mV, 1μV/°C, at 1–24 prices of $21.20, $29.80, $38.

*For complete information on AD508, use the reply card. Circle F13
†For data sheet and application note on AD504, Circle F14

AD507: GENERAL-PURPOSE OP AMP 100MHz G-BW, 35 V/μs Slew Rate

The AD507‡ is a high-performance monolithic operational amplifier that combines slew rates of 35V/μs and 100MHz gain-bandwidth with bias and offset currents below 10nA, and gain of 150,000.

They are intended for applications where performance superior to that of the popular AD741 or AD101A series is required. They are especially well-suited for use in fast, high-impedance comparators, integrators, wideband amplifiers, and in sample-hold circuits.

The AD507 is stable at closed-loop gains greater than 10, with 6dB/octave open-loop rolloff. External compensation provides stability to unity gain and permits flexibility for special dynamic feedback characteristics. The circuit is short-circuit protected and offset-voltage-nullable. The AD507J has typical offset voltage drift of 15μV/°C (0° - 70°), which is guaranteed maximum for the AD507K. Prices (1–24) are $9 for the J and $12.25 for K.

‡For further information on the AD507, Circle F15

Log/Antilog Modules

MODEL 755: COMPLETE & SELF-CONTAINED

- Log Ranges: 1nA to 1mA, 1mV to 10V, for Rated Performance
- Better (10pA max I_B), Smaller (1½"^{2} x 0.4"), Cheaper ($55., 1–9)

The output voltage of Model 755*, in the *log* connection, is proportional to the logarithm of the input voltage or current, with ½% log conformity guaranteed over 4 decades, and 1% over the full range of 6 decades of input current. In the *antilog* connection, the inverse function is performed: output voltage is an exponential function of input voltage.

Three classes of applications stand out among a wide variety of possible uses:

- Signal compression and expansion
- Linearization of log or exponential transducers and other devices
- Mathematical functions for analog computing

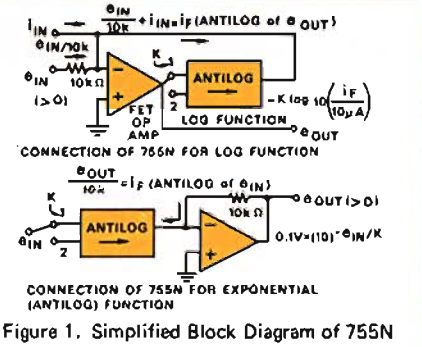


Figure 1. Simplified Block Diagram of 755N Showing Log- and Antilog Connections

The Model 755 consists of a temperature-compensated antilog voltage-to-current transducer and a low-bias-current FET-input operational amplifier. When the antilog device is fed back from the output of the amplifier, its current into the summing junction must be equal and of opposite polarity to the input current, a condition satisfied only if the output of the amplifier is proportional to the logarithm of the input signal. When connected in the *antilog* mode, the signal is applied directly to the input of the antilog device, and its output current is transduced into a voltage by the op amp. Figure 1 illustrates these connections, and shows the corresponding idealized mathematical relationships.

*For complete information on Model 755, use the reply card. Circle F16

The log sensitivity, K, in volts per decade (a 10:1 change of input) has a choice of two fixed values, 1, or 2, depending on the connection; and K = 2/3 may be embodied by tying both terminals together. The reference current (when i_{IN} = I_{REF}, the log is zero) is preset at 10μA, which corresponds to an input voltage of 0.1V. Since log x is defined as a real variable only for positive values of x, two versions of the Model 755 are manufactured: the 755N, to obtain the log of positive input voltage, and the 755P (which contains a negative reference) to obtain the log of a negative input voltage.

The input-output relationships of both types are shown in Figure 2, using a semi-log plot. A linear plot of a portion of the characteristic is also shown, to illustrate both the polarity relationships and the advantages of log compression.

Figure 3 shows an example of a system

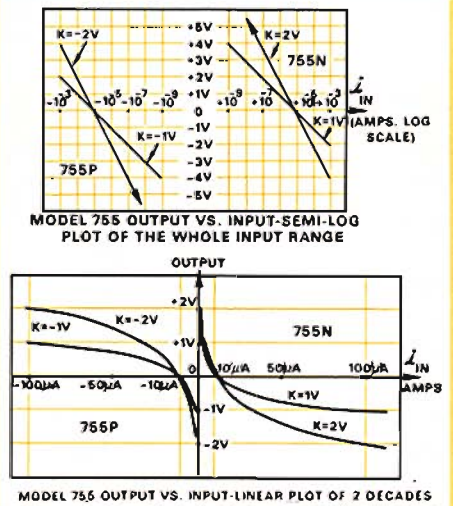


Figure 2. Log Module Performance. Comparison of 755N and 755P. Maximum output is ±10V.

application of the low-cost 755, in which a 4½-decade current range is compressed to a 9-volt logarithmic range, with 8.6 millivolts representing resolution of 1% of actual value anywhere in the 4½ decade range. (One part in 3.2 million of full scale, at the bottom of the range!) The compressed signal can be handled easily by components having modest performance and realistic cost.

Both versions are available from stock at $55 (1–9), less in quantity.

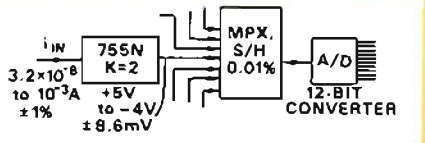


Figure 3. Using Model 755 for Range Compression in Data-Acquisition System. (From About 22-Bit Resolution to 12 Bits)

MODEL 752 LOG/ANTILOG TRANSCONDUCTOR

Get Lowest Cost or Better Resolution by Choosing an External Op Amp

Model 752* is essentially the antilog transconductor employed in the 755. Since the resolution at the low end is limited by the op amp's offset voltage or bias current, the 752 allows an external op amp to be used for better resolution.

- Use the chopper-stabilized Model 233J with the 752 for overall 200μV resolution, to rated accuracy.
- Use Model 42J "electrometer" FET-input op amp for rated accuracy from < 100pA to 1mA.
- Use the Model 40J FET-type with the 752 for 755 performance at lowest cost. Model 752 is available from stock, at $32.

*For complete information on Model 752, use the reply card. Circle F17

TDN: Temperature-Drift Nonlinearity— A New Dual-FET Specification

GETTING PREDICTABLE 5μV/°C MAXIMUM DRIFT FROM 50μV/°C TRAK-FET's

The most common application for dual FET's is as high-impedance inputs for instrument circuits. Quite often, they are used with IC op amps, functioning as an external high-impedance input stage (Figure 1). In such applications, the FET's picoampere-level bias current greatly reduces the drift that would be caused by the flow of the basic amplifier's bias current through high resistance paths. FET's can add substantial amounts of voltage drift, because — conventionally — they have been hard to match (or if well-matched, they are expensive or have some other problem.) This is unfortunate, because the basic amplifier is often capable of quite low voltage drift.

We discuss here briefly the devices resulting from a new FET process that not only provides excellent yields of low-leakage devices with low drift, but also allows the drift to be further reduced, in a predictable way, because of the linearity of offset with temperature.

More than a year ago, we introduced, in these pages* two families of monolithic matched-dual-FET's: the medium-geometry AD3954-8, with maximum gate current of 50pA, maximum offsets from 25-50mV, and maximum drifts from 5 to 100μV/°C; and the small-geometry AD5905-9, with maximum gate currents of 1pA, maximum offsets of 20-75mV, and maximum drifts from 5 to 75μV/°C.†

We also discussed the advantages they had over both two-chip hybrid assemblies (better tracking, better thermal transient rejection, lower cost), and interdigitated monolithics with common back gates (virtual elimination of bulk bias problems and gate-to-gate breakdowns). And we showed a number of examples of applications of dual FET's, including their use as input stages with low cost general-purpose op amps, such as the AD741.

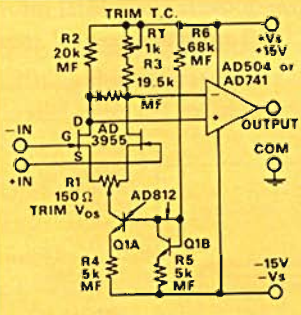


Figure 1. TRAK-FET Used in Differential Op Amp for < 5μV/°C Drift, 5pA Typ. I_b

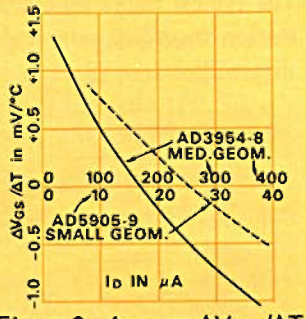


Figure 2. Average $\Delta V_{GS}/\Delta T$ vs Drain Current for Single FET Unit

Since then, a new process has been developed for manufacturing these FETs, using silicon nitride and low-dislocation diffusion techniques. The result is: better yields, lower leakage current (0.1pA *max* is routine for the AD830), less drift with temperature, and — of great importance — highly-linear drift with temperature, due to their superior tracking. The new devices bear the same type numbers and specifications as their earlier namesakes, are now available from stock (completely replacing the earlier devices), and they cost no more. In addition, they bear a new specification, *Temperature-Drift Nonlinearity (TDN)*, of 5μV/°C maximum (typically 1μV/°C), which allows the user the option of purchasing low-cost, moderate-drift (e.g., 50μV/°C) units and, with a modicum of "tweaking," obtaining 10:1 improvement routinely. We call these new FET's TRAK-FETs™.

OFFSET, DRIFT, AND TDN

Since single FET's have V_{GS} of 0.5 to 4 volts and $\Delta V_{GS}/\Delta T$ ranging from 0 to ±1mV/°C or worse (Figure 2), they are generally unsatisfactory for low-drift dc amplifier applications, even when great pains are taken to operate them at their "zero-drift" drain current. (Typical sensitivity of ½-AD3954 types to drain current is about 6.1μV/°C/μA, or 12.2μV/°C/% ΔI_D, and for ½-AD5909, 33μV/°C/μA, or 10μV/°C/% ΔI_D). When used in matched pairs, the initial dc offset $V_{GS\,1\text{-}2}$) is less than 50mV, typically 5mV, thermal drift ($\Delta V_{GS1\text{-}2}/\Delta T$, is less than 100μV/°C (Figure 3), typically 5μV/°C, and it is independent of small variations in drain current for equal drain currents.

Since the T.C. is a function of drain current, it ought to be possible to reduce temperature drift by unbalancing the drain currents. For example, if temperature drift for the pair, with equal currents, is 24μV/°C, then, in view of the typical 6.1μV/°C/μA sensitivity to drain current, a 4μA current unbalance should result in near-cancellation of drift . . . *if* the offset vs temperature curve is linear. (In fact, 3 different FET's, connected in the circuit of Figure 1, with initial drift rates of 50, 30, and 18μV/°C, turned up with 4.5, 2.5, and 1.5μV/°C when the *calculated* value of R_T required to furnish the current unbalance appropriate to each FET was used.)

This technique can obviously result in economies, since a user may purchase a less-tightly-selected FET, at considerably lower expense, and yet obtain premium performance, at the cost of obtaining initial drift data. In order to ensure that the FET's purchased by a user have adequate temperature-drift nonlinearity, (see Figure 4 for a qualitative comparison of essentially-linear monolithic TRAK-FET's and nonlinear hybrid

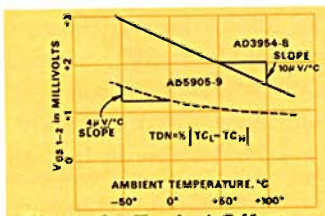


Figure 3. Typical Offset vs Temperature for Dual TRAK-FETS. Note Linearity (TDN's < 1μV/°C)

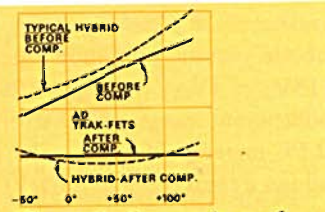


Figure 4. Comparison of Typical TRAK-FET's vs Hybrid FET's, With and Without Drift Compensation

*Analog Dialogue, Vol. 4, No. 2

†For complete technical data on Analog Devices' TRAK-FETs, use the reply card. Circle F18. For a more-detailed version of this design discussion, Circle F19

dual FET's) we define a *temperature-drift nonlinearity (TDN)* specification as follows:

$$TDN = \tfrac{1}{2} \mid TC_L - TC_H \mid$$

where TC_L is the average temperature coefficient from -55° to +25°C, and TC_H is the average temperature coefficient from +25° to +125°C. If it were possible precisely to null out the average temperature sensitivity over the entire range, the TDN would represent the remaining irreducible thermal drift. For nearly all grades of TRAK-FET's, the TDN specification is ±5μV/°C maximum, ±1μV/°C typical. *Maximum* TC is determined by the larger of TC_L or TC_H; *average* TC is one-half the sum of their magnitudes, with the polarity of the larger.

To enable the reader to grasp the full meaning of the TDN specification, the table indicates the limiting effect of the TDN specification on FET selection. The table lists a number of maximum TC's and TDN's for FET's that meet a ±50μV/°C specification. The units outlined in the unshaded area also meet a TDN specification of ±5μV/°C, and are therefore capable of being trimmed to within ±5μV/°C. To be sure of obtaining this kind of performance without the TDN specification, the user would have to specify the severely-restricted class of expensive units lying within the dashed lines.

TC_L or TC_H ↓	T_{CH} or T_{CL} → / PARAMETER	-50	-25	-10	-5	0	+5	+10	+25	+50
+50	TC	50	50	50	50	50	50	50	50	50
	TDN	50	37.5	30	27.5	25	22.5	20	12.5	0
+40	TC	50	40	40	40	40	40	40	40	50
	TDN	45	32.5	25	22.5	20	17.5	15	7.5	5
+30	TC	50	30	30	30	30	30	30	30	50
	TDN	40	27.5	20	17.5	15	12.5	10	2.5	10
+20	TC	50	25	20	20	20	20	20	25	50
	TDN	35	22.5	15	12.5	10	7.5	5	2.5	15
+10	TC	50	25	10	10	10	10	10	25	50
	TDN	30	17.5	10	7.5	5	2.5	0	7.5	20
+5	TC	50	25	10	5	5	5	10	25	50
	TDN	27.5	15	7.5	5	2.5	0	2.5	10	22.5
0	TC	50	25	10	5	0	5	10	25	50
	TDN	25	12.5	5	2.5	0	2.5	5	12.5	25
-5	TC	50	25	10	5	5	5	10	25	50
	TDN	22.5	10	2.5	0	2.5	5	7.5	15	27.5
-10	TC	50	25	10	10	10	10	10	25	50
	TDN	20	7.5	0	2.5	5	7.5	10	17.5	30
-20	TC	50	25	20	20	20	20	20	25	50
	TDN	15	2.5	5	7.5	10	12.5	15	22.5	35
-30	TC	50	30	30	30	30	30	30	30	50
	TDN	10	2.5	10	12.5	15	17.5	20	27.5	40
-40	TC	50	40	40	40	40	40	40	40	50
	TDN	5	7.5	15	17.5	20	22.5	25	32.5	45
-50	TC	50	50	50	50	50	50	50	50	50
	TDN	0	12.5	20	22.5	25	27.5	30	37.5	50

For the circuit of Figure 1, total drain current of 400μA is maintained constant by the current source, Q1, Q2. Since the op amp maintains the drains at very nearly equal voltage, the distribution of current between the two FET's depends on the resistances R_2 and $R_3 + R_T$. The 20kΩ value was chosen to obtain input common-mode swing of +5V minimum ($15V_S - 4V_{GS} - 2V_{DS} - 200\mu A \times 20k\Omega$). R_T allows a TC adjustment range of ±2.5%I_D, or about ±30μV/°C. Since a 2.5% increase of I_{D1} results in a 2.5% decrease in I_{D2}, this allows a total range of ±60μV/°C.

Adjust R1 for zero offset at 25°C, measure $\Delta V_{OS}/\Delta T$ over the desired temperature range, set R_T to the appropriate value, readjust R1 at room temperature, and confirm by measurement that the drift is within the predicted range.

EBR Uses 16-Bit DAC

4096 SCAN LINES WITH 5% SPACING-ERROR ALLOWS HIGH-RESOLUTION, HIGH-SPEED ELECTRON-BEAM RECORDINGS ON FILM

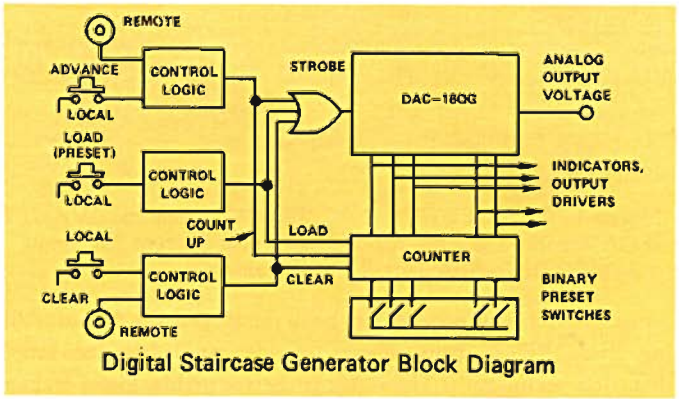
At CBS Laboratories, high-resolution electron-beam recording is accomplished by directing a controlled stream of electrons at a sensitive film in a vacuum. The electron beam is scanned horizontally, with stepwise vertical displacement of successive sweeps, and intensity modulation of the beam. The result is a latent image on film, which is subsequently developed. Thus, in this application, the EBR operates in much the same manner as the familiar TV raster, except that, in a typical system, there are 4,096 lines, with 8,192 data points/line, and 128 distinct "gray" levels. The image is formed on 70mm film with, typically, 2-micron line widths and 4μ interlinear spacing.

Since the developed film may be examined quite closely, and with considerable magnification, the spacing of the lines must be maintained within quite close tolerances, to avoid "gaps" and "banding," and to facilitate interpolation. A typical specification for line spacing tolerance is within ±5%.

The maximum tolerable vertical error is thus ±5% of 1/4096, or 1/82,000. If the vertical line-spacing is generated digitally, a 16-bit DAC with ±½LSB nonlinearity would have a maximum linearity error of 1/131,072, which is quite adequate. (½LSB of 15 bits would be 1/65,536, which is inadequate, and an ordinary "12-bit" converter, which might be implied by 4,096 lines, is out of the question.) Translated into actual voltage, for a ±5V range, the maximum allowable error is ±122μV.

The vertical scan is a 4,096-step voltage staircase, generated by a counter and the 12-most-significant bits of a DAC-16QG.* (For some projects, more steps are used, with tighter line-to-line spacing.) The counter may be advanced either manually (for test) or by a digital clock pulse; it may be cleared either manually or automatically; it may be preset to a desired initial value by a set of manual switches. The analog output scale factor and position are both adjustable.

The typical frame time is 2 minutes: 300kHz horizontal information recording rate, and 30ms dwell time per vertical step.



Digital Staircase Generator Block Diagram

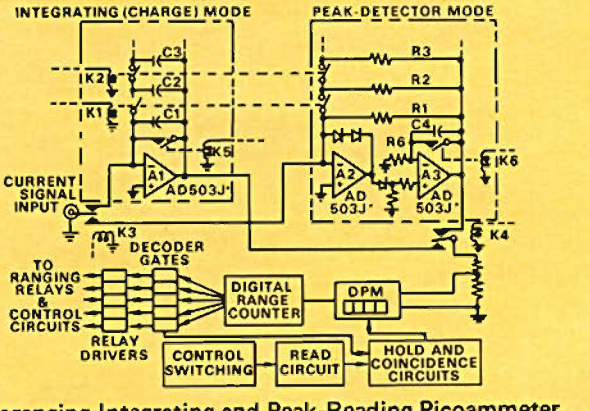
Our thanks for this Application Note go to Marvin H. Gold, Senior Electronic Engineer at CBS Laboratories, Stamford, Connecticut.

*For information on Model DAC-16QG, use the reply card. Circle F8

Two Low-Current Integrators with Digital Readout

AUTO-RANGING PICOAMMETER INTEGRATES OR READS PEAKS

EG & G has developed an auto-ranging picoammeter that responds to full-scale current ranges from 1nA (±3%) and 10nA (±2%) to 10μA (±1%) and provides a digital readout of either the peak input or the average input over a predetermined integrating period. The device was designed for thermoluminescent dosimetry (TLD), and provides a direct digital readout, in physical units, of average or peak dosage for full-scale ranges from 19.99 milliroentgens to 199.9R. In thermoluminescent dosimetry, exposure to nuclear radiation is measured by heating the material that has been exposed, and reading out the resulting light energy given off via a photomultiplier. Though the instrument is designed for this specialized application, the technique – and the instrument – is applicable to a variety of other measurements involving an input current.



Autoranging Integrating and Peak-Reading Picoammeter, EG & G Model 2025A – Block Diagram

Input current is routed to either the integrator or the peak-follower. The scaled output is applied to the digital panel meter. If the output exceeds a prescribed range, the DPM overrange signal increments a counter and decoder-driver, which switches to the next-lower range and shifts the decimal point.

Range switching is accomplished by adding feedback capacitance (in the integrator) or conductance (in the peak-follower) in parallel with the existing admittance, in the ratio 1, 9, 90, . . . (e.g., 1 + 9 + 90 = 100), without interrupting the computation.

After computation, the instrument is switched to *read*, and the result is held indefinitely by the DPM, unaffected by input changes or drift in the analog circuitry. In *reset*, the capacitors are discharged, in readiness for the next computing cycle. In the peak-follower, the feedback current, $-e_{out}/R_1$, etc., is compared with the input current in A2. If it is insufficient, C4 is caused to charge to the proper value. If it is sufficient, or excessive, C4 retains its charge until the next peak or *reset*.

We are indebted to Robert A. Capobianco, of EG & G Electro-Optics Division, Salem, Mass., for the description of his instrument's design.

*For information on the AD503 FET-input IC op amps or the AD2001 DPM, use the reply card. Circle F20 for the AD503, F21 for the AD2001

MEASURING X-RAY DOSAGE WITH AN INTEGRATOR

In an instrument developed at the University of California's San Francisco Medical Center, a parallel-plate ionization chamber produces a current as low as 10^{-13}A, which is integrated to obtain real-time measurement of total radiation dosage during radiotherapy procedures. Readout is on a digital panel meter, and a comparator compares the actual dosage with a preset dosage level, turning off the radiation when they have become equal. Because the dosage rate can fluctuate, integration provides a more-accurate measurement of the total dosage actually encountered.

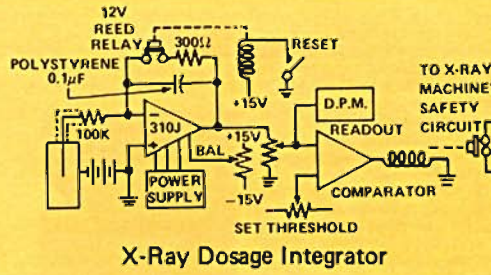
Detector. A parallel-plate ionization chamber with thin aluminum-plate electrodes, was used in this design, with 300V of biasing voltage. For future designs, several diodes, connected in series, appear to be a promising substitute, eliminating both the hermeticity problem and the bias voltage, without substantially affecting the efficacy of measurement.

Amplifier. The Model 310J* parametric operational amplifier was used because of its low leakage-current specification of 10fA (10^{-14}A) and its low voltage drift and high input impedance.

Capacitor. The capacitor is potentially the limiting factor on integration accuracy. A device having high insulation-leakage resistance (typically 10^{12} ohms) and low dielectric hysteresis (< 0.1%) is desirable. Polystyrene, teflon, and polycarbonate are the best dielectrics for this purpose.

Wiring practice. At sub-picoampere levels, shielding, guarding, and rigid wiring are essential, because insulation alone is inadequate to minimize circuit leakage and pickup. (See "The World of fA," in *Dialogue*, Volume 5, No. 2).

Comparator. For the original design, a digital comparator was used, with thumbwheel switches providing the threshold setting for the logic circuitry to compare the DPM output with the preset value. An analog comparator (such as the AD351) could also be used at the integrator output, with a 10-turn potentiometer or resistive decade-switching providing the reference.



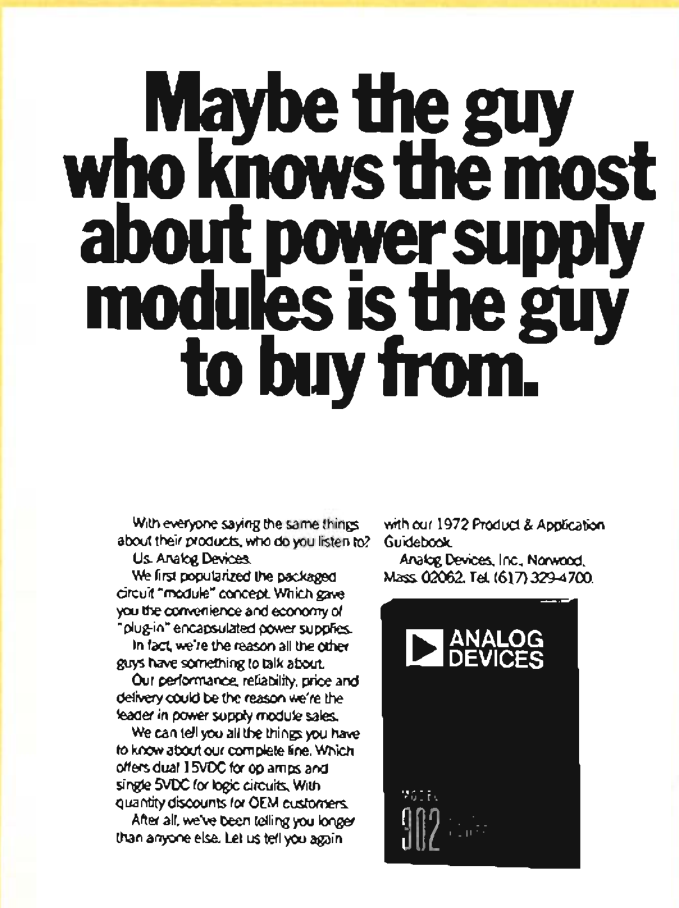
X-Ray Dosage Integrator

We are grateful for information supplied by Rod McDougall, Hospital Radiation Physicist at the San Francisco Medical Center, in the form of a paper (with R.H. Rydman, Ph.D.) "A Digital Integrator for X-Ray Machines."

*For information on the 310J and the AD351 comparator, use the reply card. Circle F22

For more information on FET-input IC Op Amps, Circle F20

For more information on 1µV/°C Monolithic Op Amps, Circle F14



For more information on Modular Power Supplies, Circle F23

For more information on the AD2001 DPM, Circle F21