ANALOG DIALOGUE

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete.

**MONOLITHIC OP AMP
HAS 130V/μs SLEWING RATE**
See Page 3

Contents: Volume 5, Number 4

ANALOG DEVICES
Circuit Specialists

Editor's Notes

ON PRECISE EXPOSITION

Engineers and editors of technical publications alike are impressed by equipment specifications that record great fidelity to ideal performance. For example, "16-bit" converters are currently a topic of great interest, because of their ability to resolve 1 part in 2^{16} (1/65,536). It is curious, however, that precision in writing has had difficulty in surpassing the 1-bit level. That is, if there are two choices (e.g., between "linearity" and "nonlinearity," between "accuracy" and "error"), all too often the wrong choice will appear in print. That none is immune (perhaps because of a "Gresham's Law" that might read "Bad terminology drives good terminology out of circulation"), is underscored by the following communication we recently received from reader van Zee, of the University of Washington:

"Taken literally, a statement on p.9 (*Dialogue*, Vol. 5 No. 2) says that the Y-input 'linearity' of 0.15%, compared to 0.25% is an advantage if one wants 'linearity' as low as possible. But who wants such low *linearity*? Most people want linear response from an MDSSR* with as low a *nonlinearity* as possible."

Our reaction was: Hurrah for reader van Zee! At last we have heard from someone who cares about the logical relationship between magnitude of an error (nonlinearity) and its comparison as such rather than its opposite (linearity). The only excuse (and a frail reed it is) that has any validity is the plea of purposeful omission instead of sloppiness — that when we say "linearity of 0.15%," we mean "linearity *error* of 0.15%," to save paper, ink, and time. We understand it, the reader understands it, so why make a mountain out of a molehill?

Why indeed! Because it brings us one step closer to a frame of mind that accepts Orwell's "Newspeak" ("War is Peace," "Slavery is Freedom," etc.) — and 1984 is fast-approaching! Let us leave deliberate misuse of precise language to the political propagandists; in science and engineering, at least, we are taught to think quantitatively and to express ourselves with precision. Let us not abandon it in the name of either sloppiness, false economy, or because "everyone's doing it."

Examples of such misuse appear with discouraging frequency in the Engineering press. Here are a few examples, found in leafing casually through a few publications:

"This results in a linearity of 0.25 per cent of full scale" (*EDN-EEE*, May 15, 1971)

"Two-tone linearity over the frequency range is −30dB or better . . ." (*IEEE Journal of Solid-State Circuits*, June, 1971)

"Over a 15°C to 35°C temperature range, accuracy is ±0.1% of full scale, ±1 digit." (*Electronic Products*, May 17, 1971)

On the other hand, just to demonstrate that this aberration is not universal (hence "standard"), here is the right way:

"The linearity error of the time/voltage relationship is less than ±0.05 percent for a voltage variation from 0.5 to 14V" (*IEEE Trans. Instrumentation & Measurement*, May, 1971).

We doubt that our small voice will serve to still the tide of "standard usage" that will prevail in imposing the illogic of using "nonlinearity" in place of "linearity," "accuracy" instead of "error," etc. It is unlikely that even our own publications will ever achieve beneficial consistency. However, with the hope that "someone is listening," we invite you to join a movement to restore "1-bit accuracy" by achieving clear expression in few words without falling into logical traps:

NOT	BUT
Linearity is 0.1%	Linearity error is 0.1%, or Nonlinearity is 0.1%
Full-scale accuracy: ±1%	Errors:
Linearity: ±0.5%	Full scale: ±1%
	Linearity: ±0.5%
	Scale factor error: ±1%
	Nonlinearity: ±0.5%
	Linear to within: ±0.5%

It is our hope that, if you have stayed with us to this point, we have succeeded in planting that little nagging doubt that will cause you to become conscious of the use of words that say the opposite of what they mean, and to balk at using the wrong one. You will thus be doing your part in establishing a mini-revolution that will help to delay the approach of the worlds of Orwell and Kafka. ▶▶▶

AN INVITATION TO INCREASE THE LOOP GAIN

We develop and produce modular and IC op amps and conversion products for you to use as high-precision links in instruments, equipment, or systems, at lower cost than if you had built them yourselves. Our devices tend to be *general*, rather than *specific*, in their uses. Thus, new applications —as well as new devices—continually appear, modes of behavior thought unimportant catch the spotlight, and new groups of users need to know what the specifications and terms mean to them. *Analog Dialogue* seeks to grasp this changing picture and provide what today's readers (i.e., *you*) need to know.

BUT — *we also* need to know something that only *you* can tell us. We need to know how well we are satisfying your needs. Are we telling you what you want to know? What are we missing? Do we strike a proper balance between information and interpretation? What would you like us to tell you more about? What would you like to see *less* of? We try to read your mind by every possible indirect means (short of witchery), but we'd much rather you told us directly. With more gain in the loop, perhaps we can strike a truer course (if we can avoid oscillation). "So keep those cards and letters coming, folks!" ▶▶▶

Dan Sheingold

*MDSSR: Multiplier-Divider-Squarer-Square Rooter

Stable Monolithic Op Amp Slews at 130V/μs

by Heinrich Krabbe and Richard S. Burwen

The AD505* is a monolithic IC operational amplifier designed primarily to offer high speed in inverting applications. It is characterized by slew rate of 130V/μs, full-power bandwidth of 2MHz, and open-loop gain of 300 at 1 MHz. It obtains this excellent dynamic performance without sacrificing either stability or low-frequency parameters; for example, the open-loop dc gain is typically 500k (114dB), and the drift is about 10μV/°C (AD505K).
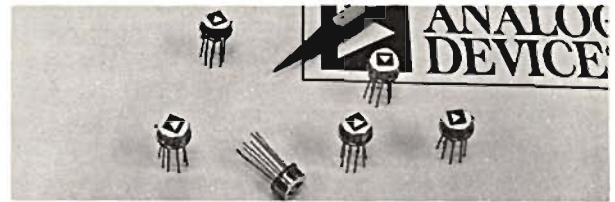
The amplifier's high speed is obtained via a feedforward connection, which limits its range of applications to those calling for sign inversion. Nevertheless, it does have dc common-mode rejection of about 80dB up to 20Hz, which is a useful feature for processing differential signals having high-frequency content, in the presence of a dc common-mode level.

The amplifier is manufactured by a bipolar/thin-film process, which results in lower cost than that of high-speed amplifiers that use dielectric isolation. Typical applications include active filters, D-A converters, ac voltmeters, pulse amplifiers, pre-amplifiers for use with wideband IC multipliers (such as AD530[†]), and general-purpose ac amplifiers. It is packaged in the convenient 10-lead TO-100 hermetically-sealed can.

AMPLIFIER DESIGN

The AD505's circuit is shown schematically in Figure 1, while its basic circuit structure is depicted in the block diagram of Figure 2. The combination of high dc gain and high speed is obtained in a manner similar to that of chopper-stabilized amplifiers, in which the high-frequency gain and part of the dc gain are obtained in a common main amplifier stage, while additional dc gain is obtained in a preamplifier stage having relatively-narrow bandwidth.

The open-loop small-signal characteristic of the amplifier is essentially that of an integrator, with unity gain occurring at about 5MHz. The amplifier is therefore stable for all normal values of loop gain. In addition, however, provision is made for shunting the integrator's input resistor to obtain wider band-width for higher values of closed-loop gain. For example, one may completely short-circuit the integrating resistor to obtain a stable gain of 10, using a 5kΩ:50kΩ resistor ratio, with 1.5MHz bandwidth (both small- and large-signal). Gain of 50 — without any reduction in bandwidth — can be obtained using a 1kΩ:50kΩ ratio.

The dc signal path is via the input differential current amplifier, Q1 and Q2 (which have a low bias-current/temperature coefficient, typically 0.2nA/°C), followed by gain stage Q6, Q7, and Q11. A 390pF (external) feedback capacitor from the emitter of Q11 makes this gain stage an integrator, and an additional 4700pF to ground provides a lag to ensure that this portion of the amplifier rolls off to below unity gain above the frequency at which the fast dc amplifier, Q12, Q13, starts its rolloff.

The ac signal is fed forward via an external 0.01μF capacitor to emitter-follower Q15, which drives the other differential input of the fast dc amplifier.

The output of the fast dc amplifier drives the complementary emitter-follower output stage, Q21, Q22, and also the internal feedback connection, via an internal 1.5pF capacitor, C1, which, with R1(20kΩ), provides the amplifier's overall 6dB/octave rolloff to unity gain at about 5MHz.

Q8, Q9, Q10, Q14 provide current sources for operating the gain stages, while Q3, Q4, Q5, Q6, Q7, Q18, and Q19 form dynamic loads for these stages. Diodes Q16 and Q17 provide appropriate biasing for the class AB output stage, which is notably free from crossover distortion.

A 180-ohm resistor in series with the output terminal of the amplifier serves for stabilization against small capacitive loading (to typically 50pF).

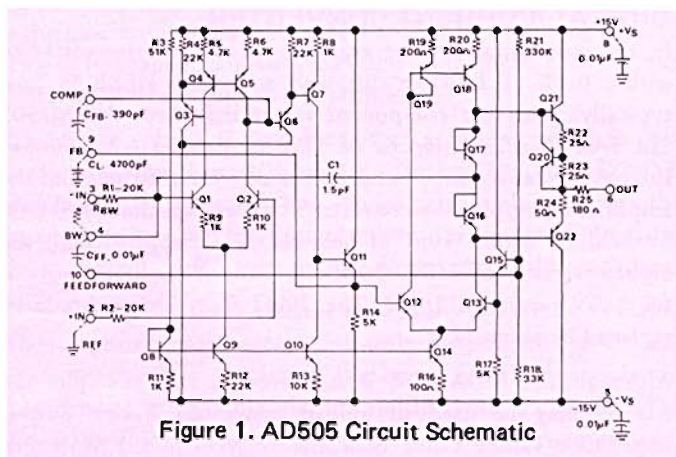A photomicrograph of the complete AD505 chip is shown in Figure 6 on page 5.

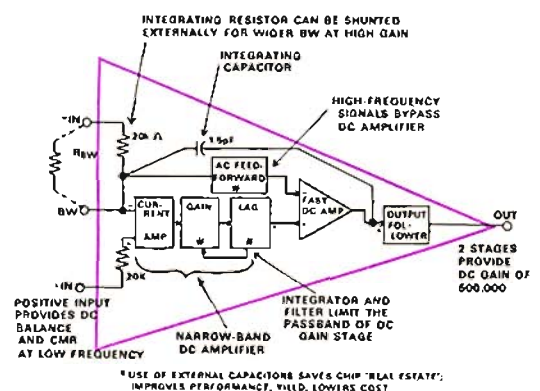Figure 1. AD505 Circuit Schematic

Figure 2. AD505 Block Diagram

3

DYNAMIC CHARACTERISTICS

Like the modular type 120, the AD505 is designed to have a stable 6dB/octave rolloff for normal applications with the loop tightly closed, yet remain capable of being externally connected for as much as 35dB of additional closed-loop gain at high frequencies without suffering decreased small- or large-signal bandwidth, or increased settling time.
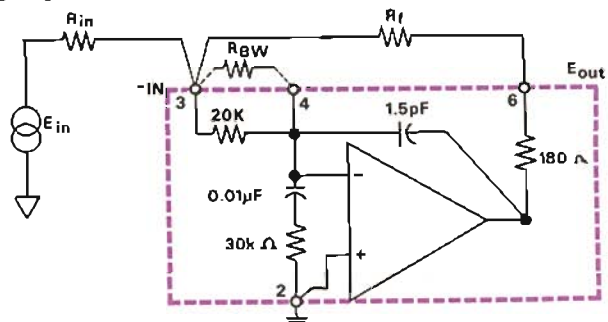

Figure 3. Approximate equivalent circuit of the AD505 at high frequencies

Figure 3 shows an approximate high-frequency equivalent circuit of the AD505. With no external R_{BW} resistor, the amplifier can be seen to be an integrator with $20k\Omega$ input resistance. The open-loop gain as a function of frequency is shown as Case $R_{BW} = \infty$ in Figure 4. If R_{BW} is zero, (i.e., the $20k\Omega$ resistor is shorted out) the open-loop gain is increased, as shown. In addition, the input impedance at high frequencies can be represented by, in effect, a 500Ω resistor to common (the "Miller" impedance of the 1.5pF capacitor*). Paradoxically, this permits the amplifier to be stable (for large enough feedback resistance) even at low values of signal gain, and permits gain to be adjustable by a single resistor, without necessitating changes in R_{BW}.
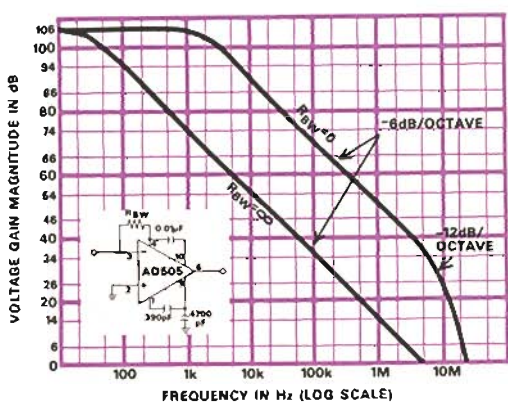

Figure 4. Open-loop gain magnitude vs frequency at extreme values of R_{BW}

In order to make the AD505 truly economical and obtain high yields (and low cost), a number of capacitors (that one finds normally in modular types) are designed to be connected externally. As with modular types, they are fixed values to meet design goals. The design allows quite reasonable tolerances (but *not* additional degrees of freedom). In effect, the user can obtain performance available normally in modular types (at much higher cost), in the form of a low-cost IC-plus-capacitors. Several compensation circuits for differing conditions are shown in Figure 5.

$$\cdot Z_{in} \cong \frac{X_c(\omega)}{G(\omega)} = \frac{f}{2\pi f c \times 300 \times 10^6} = \frac{10^{12}}{1.88 \times 10^9} \cong 500\Omega$$

4

A summary of the AD505's performance characteristics is given in the table on the facing page.
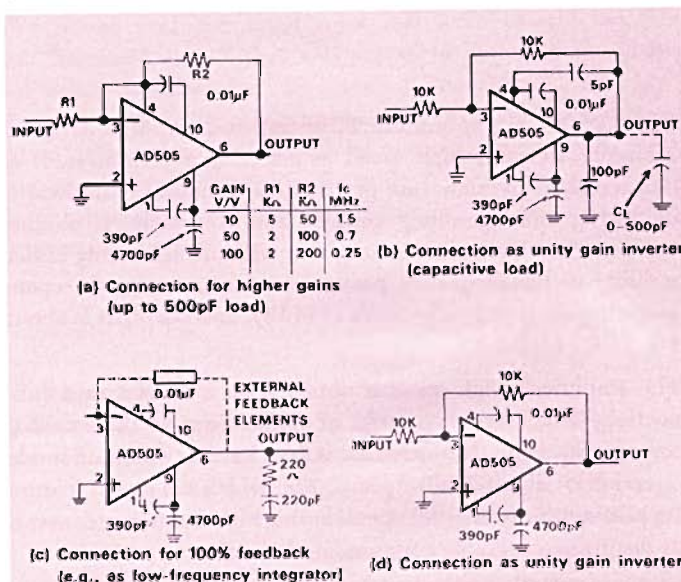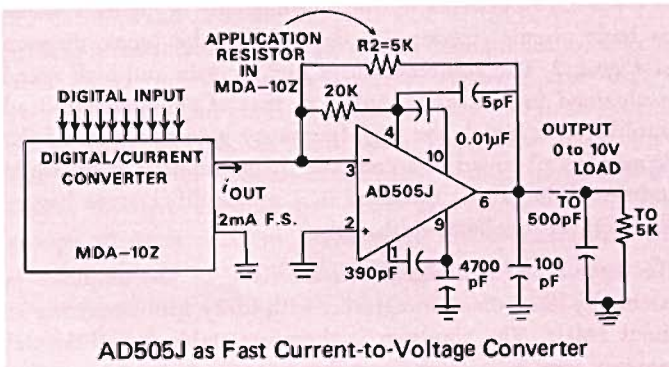

Figure 5. Compensation Connections of AD505 for various conditions of feedback. Not shown are power supply connections, with 0.01µF from amplifier's terminals to ground. Terminal 2 may be connected to a zeroing potentiometer instead of ground
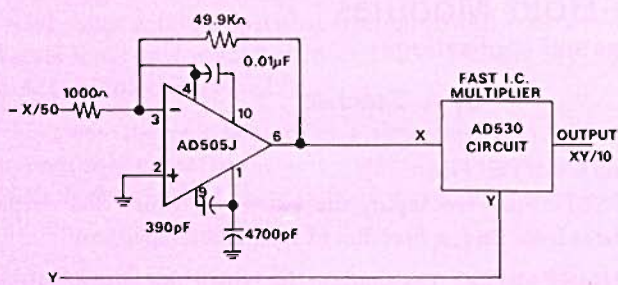
TYPICAL APPLICATIONS

AD505J as Fast Current-to-Voltage Converter

FAST OUTPUT BUFFER FOR DIGITAL/CURRENT CONVERTER

In this configuration, the converter and amplifier settle to within 0.1% (1 LSB) in 3µs, and to within ½LSB in 5µs, typically. With the component values indicated, the AD505 can feed load impedances of 5kΩ in parallel with 500pF. Interwiring capacitance between the converter output and the amplifier input, plus the converter's output capacitance, should be held to within 10pF if possible. When applied with the *bipolar* version of MDA–10Z, the built-in feedback resistor for ±10V output is 10kΩ. The 20kΩ R_{BW} shunt should be replaced by about 5kΩ.

Although the MDA–10Z is indicated in this example, the AD505 may be used to unload converters having output impedance values other than the MDA–10Z's 1.5kΩ. For example, when used with a 10-bit converter assembled from µDAC switches and resistor networks, the external R_{BW} shunt may be omitted and a 7.5kΩ load connected from the summing point to ground.

Preamplifier For Fast I.C. Multiplier

PREAMPLIFIER FOR FAST IC MULTIPLIER

Multipliers often provide their best accuracy when both inputs and output can swing through the full-scale range. One of the problems in taking advantage of the excellent high-frequency capabilities of the AD530 Multiplier-Divider is simply finding a low-cost integrated-circuit amplifier capable of driving it with ±10V at frequencies up to 1 MHz. The AD505J makes an excellent preamplifier for this purpose; it is shown above connected for gain of 50, and applied to one of the AD530 inputs. Either or both input signals can be preamplified in this manner.

In this circuit, the internal 20kΩ resistor has been shorted out for maximum bandwidth. The frequency for −3dB response in this configuration is typically 1.6MHz, with full output capability.
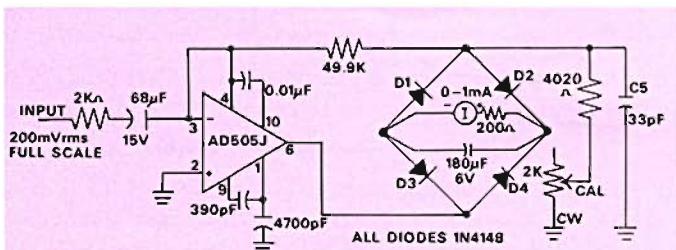
Wideband Average-Reading AC Voltmeter

WIDEBAND AVERAGE-READING AC VOLTMETER

This simple ac voltmeter circuit provides accuracy to within 1% at 200mV full-scale input, from 10Hz to 200kHz. Higher values of input voltage may be handled by switching-in additional resistance in series with the 2kΩ input resistor, and reducing the capacitor size in proportion.

The input voltage is transduced into a current, which is constrained to flow through the meter via either D1–D4, or D2–D3, depending on polarity. The diodes serve only to route the current, and the meter responds only to current, hence linearity is preserved, independently of diode threshold variations.

The 49.9kΩ feedback resistor serves three functions: It makes the amplifier operate near full-scale output voltage at full-scale input, thus protecting the meter from being violently overdriven; it presents the amplifier with a more-or-less linear feedback circuit having easier-to-handle dynamics; and, with the resistance to ground in the calibration circuit, it forms a current divider which provides current gain of 10:1. The potentiometer is adjusted to compensate for meter and resistor tolerances.

BRIEF SPECIFICATIONS

Typical at 25°C and V_s = ±15V, unless otherwise noted

Parameter	AD505J	AD505K
Input Offset Voltage ($R_s \leqslant 10k\Omega$)		
Initial, mV: typ; max	3.0; 7.5	2.0; 5.0
Drift vs Temp. $\mu V/°C$	25	10
Input Bias Current		
Initial, nA: typ; max	50; 200	50; 100
Drift vs Temp. nA/°C	0.2	0.15
Wideband Noise μV rms,		
10Hz to 1 MHz	20	20
Input Resistance		
dc, megohms	2	2
f > 10Hz, kΩ	20	20
f > 30kHz(R_{BW} = 0), ohms	500	500
Voltage Gain, V/mV, typ; min	500; 50	500; 200
Output Voltage Swing		
(I_L = 5mA), min	±10V	±10V
Short-circuit Current, mA	25	25
Gain Magnitude @ 1 MHz, V/V		
R_{BW} = ∞	5	5
R_{BW} (External) = 20kΩ	11	11
R_{BW} = 0	300	300
Full-power Bandwidth,		
(R_L = 10kΩ), MHz	2	2
Slew Rate, (R_L = 10kΩ), V/μs	130	130
Settling Time, $R_L = R_f = R_s$ = 10kΩ,		
μs From Initiation of 10V Step Input		
to 10mV	2	2
to 100mV	0.5	0.5
Power Supply Current, mA, typ; max	5; 8	5; 8
Power Supply Rejection, dB	80	80

TYPICAL RESPONSE ($R_f = R_L$ = 10kΩ)

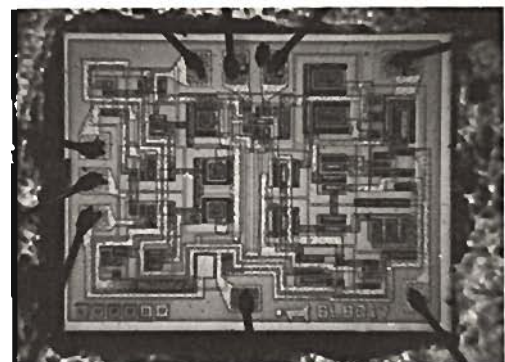| Gain (R_f/R_s) | R_{BW} = 0 | | R_{BW} = ∞ | |
	Slew Rate V/μs	Settling Time (to 10mV) μs	Rise Time (10-90%) ns	Settling Time (to 10mV) μs
1	–	–	70	2
2	–	–	70	2
5	–	–	400	3
10	130	3	800	3
100	130	4	6000	18

▶▶▶

Figure 6. AD505 Chip Photomicrograph

THE AUTHORS

Heinrich "Hank" Krabbe is Director of Engineering at Analog Devices. Dick Burwen, one of the founders of Analog, is a Consulting Engineer. For further information, see *Dialogue*, Vol. 5, No. 1, and Vol. 5, No. 2.

Understanding Sample-Hold Modules
a guide to their specifications and application

by A. Sanchez

A Sample-Hold module is a device having a signal input, an output, and a control input. It has two steady-state operating modes: *Sample,* (or "Track") in which it acquires the input signal as rapidly as possible and tracks it faithfully until commanded to *Hold,* at which time it retains the last value of input signal that it had at the time the control signal called for a mode change. Sample-Holds are often more-appropriately known as "Track-Holds" if they spend the major portion of the time in *sample,* tracking the input.

Sample-Holds usually have unity gain and are non-inverting. The control inputs are operated by "standard" logic levels, and are usually TTL-compatible. Logic "1" is usually the *Sample* command and logic "0" the *Hold* command.

Figure 1. Typical Sample-Hold Waveforms
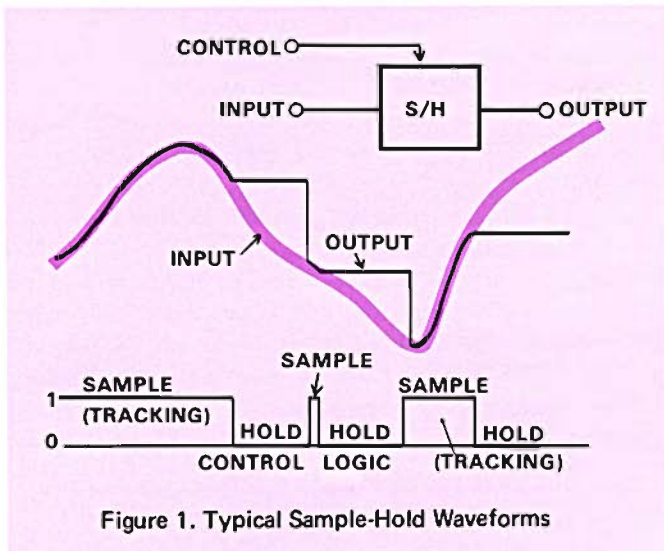
USES OF SAMPLE-HOLDS

In data-acquisition systems, Sample-Holds are used either to "freeze" fast-moving signals during conversion or to store multiplexer outputs while the signal is being converted and the multiplexer is seeking the next signal to be converted. In analog data-reduction, they may be used to determine peaks or valleys, establish amplitudes in resolver-to-digital conversion, and facilitate analog computations involving signals obtained at different instants of time. In data-distribution systems, Sample-holds are used for holding converted data between updates. Fast Sample-Holds may be used to acquire and measure fast pulses of arbitrary timing and width.

CHARACTERISTICS OF REAL SAMPLE-HOLDS

In the ideal Sample-Hold of Figure 1, tracking is error-free, acquisition and release occur instantaneously, settling times are zero, and hold is infinite. Commercially-available units* are specified in terms of the extent to which they depart from the ideal. Here are some of the commonly-occurring deviations (See also Figure 2):

*For data on Sample-Hold modules available from Analog Devices, use reply card. Circle D3
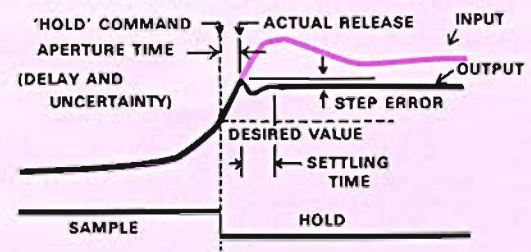
During SAMPLE (Figure 2a):

OFFSET: For zero input, the extent to which the output deviates from zero, a function of time and temperature

NONLINEARITY: The amount by which the plot of output vs input deviates from a "best straight line"
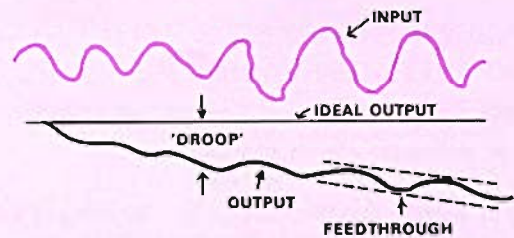
SCALE FACTOR ERROR: The amount by which the output deviates from specified gain (usually unity)
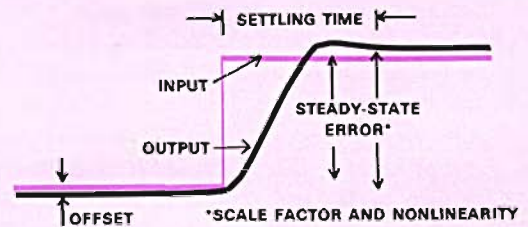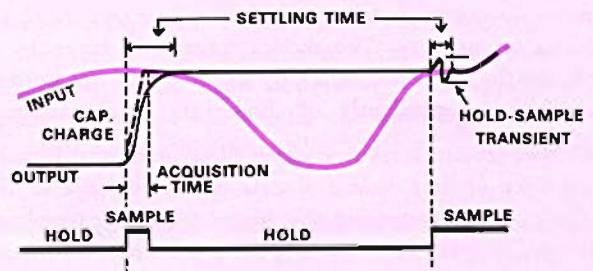

a. Tracking Errors During Sample

b. Sample-to-Hold Errors

c. Errors in Hold. Droop may be either Positive or Negative

d. Hold-to-Sample Errors

Figure 2. Sample-Hold Errors, Shown Qualitatively. Magnitude Scale is Greatly Exaggerated.

SETTLING TIME: The time required for the output to attain its final value within a specified fraction of full scale when a full-scale input step is applied (0 to ±FS or −FS to +FS). See also *Acquisition time* (Fig. 2d).

In this state, the unit behaves as a slow unity-gain follower. Thus one might expect to encounter other specifications typical of such devices, such as phase shift, slew rate, full-power bandwidth, small-signal bandwidth, etc.

SAMPLE to HOLD (Figure 2b):

APERTURE TIME: The time elapsing between the command to *Hold* and the actual opening of the *Hold* switch. It has two components: a nominal time delay, and an uncertainty caused by jitter or variation from time-to-time or unit-to-unit. If a signal changing at a rate of $1V/\mu s$ must be resolved to within 0.1% of 10V (FS), the aperture *uncertainty* must be less than 10ns, provided that it is possible to anticipate the nominal delay and advance the command by an appropriate interval. In some sampled-data system applications, such as spectrum analyzers, auto- and cross-correlation function generators, the delay is unimportant, but the uncertainty directly affects uniformity of the sampling rate. Manufacturers — to date — have not displayed consistency in their usage of *aperture time*; hence it is a good idea to find out exactly what the specification means for a unit you may be considering.*

SWITCHING TRANSIENTS: At the time the switch opens, the circuit may not be in equilibrium — especially if the signal is changing rapidly — because of amplifier delay error, etc. This will cause transients at the time the switch opens.

SETTLING TIME: The interval required for the output to attain its final value within a specified fraction of full scale, following the opening of the switch.

SAMPLE-TO-HOLD OFFSET: A step error occurring at the initiation of the *Hold* mode caused by "dumping" of charge into the storage capacitor via the capacitance between the control circuit and the capacitor side of the switch (e.g., the gate-to-drain capacitance of a field-effect transistor). It can be partially compensated by coupling an out-of-phase signal through a compensating capacitor, but usually only under a given set of tightly-controlled and highly-"tweaked" conditions. This offset does not occur in units having digital *Hold*.

During HOLD (Figure 2c):

"DROOP:" A drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor. ($dV/dt = I/C$) The current is the sum of the leakage across the switch, the amplifier's bias current, and leakage to the power supplies and to ground. In a well-designed unit, only the first is of any consequence. Units having digital storage have no droop. A rough figure-of-merit for analog Sample-holds is the ratio of droop time to settling time for the same percentage (FS) error. For example, a unit having settling time of $5\mu s$ to 0.01% and droop rate of 50mV/s (0.02s to 1mV), would have a figure-of-merit of 20,000/5 = 4,000.

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*The inconsistency in the industry extends even to the spelling. However, there seems little question that *aperture*, which is derived from the Latin *apertura* (from *apertus*, open) is the correct spelling, preferable to *aperature*, which cannot be found in most dictionaries.

FEEDTHROUGH: The fraction of input signal that appears at the output in *Hold*, caused primarily by capacitance across the switch. Usually measured by applying a full-scale sinusoidal input at a fixed frequency (e.g., 20Vp-p at 10 kHz), and observing the output.

DIELECTRIC ABSORPTION: The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. Less than 0.01% for good polystyrene and teflon capacitors, as large as several percent for ceramic and mylar capacitors.

Output impedance of the Sample-Hold should be low and recovery fast to minimize transients caused by dynamic loads, such as A/D converter inputs.

HOLD to SAMPLE (Figure 2d):

ACQUISITION TIME: The time duration for which an input must be applied for sampling to the desired accuracy. Essentially the same as *Settling time* for feedback types, but shorter than *Settling time* for two-stage units and for open-loop follower types in which the amplifier's settling time is appreciable compared to the capacitor's charging time.

HOLD-TO-SAMPLE TRANSIENTS: Transients (e.g. spikes) occurring between the *Sample* command and final settling. Not too important for large changes, but can be crucially important in some applications if the spikes are large compared to the actual change (e.g., at constant input). Such "glitch"-like spikes may be due to limiting and other sources of dynamic disequilibria within the Sample-Hold circuit, or to capacitive feedthrough from the control signals.

TYPICAL DESIGNS

The choice of storage element divides Sample-holds into two major classes. The more conventional, popular, and the lower in cost employs a capacitor for storage (*analog* storage); several forms of this design will be discussed here. The other technique, which uses an A/D converter and a register for storage, and reads out via a D/A converter, is somewhat more complex and costly (especially where high accuracy or fast sampling are necessary), but it has the undisputed advantage of arbitrary — and essentially "infinite" — *hold* time. Some ways of instrumenting that approach are discussed on page 15 of this issue.

Open-Loop Follower (Figures 3, 4, 5)

The most obvious circuit to come to mind is that shown in Figure 3. When the switch is closed, the capacitor charges exponentially to the input voltage, and the amplifier's output follows the capacitor's voltage. When the switch is opened, the charge remains on the capacitor. The capacitor's *acquisition time* depends on the series resistance and the current available to charge its capacitance. Once charge is acquired, to the appropriate accuracy, the switch may be opened, even though the amplifier has not yet settled, without affecting the final
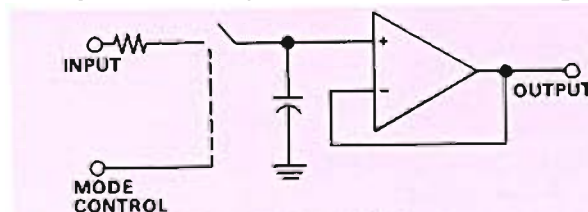

Figure 3. Simple Follower

output value or the settling time (assuming that the amplifier's input stage does not draw appreciable current at any time). The switch is typically a FET, and the amplifier is a FET-input type. This circuit has the disadvantage that the capacitor loads the input source, which — often enough — will either oscillate or lack sufficient current to charge the capacitor speedily. The circuit of Figure 4 includes a follower to isolate the source. The Analog Devices general-purpose SHA-1A uses this scheme.
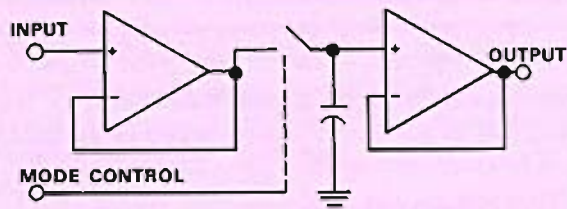
Figure 4. Same as Fig. 3 but with Isolated Input.*

For extremely fast charging at approximately a linear slew rate, a diode bridge scheme may be used, essentially as shown in Figure 5. Here, current sources are switched on to charge the capacitor. If the bridge and current sources are appropriately balanced, current flow into the capacitor will cease when the capacitor voltage is equal to the input voltage. Figure 5 is a simplified block diagram of the SHA-II, which has an acquisition time of 200ns to 0.1%, for a 10V step.
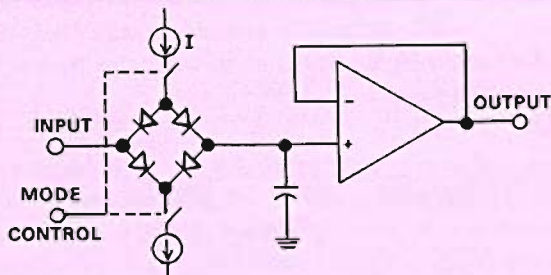

Figure 5. Switched Current Sources for Shorter Acquisition Time

Feedback Circuits (Figures 6 & 7)

The circuits of Figures 3, 4, 5 have the essential advantage of potentially fast acquisition and settling, but they are open-loop devices. If low-frequency tracking accuracy is more important than speed, the cascaded configuration of Figure 4 will be less satisfactory than a configuration which is, in effect, a single amplifier, yet provides isolation. This can be accomplished by closing the loop around a storage capacitor, and using high loop gain to enforce tracking accuracy. Figure 6 shows a
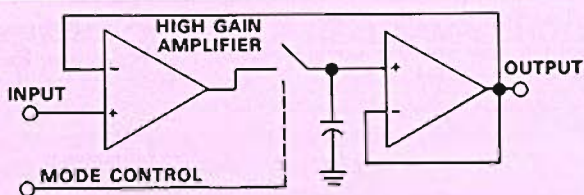

Figure 6. Track-hold Employing Feedback

*See Vol. 5, No. 2, P. 14, for a complete practical circuit, employing a FET switch and two AD503 FET-input IC op amps

configuration in which the input follower of Figure 4 is replaced by a high-gain difference amplifier. Now, when the switch is closed, the output (which represents the charge on the capacitor) is forced to track the input, within the gain and common-mode errors and the current-driving ability of the input amplifier.

Common-mode and offset errors in the output follower are automatically compensated for by adjusting the charge on the capacitor. When the switch is opened, the output retains the final value.

In Figure 7 (a simplified schematic of the SHA-IIA, SHA-3 and SHA-4), an integrator is used, permitting the switch to operate at ground potential.
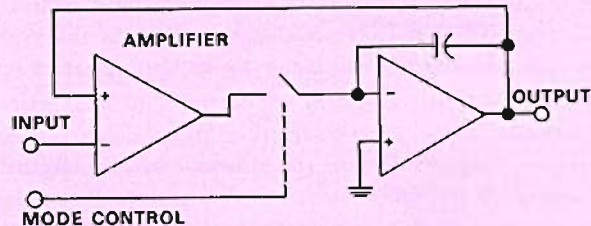

Figure 7. Feedback Track-Hold with an Integrator

In the circuits of both Figure 6 and Figure 7, because the charge on the capacitor is controlled by the output, as well as the input, the *acquisition time* and the *settling time* are identical. If the circuit of Figure 6 is switched into *hold* before the output has settled at the input value, the sample may be in error. Also, because the loop is open during *hold*, it must re-acquire the input when returned to *sample*, even if the input is unchanged. As a rule, this will result in a spike, if the input amplifier has high voltage gain.

Cascaded Sample-Holds (Figure 8)

If a long period of *hold* is required, in conjunction with very fast acquisition, a fast Sample-Hold, such as SHA-II, may be cascaded with one having slower acquisition but less droop. The resulting figure-of-merit can approach the product of the two.
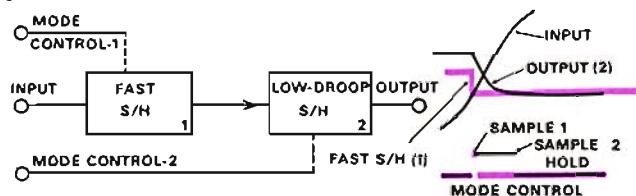

Figure 8. Use of Two Cascaded Sample-Holds for Fast Acquisition and Long Hold

APPLICATIONS

Sample-Holds are most-widely used in data acquisition systems, typically as shown in Figure 9. The Sample-Hold maintains the input to the A/D converter constant during the conversion interval; meanwhile, the multiplexer is seeking the next channel to be converted, either randomly or sequentially. As soon as conversion is completed, the Sample-Hold samples the newly-established input, and the cycle is repeated. This mode of operation is known as *synchronous* sampling: the Sample-Hold

operates in synchronism with the other system elements. If the input signals vary at widely disparate rates, programmed random access is necessary, to ensure that the signals with the most information are sampled most often. In another mode
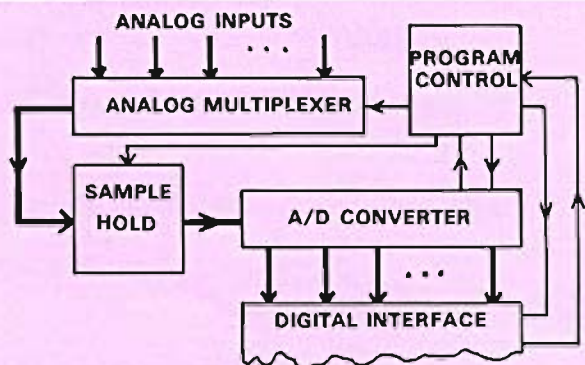

Figure 9. Typical Data-Acquisition System

(viz., *asynchronous*), a large number of Sample-Holds are used, to acquire and store data at rates pertinent to each individual channel. They are then either interrogated by analog multiplexers, or the signals are individually converted asynchronously, then multiplexed digitally, sometimes after preliminary digital processing.*

In data distribution, 0.01% Sample-Holds may be less costly than large numbers of D/A converters having comparable accuracy. A typical data distribution system is shown in Figure 10. A fast, accurate D/A converter updates a large
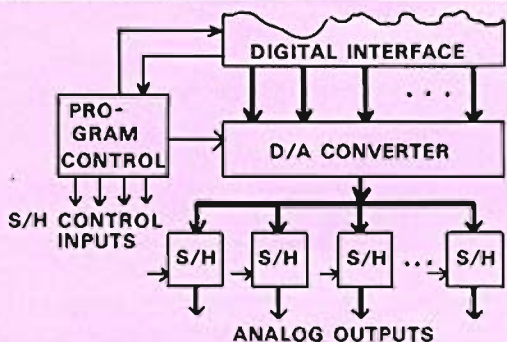

Figure 10. Data Distribution System with Analog Storage

number of Sample-Holds at speed and accuracy levels appropriate to the individual channels. Sample-Holds may be used to "de-glitch" D/A converters, in systems that are sensitive to spikes, by sampling their outputs after they've settled.

There are many applications in analog and hybrid computing and data-reduction. A typical example is shown in Figure 11: a peak follower, using a Sample-Hold and a comparator circuit. The Sample-Hold output (or the Comparator input) is biased by a few millivolts of hysteresis to avoid ambiguity during step inputs, and minimize false triggering by noise. Here's how the circuit works: When the input is greater than the S/H output, the comparator's positive output causes the S/H to track. When the input backs away and becomes less than the S/H output, the comparator's "0" output causes the S/H to *Hold* until the input once again becomes greater than the

---

*See the discussion of an adaptive low-redundancy data-acquisition system in *Dialogue*, Vol. 5, No. 1: "New Approaches to Data-Acquisition System Design," by Tage Anderson.

output. To reset, the control input is arbitrarily switched into *Sample,* and the lowest level contemplated is applied at the input.
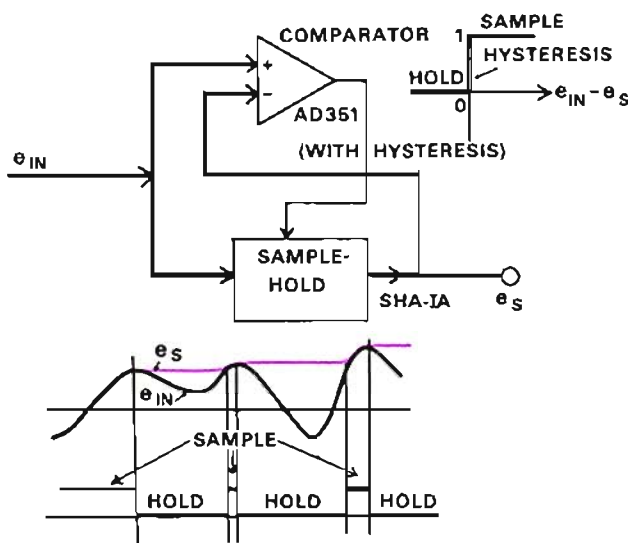

Figure 11. Peak-Follower using Sample-Hold and Comparator

The above are but a few examples of the wide applicability of these versatile modules. ▶▶▶
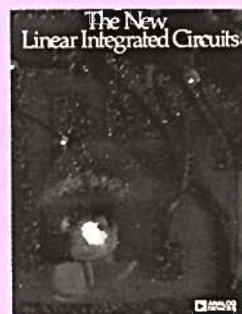
THE AUTHOR

Albert Sanchez, Manager of the Analog Product Engineering Group at Analog Devices has an M.S. degree from M.I.T., a B.E.E. from C.C.N.Y., and a comprehensive record of accomplishment at Litton and M.I.T. Instrumentation Laboratory in product design and project management in the areas of A/D and D/A devices and systems.

new products

## 12-Bit Analog-to-Digital Converter Has Ultra-Low Power Drain
IDEAL FOR OCEANOGRAPHIC AND OTHER ISOLATED APPLICATIONS
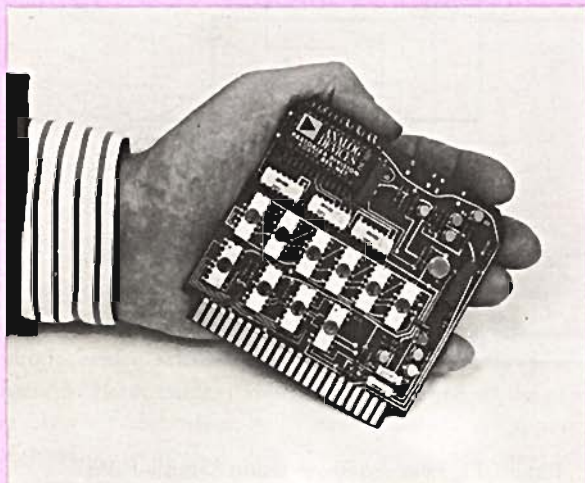
Analog's new Model ADC-12QL* is the *only* commercially-available A/D Converter optimized for data-collection for prolonged periods at remote and inaccessible locations. The reason is that a number of elements of its design were specifically tailored to meet the needs of such applications.

LOW POWER DRAIN
Perhaps most important, the unit was designed for submilliwatt standby power drain, or about 5 watt-hours per *year*. Until a conversion command is given, the power remains at this low standby level. When a conversion is ordered, the unit's circuits are turned on for the $85\mu s$ conversion interval, then returned to standby. During each conversion, an additional $75\mu W$ are drawn. Thus, if the converter is interrogated infrequently, the average power required is only a little more than standby. If the number of conversions is 8/s, then 2 X standby power is all that is needed. The graph below shows the required power for larger numbers of conversions-per-second. Besides applying circuit power only when needed for conversion, the actual power required is kept low by the use of C/MOS logic circuitry.

CURRENT DRAIN vs. CONVERSION RATE
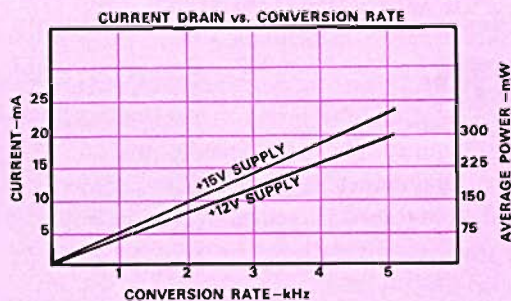
POWER SUPPLY INSENSITIVITY
The ADC-12QL is designed to operate from a single 12-15V power supply — for example, a 12.6V car battery. Though

FEATURES:
- **LOW POWER DRAIN**
  - Standby $< 600\mu W$ at 15V
  - Per Conversion/s $75\mu W$
  - At 100 Conversions/s 7.5mW
- **OPERATES FROM SINGLE 12-15V SUPPLY**
- **LOW P. S. SENSITIVITY** < 1 LSB/3V
- **PARALLEL AND SERIAL OUTPUTS**
- **C/MOS LOGIC:** Binary or Offset Binary
- **COMPACT:** Single Card Can Fit Inside 6" I.D. Cylinder

battery voltages can vary widely between charge and discharge, the conversion accuracy is affected by less than 1 LSB, over a range of 12-15V.

VERSATILITY
Using a single supply, the converter's output is C/MOS-compatible. However, if the logic is operated at +6V (either from a separate supply or tapped off the main supply), the output will work with external TTL logic inputs. Both parallel and series (RTZ) outputs are available, making the unit "at home" with either means of communication. Despite the use of a single supply, input-signal range options of ±10V, ±5V, +10V, and +5V are available. Bipolar options have offset binary coding.

12-BIT PERFORMANCE
Although resolution of 1:4096 is not always necessary, the kind of performance it represents assures reliable data, with errors less than 0.1% over the specified temperature range, an important feature because of the extremes of temperature in some remote applications. The Analog Devices "μDAC" IC conversion components ensure excellent linearity and temperature tracking. All active components are hermetically-sealed.

APPLICATIONS
The prime applications for the ADC-12QL occur in data-collection activities for prolonged periods at remote and inaccessible locations. Typical situations include ocean buoys, earth- and space probes, and radiation-monitoring devices. The ADC-12QL is also well-suited for use in portable medical and scientific instruments of high sensitivity, where the use of battery power can result in freedom from power-line-transmitted noise, as well as simplification of the common-mode noise problems that are so often the most difficult environmental problems faced in setting-up precision instrumentation. It makes feasible *digital* data transmission (with its greater inherent reliability) of signals from remote sources.

*For complete information on Model ADC-12QL, use reply card. **Circle D5**

10

Low-Cost D/A Converters

"THE BEST GENERAL-PURPOSE ECONOMY DAC IN THE INDUSTRY"
10-BIT UNITS HAVE IMPROVED TC, FASTER SETTLING TIME
COST ONLY $29 IN 100's

Models DAC-10Z and MDA-10Z* are the voltage- and current-output forms of new low-cost, high-performance 10-bit D/A Converters.

BACKGROUND

In 1970, Analog Devices pioneered the use of low-cost D/A Converters by OEM's, when the DAC-10H was introduced at $75. Its ready acceptance by the industry and more than a year of successful production experience have now led to the design of an improved model at a new low cost of only *$29 in 100's.*

IMPROVED PERFORMANCE

The DAC-10Z is nearly an order of magnitude faster than its predecessor, with settling time of 5μs to within 0.05% of full scale (10V), and it is twice as insensitive to temperature, with a gain temperature coefficient of only 30ppm/°C.

OTHER FEATURES

The DAC-10Z has voltage output of 0 to -10V for the unipolar option, ±10V for bipolar; the MDA-10Z has current output of 0 to 2mA unipolar and ±1mA bipolar. Unipolar coding is binary, and bipolar is offset binary. Both models are potted in the low-profile 2" x 2" x 0.4" modular package with pins on 1.8" dual in-line spacing. The MDA-10Z has 300ns settling time to within 0.05% for a full-scale current step, and — for faster voltage response than the DAC-10Z — can be used with such fast-settling op amps as the Model 46 (see adjacent column). Accuracy and linearity errors are within ±½LSB (0.05% of full scale), zero offset is negligible for unipolar models and within ±½LSB for bipolar units.

Logic is, of course, DTL–TTL-compatible and power supply required is a standard ±15V at only ±15mA (vs 25 and 20mA for DAC-10H and MDA-10H). For convenience, and improved gain tracking, the MDA-10Z includes a feedback resistor, appropriately scaled to provide -10V (unipolar) or ±10V full-scale output when used with an external operational amplifier.

APPLICATIONS

In addition to providing low-cost performance for large-scale data-distribution systems, their low cost and simplicity make these models ideal for use in do-it-yourself A/D converters, tracking-type sample-holds with arbitrarily-long *hold* duration (see page 15), and hybrid multipliers, in which the D/A converter is used with a low-cost analog multiplier to provide digitally-set adjustable gains. ▷▷▷

AVAILABLE SOON: 12-BIT PERFORMANCE AT LOW COST. WATCH FOR THE DAC–12QZ, ONLY $49 (100's).

*For further information on low-cost DAC's, use reply card. **Circle D6**

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new products

Ultra-Fast-Settling Op Amp

MODEL 46 SLEWS AT 1000V/μs, SETTLES TO WITHIN 0.1% IN 100ns, DEVELOPS ±100mA OUTPUT COSTS ONLY $62 IN 100's

FEATURES

Settling time to 0.01%	300ns
Slew rate	1000V/μs
Output current to ±10V	±100mA
Common-mode voltage	±10V
Common-mode rejection	4000

FET Inputs
Inverting or non-inverting operation

Analog Devices' Model 46*FET-input differential operational amplifier offers to the industry — for the first time — a unique combination of high slew rate, fast settling, and ±100mA output current. A novel design for the differential input stage achieves slewing rates of 1000V/μs, while simultaneously attaining settling times of 100ns to 0.1% and 300ns to 0.01% in the inverting mode, or 150ns to 0.05% in the unity-gain non-inverting mode. When operated non-inverting or differentially, the amplifier handles ±10V of common mode input.

In contrast with Model 46, competitive ultra-fast-response op amps offer *either* fast slewing rates *or* very short settling times . . . not both. Those approaching its performance do so at nearly double the cost. Consequently, the new Model 46 provides a valuable design solution for the many applications that require all-around rapid operation at a new low industry price.

SPECIFICATIONS

Besides the 1000V/μs slewing rate, ultra-fast settling (see above) and 4000 CMRR at ±10V common-mode input, Model 46 features a stable 6dB/octave rolloff and 40MHz minimum bandwidth, which ensure full performance and oscillation-free operation, even for 200pF load capacitance. Two versions of the basic Model 46 are available from stock, distinguished primarily on the basis of 75μV/°C voltage drift for Model 46J and 25μV/°C for Model 46K. Unit prices are $75 and $92, respectively, with Model 46J's price dropping to $62 in 100's.

APPLICATIONS

Besides the obvious application as an output amplifier for fast D/A converters, such as the 60ns MDAF, or even the MDA-10Z (adjacent column) the high speed and current capability suggest numerous others:

- **Stable Unity-Gain Buffer to 40MHz**
- **Sample-Hold Circuits**
- **A/D Buffer Amplifier**
- **Video Pulse Line Driver**
- **Ultra-Fast Current Source**
- **Deflection-Amplifier Driver** ▷▷▷

*For complete information on Model 46, use reply card. **Circle D7**

# new products

Active Filters Are Tunable

LOW-PASS UNITS SAVE MONEY, SIMPLIFY INVENTORY, ELIMINATE NEGOTIATIONS & DELIVERY DELAYS. BUTTERWORTH & BESSEL TYPES AVAILABLE. 4 OVERLAPPING BANDS COVER RANGE 0.1 Hz– 20kHz. UNIT PRICE $69, GENEROUS QUANTITY DISCOUNTS.

A problem that has long bothered both manufacturers and users of active filters has now been solved by the introduction of the 730 Series* of Tunable Active Filters.

The 730 Series consists of 4 ranges of 4-pole low pass designs with externally-adjustable cutoff frequencies. Any nominal cutoff frequency in a given range may be obtained by connecting or switching-in a set of 4 *identical* tuning resistors, chosen by the simple formula:

$$R(k\Omega) = 5 \left[\frac{f_c \,(max)}{f_c} - 1 \right]$$

Available with either Butterworth or Bessel responses, these models will meet their specifications over a 20:1 range of cutoff frequency adjustment. As shown in the response plots, the Butterworth characteristic is chosen for sharply-increasing attenuation in the vicinity of the cutoff frequency, while the Bessel characteristic is chosen for its linear phase shift and essentially-monotonic step response.
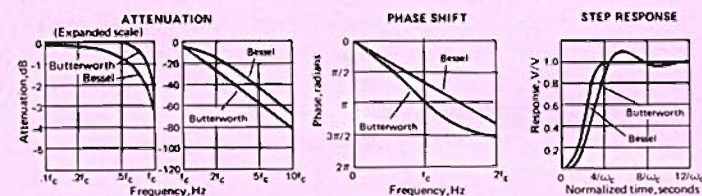
Idealized Low-Pass Response Curves

Because the Series 730 filters span the 0.1Hz to 20kHz cutoff range with only four different versions, customer logistics and inventory requirements are considerably reduced. Filters may be held in stock and adjusted, as required, to specific system frequencies, by *you*, thereby short-circuiting delivery delays that may occur when filters for special frequencies are ordered from the manufacturer. The upshot is a reduction in costly design delays and production inventory levels.

BRIEF SPECIFICATIONS

The Series 730 tuneable filters span the 1Hz– 20kHz cutoff frequency range in four overlapping bands: 1– 20Hz, 10– 200Hz, 100– 2000Hz, and 1k– 20kHz. Passband gain (Butterworth types) is held to unity within ±0.02dB (±0.2%) to 0.5f_c, typically, and the maximum output offset drift temperature coefficient is only 50µV/°C. If necessary, the user may extend the cutoff frequency range at the low end by 10:1 (200:1 overall) at the cost of proportionally-increased drift. The initial offset of 1 mV may be zeroed — as in an operational amplifier — by the use of an external potentiometer. Module size is

2.9" x 1.1" x 1", and the optional mating socket will serve for mounting of the tuning resistors in fixed-cutoff applications. For four equal resistors, the cutoff frequency will be within ±3% of the nominal value, and stable to 0.05%/°C. Noise is 75µVrms for the full-power 20kHz bandwidth.

APPLICATIONS

The Series 730 filters are a powerful design tool for data transmission, test instrumentation, and frequency analysis equipment, where signal fidelity and adjustable cutoff frequency are critical requirements. The filters are also useful in fixed-frequency applications, where cutoff frequency must be set to an empirically-determined "oddball" value at the time of system design. Finally, these filters may be used for system breadboarding to prove the efficacy of a given characteristic, after which fixed filters may be ordered in OEM quantity at low cost from the manufacturer (Analog). ▶▶▶

new literature

AD530 Application Brochure

The AD530* is the world's first complete-on-a-chip monolithic Multiplier-Divider-Squarer-Square Rooter (MDSSR). This 12-page booklet outlines its background and prospects, its circuit design, the connections for the various modes of operation, and a set of applications that go beyond the obvious functions implied by its name. We think you will find the brochure interesting and useful, and we invite you to send for it.

We asked Stan Harris, the "father" of this applications brochure, for a brief review of it. We had expected his response to be somewhat partisan, but we were totally unprepared for his stunningly hyperbolic description of its place in the firmament of human communication. Since the review is itself a unique document, we publish it here in its totality. (You may vote "in favor" by circling D18 or deplore it by circling D19.)

Since his first primitive cave drawings, evidences of man's efforts to document his existence have evolved from the cuneiform-and-clay of the Tigris and Euphrates Rivers and the hieroglyphics of the Egyptians, through the laboriously-etched Bible illuminations of the Mediaeval Monks and the first printing presses, into this era of xerography, electronically-controlled ink beams, and laser holography.

As one scans the immense spectrum of recorded knowledge, several works emerge as truly monumental efforts -- documents whose production has greatly affected and benefited the existence of Man.

Certain to be thus classified are the Dead Sea Scrolls, the Rosetta Stone, the Magna Carta, the Gutenberg Bible, the Declaration of Independence, the Emancipation Proclamation, and the 1968 Sears Roebuck Fall-and-Winter Catalog.

Another has joined this select group:

The culmination of many thousand manhours of toil by the finest scientific minds of Analog Devices, there is now available the *AD530 Complete Monolithic MDSSR Technical Bulletin*, 12 pages of definitive exposition of the history, theory, operation, and application of the World's Finest I.C. Multiplier -- the complete-on-a-chip AD530.

The AD530 MDSSR Bulletin is hot-off-the-high-speed presses. Its hieroglyphics are to the point, its cuneiforms concise, its illuminations the essence of clarity. Besides being a collectors' item, it will greatly aid your understanding and use of the AD530. Send for it.

▶▶▶

Application Brief

Fast-Recovery AC Coupling and Galvo Driver

TYPICAL CIRCUIT TECHNIQUES THAT CAN BE USED WITH OUTPUTS FROM THE MODEL 272 MEDICAL ISOLATION AMPLIFIER

Model 272* and some of its applications have been described in the two most recent issues of *Analog Dialogue*.† Briefly, Model 272 is a unity-gain amplifier with FET-input circuit isolated from both the output and the dc supply. It is specifically designed to protect hospital patients from both macro- and microshock, by isolating the outputs of patient-connected transducers from the instrumentation system. It will withstand 5kV defibrillation pulses, and can operate in the presence of 1,000VCM. Its common-mode rejection at 60Hz is 120dB with 5kΩ source unbalance. It is a potted module costing well below $100 in quantity. These few of its characteristics offer some hint as to its potential applicability in both medicine and industrial OEM applications calling for high isolation voltage.

We will discuss here some of the circuit techniques for dealing with its output signal in the context of a typical application family: electrocardiography.

AC COUPLING

The ecg signals transmitted by the 272 at unity gain have amplitudes typically of the order of a few millivolts. However, dc contact potentials at the electrodes add a normal mode signal of several hundred millivolts. In general, this dc potential is not constant, and thus cannot be conveniently biased out. For this reason, ac coupling to the preamplifier is used almost universally, to provide high signal gain without allowing the dc level to cause amplifier saturation. Unfortunately, ac coupling, using time constants long enough to pass ecg waveforms with reasonable fidelity, has a glaring weakness: Large transient signals can cause the preamplifier to "block" and the coupling capacitor to charge to a large potential, which must be discharged over a period of several heartbeats, during which time the ecg information is unavailable. Sources of transients include artifacts caused by patient motion, de-fibrillator pulses, and pacemaker pulses. An obvious approach to ameliorating this situation is to reduce the amount of charge acquired by the capacitor. This can be done using a pair of diodes back-to-back (Figure 1). For small signals, the diode's resistance is very large compared to that of the 62kΩ resistor. For large signals, the diodes will soft-limit in the neighborhood of 600mV. When the transient is removed, recovery to the 10mV region occurs within about 4.1 time constants, or 2.5 seconds. While this helps with infrequently-applied transients, it is of little
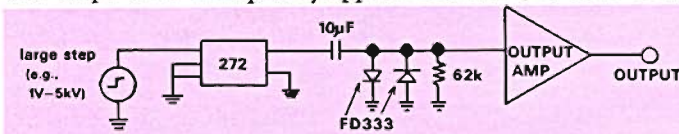
value if the transient is an 80-100mV pacemaker pulse applied for 10-20ms at every heartbeat.

To solve this problem, we can make use of the fact that the timing of the pacemaker pulse is known. Thus, suitably delayed and tailored, it can be applied to a clamp circuit that briefly "holds" the output during the interval that the pacemaker pulse is expected to appear on the electrocardiogram. One way of accomplishing this is shown in Figure 2.

There are a variety of other approaches in use, including one in which the signal is measured, processed, and compared with a reference level. A capacitor-shorting relay permits ac operation only if the signal is not excessive
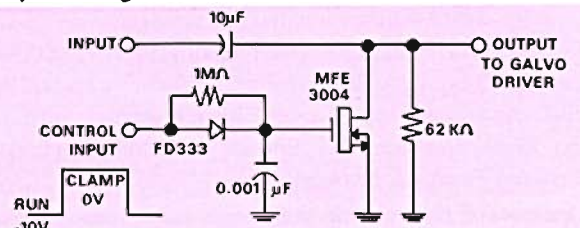
Figure 2. Circuit to Clamp Output During Pacemaker Pulse

GALVANOMETER DRIVER

Galvanometer coils respond most readily to current input. Therefore, following the input and its preamplifier, there is usually a voltage-to-current converter having sufficient output current available to drive the pens. Figure 3 shows a fairly conventional approach to such a circuit, using an op amp plus booster circuitry, and adjustable voltage feedback from a current-sensing resistor R3, to set the appropriate transconductance. C1 and C2 may be needed to stabilize the circuit by allowing feedback to bypass the high-frequency rolloff of the galvanometer and its driver. Shaping networks may be desirable in the feedback loop to compensate for the galvanometer's response characteristic.

Most commercially-available galvanometers are supplied (often optionally) with built-in amplifiers having appropriate characteristics. The "do-it-yourself" approach is best suited to those needing (or wishing) to save money at the expense of design time.
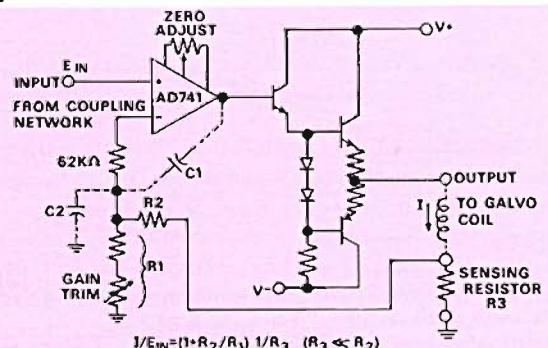
Figure 1. AC Coupling with Limit Protection

$$I/E_{IN} = (1 + R_2/R_1) \, 1/R_3 \quad (R_3 \ll R_2)$$

Figure 3. Typical Form of Galvanometer-Driver-Current-Boost Circuit

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Application Brief
The Many Scale Factors of the AD855 R-2R Ladder Network

In Vol. 5, No. 2 of *Dialogue*, the matter of voltage switches and R-2R resistive ladder networks for D-A conversion and 2- or 4-quadrant hybrid multiplication was discussed in some depth*, with particular reference to the AD555 12-bit quad voltage switches and the AD855[†] 12-bit R-2R resistive ladder network. As a reminder of that article, we reproduce here its "Figure 3" showing the connection of these devices as a 2-quadrant 12-bit multiplier (Unipolar digital number X bipolar analog signal).
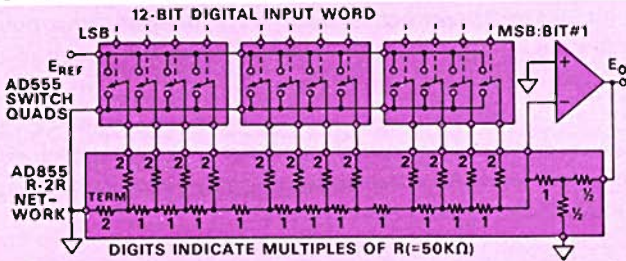
Quad Switches and R-2R Ladder Network Used in Simple 12-bit D/A Converter or 2-Quadrant Hybrid Multiplier. Amplifier may be used Either Inverting, with Tracking Gain Resistors, as Shown, or Non-Inverting, with External Feedback Network.

A feature of that circuit that bears some further discussion is the set of three feedback resistors shown in a "T-network" feedback connection around the operational amplifier. These resistors track one another, as well as the rest of the network, rather closely because of their monolithic construction and their close physical proximity.

If the output of the ladder is connected to the summing point of an inverting operational amplifier, and these resistors are used in the feedback path, a number of highly-precise scale factors are available, depending on the connection used. If, on the other hand, the amplifier is used non-inverting, these resistors may be used to obtain a number of values of fixed input attenuation. (Unfortunately, the 16-lead package used for the AD855 limits the number of available external leads, and thereby constrains the number of possible applications to something less than the ultimate number of permutations of three resistors and an op amp.)[‡]

The illustrations on this page show how to connect the resistors for each value of gain or attenuation. The network can be represented by the following equivalent circuit:
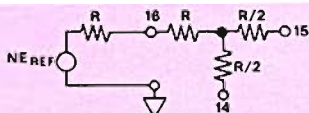
Equivalent Circuit of Switch-and Resistor Network, One Side Grounded. N is the Value of the Digital Number, as a Fraction of Full Scale (2^n), E_{REF} is the Input Voltage, in the Range ±4V (for AD555).

INVERTING CONNECTIONS
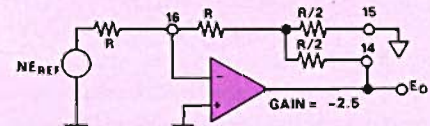
GAIN = -2.5
Full-scale output is ± 10V for E_{REF} = ± 4V
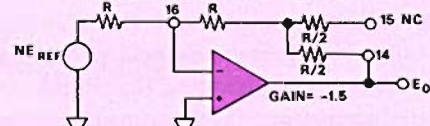
GAIN= -1.5
Full-scale output is ± 6V for E_{REF} = ± 4V
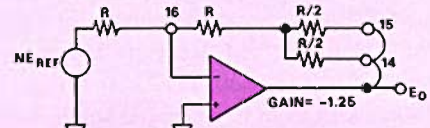
GAIN= -1.25
Full-scale output is ± 5V for E_{REF} = ± 4V
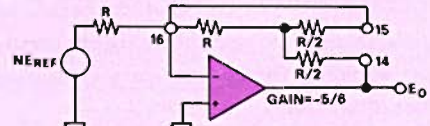
GAIN=-5/6
Full-scale output is ± 3.33V for E_{REF} = ± 4V
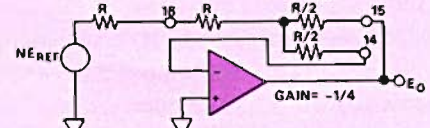
GAIN= -1/4
Full-scale output is ± 1V for E_{REF} = ± 4V

NON-INVERTING CONNECTIONS
(output to follower-connected op amp)
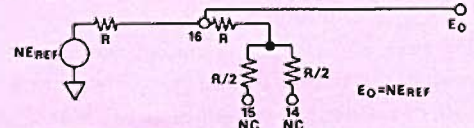
$E_O = NE_{REF}$
Full-scale output is ± 4V for E_{REF} = ± 4V
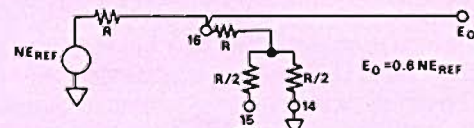
$E_O = 0.6 NE_{REF}$
Full-scale output is ± 2.4V for E_{REF} = ± 4V
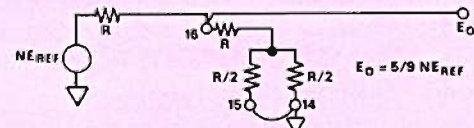
$E_O = 5/9 NE_{REF}$
Full-scale output is ± 2.22V for E_{REF} = ± 4V
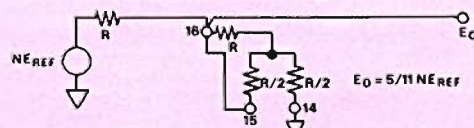
$E_O = 5/11 NE_{REF}$
Full-scale output is ± 1.818V for E_{REF} = ± 4V
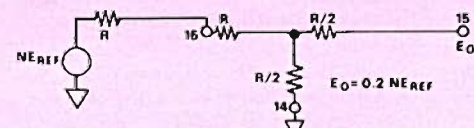
$E_O = 0.2 NE_{REF}$
Full-scale output is ± 0.8V for E_{REF} = ± 4V

Application Briefs

Sample/Arbitrary Hold

by Bob Craven, Staff Engineer, ADI

SAMPLE-HOLD USING A/D CONVERSION PERMITS ANALOG DATA TO BE STORED DIGITALLY FOR ARBITRARILY-LONG INTERVALS WITHOUT DROOP. DIGITAL READOUT IS AVAILABLE, TOO.

As we have indicated on page 7 of this issue, digital storage can provide the benefits of arbitrarily-long *hold* duration with no droop. Other advantages include: no sample-hold offset, no feedthrough, no dielectric absorption effects, and no sample-to-hold transients or settling time, since the system is automatically in *hold* after a conversion, unless a *sample* command is applied. In addition, both analog and digital outputs are available. Disadvantages are increased cost and complexity, typically longer acquisition time, and possible need for pre-sampling, in the manner of the two-stage Sample-Hold example, Fig. 8, page 8.

Figure 1 shows how this function can be achieved with a D/A Converter, an up-down counter, a comparator, a clock, and a few gates. The initial acquisition time may be quite long,
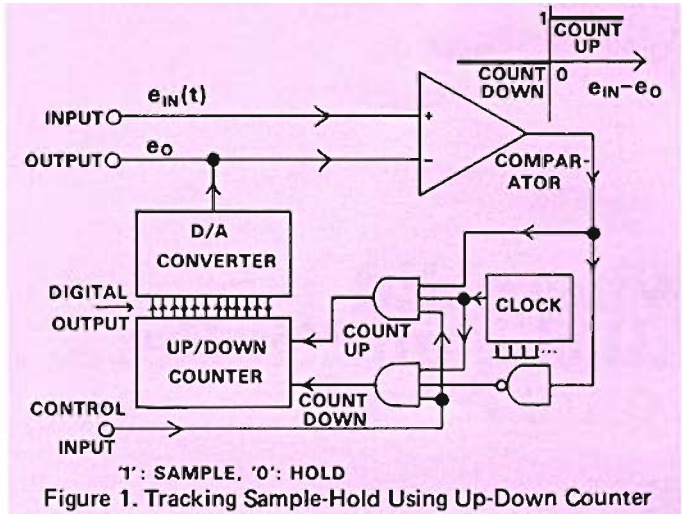

'1': SAMPLE. '0': HOLD
Figure 1. Tracking Sample-Hold Using Up-Down Counter

since the choice of clock frequency depends on the LSB settling time of the D/A converter, and the number of counts required depends on its resolution. For a full-scale step, acquisition time is approximately $(2^n - 1)\tau_s$. Smaller, slower changes, however, will be followed quite rapidly. The system can be converted into a *peak* follower by disabling the *down* count, and into a *valley* follower by disabling the *up* count. Reset, for peaks, is to 000 . . . 0, and for valleys to 111 . . . 1. The range of input signal levels and polarity determine the choice of D/A-converter output specifications. If a BCD counter and BCD DAC are used, with a numeric display, one has an "all-time-peak"-reading DVM.

Figure 2 shows the generic approach, using an A/D converter and a D/A converter. Where averaging is desired, the A/D converter may be an integrating type. The overall acquisition time is approximately equal to the sum of the A/D converter's conversion time and the DAC's settling time. If the D/A output of a successive-approximations type is available, suitably scaled

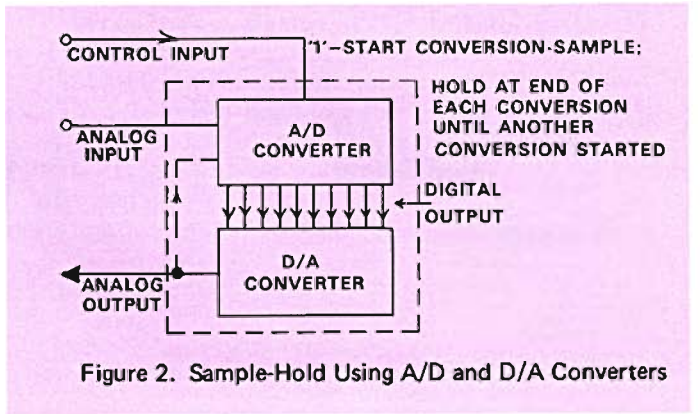and buffered, a separate D/A converter is unnecessary, and acquisition time is equal to conversion time. ◻◻◻

Figure 2. Sample-Hold Using A/D and D/A Converters

Digital Sweep Generation

by Bob Craven

CLOCK, COUNTER, AND DAC PROVIDE PRECISE SWEEP WITH INDEPENDENTLY-CONTROLLABLE AMPLITUDE & PERIOD, FAST RETRACE.

For a long time, the classical way to generate a sweep has been to make an integrator that is reset either automatically or periodically. With automatic reset, the amplitude is determined by the reset value, the frequency by the input level. With programmable reset, the amplitude is determined by the input level, the frequency by the reset rate. In either case, the essential elements are an op amp, a good capacitor, precision voltage source and resistors, a clamp switch. If frequency is to be adjustable, a choice of capacitors is needed for the several ranges, and a variable precision resistor (possibly ganged) for continuous adjustment. Amplitude and frequency are, in general, interdependent.

With low cost DAC's and digital logic now available, there is a Better Way: Use an adjustable-frequency clock pulse generator
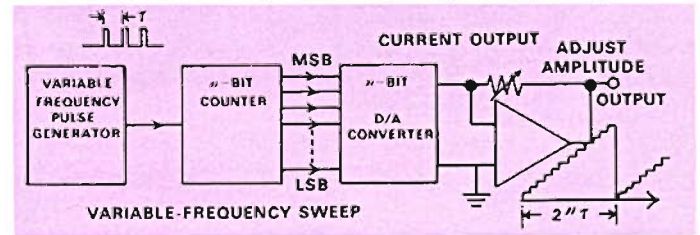
to drive a counter, which drives a D/A converter. Frequency then depends only on clock rate, and amplitude can be scaled from the output of the converter. Since the counter automatically recycles, the sawtooth is automatically reset after each 2^nth count, within 1 counting period.

Resolution is determined by the number of bits, linearity by that of the converter, and clock stability. For slow sweeps, filtering may permit use of a lower-resolution system. "Deglitched" converter output is desirable.* ◻◻◻

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*For information on the "de-glitched" DAC-10D Converter for display applications, use reply card. **Circle D14**