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Analog Dialogue

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Editors' Notes

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A key requirement in industrial and instrumentation (I&I) applications is a reliable data interface for inspecting connected systems via a diagnostic port. The RS-232 bus standard is one of the oldest and most widely used physical-layer bus designs. First introduced in 1962, this single-ended data transmission standard continues to be widely used for communications over a short cable. Page 6.

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Making Batteries Last Longer with Fast, High-Precision SAR Analog-to-Digital Converters

Low power consumption is key for today's devices: portable instruments require reduced size and weight, longer operating life, lower cost, and more features—and line-powered systems can operate without heat sinks or fans, making them smaller, lower cost, more reliable, and greener. Lowering the supply voltage, and turning a SAR ADC's fast clock off after each conversion can save power. Page 15.

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As a vital part of modern cars, wiring harnesses containing thousands of assembly components connect various electronic systems, enabling them to work together. A single failure in any harness can affect the entire system. This article offers a circuit idea that provides a robust, cost-effective technique for implementing wire diagnostics on the video and audio transmission lines in automotive applications. Page 18.

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UAV-mounted surveillance equipment, maritime microwave receivers, and vehicle-mounted infrared imaging sensors require stable platforms for best performance, but they are often subject to vibration and other undesirable kinds of motion. *Platform stabilization systems* employ closed-loop control systems to actively cancel this type of motion, thus preserving mission-critical performance objectives. Page 19.

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PRODUCT INTRODUCTIONS: VOLUME 46, NUMBER 3

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

July

ADC, quad, 16-bit, pipelined, 125-MSPS, LVDS **AD9653**
Battery charger, programmable, power path, USB **ADP5061**
Controller, dc-to-dc, step-down, tracking, synchronization **ADP1853**
Converter, dc-to-dc, step-up, 650 kHz/1.3 MHz **ADP1614**
Filter, video, single-ended, SD, short-to-battery protection **ADA4432-1**
Front-end, analog, 128-channel, digital X-ray systems **AD8488**
Front-end, audio/video, complete **ADV7850**
Sensor, inertial, ten degrees of freedom **ADIS16480**

August

ADCs, dual, 12-/14-bit, pipelined, 125-MSPS, LVDS **AD9635/AD9645**
Regulator, dc-to-dc, step-down, synchronous, 1-A, 36 V **ADP2441**

September

ADC, 12-bit, successive-approximation, ultralow-power, 1-MSPS **AD7091R**
Accelerometer, MEMS, digital, 3-axis, ±2-/±4-/±8-/±16-*g* **ADXL343**
Accelerometer, MEMS, digital, micropower, 3-axis, ±2-/±4-/±8-*g* **ADXL362**
Amplifier, audio power, 2-W, Class-D, audio processor **SSM2529**
Amplifier, audio power, 2-W, Class-D, digital input **SSM2519**
Amplifier, instrumentation, micropower, zero-drift **AD8237**
Amplifier, operational, dual, precision, ultralow-noise, zero-drift **ADA4528-2**
Amplifier, operational, quad, micropower, OVP **ADA4096-4**
Amplifier, operational, quad, micropower, precision **AD8659**
Codec, audio processor, low-power, four ADCs, two DACs **ADAU1772**
DACs, voltage-output, 10-bit *nano*DAC,® 2-ppm/°C reference **AD5316R/AD5317R**
DACs, voltage-output, quad, 12-/16-bit *nano*DAC+ **AD5684/AD5686/AD5694/AD5696**
Driver, LED flash, 1-A, I^2C-compatible interface **ADP1649**
Front-end, analog, low-power, 5-electrode ECG systems **ADAS1000**
Isolators, digital, 4-channel, 3.75-kV rms isolation **ADuM3480/ADuM3481/ADuM3482**
Sensor, inertial, precision, ten degrees of freedom **ADIS16448**
Modulator, quadrature, 100- to 2400-MHz, VCO, fractional-N PLL **ADRF6755**
Multiplexer, CMOS, high-voltage, latch-up proof, 8-channel differential **ADG5207**
Multiplexer, CMOS, high-voltage, latch-up proof, 16-channel **ADG5206**
Receiver, differential, triple, adjustable line equalization **AD8122**
Synthesizers, direct digital, 12-bit DAC, 3.5-/2.5-GSPS **AD9914/AD9915**
Translator, clock, adaptive, 4-input, 2-PLL, multiservice line cards **AD9559**

Analog Dialogue

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Isolation Technology Helps Integrate Solar Photovoltaic Systems onto the Smart Grid

By Martin Murnane

Solar Photovoltaic Inverters

A major portion of the electrical energy produced directly from the sun's radiation is generated by solar photovoltaic (PV) cells, which convert photons of light energy to electron flow that constitutes an electrical current. Figure 1 shows an aerial photo of a large solar PV installation.

Figure 1. Solar PV installation, Yuma County, Arizona.[1]

A solar *photovoltaic* (PV) *inverter* converts electrical power from a solar panel and deploys it to the utility grid efficiently. DC power from the solar panels, which act like a dc current source, is converted to ac and fed onto the utility's grid in the correct phase relationship—with up to 98% efficiency. The PV inverter conversion process can occur in one or more stages.

Stage 1 is typically a dc-to-dc conversion from the low voltage-high current solar cells that constitute the panels, to the high voltage-low current levels compatible with the ac voltage of the grid. This stage may not be necessary, depending on the topology and if enough solar cells are connected in series, on the dc side, to ensure a stable high voltage under all load conditions.

In *Stage* 2, dc is converted to ac, typically using an H-*bridge* topology. PV inverter designs may use variations of the H-bridge, such as *neutral-point clamping* (NPC), to improve efficiency and reduce reactive power in the system.

Early solar PV inverters were simply modules that dumped power onto the utility grid. Newer designs emphasize safety, intelligent grid integration, and cost reduction. Designers are looking to new technology, not used in existing solar inverter modules, to improve performance and reduce cost.

A key element is computer-based instrumentation and control, but an isolation barrier must protect measurement and computation circuitry from the power-handling circuitry—as well as from transient signals due to switching. This article will suggest how *i*Coupler® *isolation technology* can reduce cost, increase smart grid integration, and improve safety of solar PV inverters by using Analog Devices isolated analog-to-digital converters (ADCs) and gate drivers.

Smart Grid

What is a smart grid? IMS Research defines a smart grid as "a utility supply infrastructure with the inherent ability to match and manage generation and consumption efficiently, while obtaining maximum benefits from the available resources." This means that the new generation of solar PV inverters requires more intelligence to connect with the smart grid, especially to deal with the imbalance on occasions when more power is available from multiple sources than is needed by the grid. For this reason, the focus of PV system intelligence needs to be on *grid integration,* where each contributor to the system power must cooperate to stabilize the grid, rather than simply supplying power open-loop. Grid integration requires better measurement, control, and analysis of the quality of the energy fed to the grid. In addition, new directives and higher technical requirements call for new technology.

An important local feature of smart grid integration may, therefore, be *energy storage* to reduce turbulence on the grid by storing unneeded electrical energy until it is needed during peak usage. The rest of this article will focus on the role of electrical isolation in protecting the instrumentation circuitry used to measure and control the sources, interconnections, and storage elements—with primary emphasis on the key role of *i*Coupler technology. The AD7401A isolated ADC and the ADuM4223 isolated gate driver, in particular, offer performance that will meet the demands of new solar PV inverter designs.

Isolation Technology

In *i*Coupler technology, transformers couple data between two separately powered circuits while avoiding any galvanic connection between them. The transformers are fabricated directly on chip using wafer-level processing. A high breakdown polyimide layer underneath the gold layer insulates the upper coil from the lower one. Input logic transitions, encoded using 1 ns pulses, are routed to the transformer's primary side. The pulses, coupled from one transformer coil to the other, are detected by the circuitry on the secondary side of the transformer.

Isolated ADC

Figure 2 shows a pair of solar PV inverters like those described in the introduction. Tied to a power bus that is connected to the grid, they are independently measured and switched. Each solar panel is connected to its dc-to-dc step-up circuit, then to a dc-to-ac inverter. (When used, a storage battery would be connected and switched, under control. Any discussion of storage is omitted to simplify this explanation).

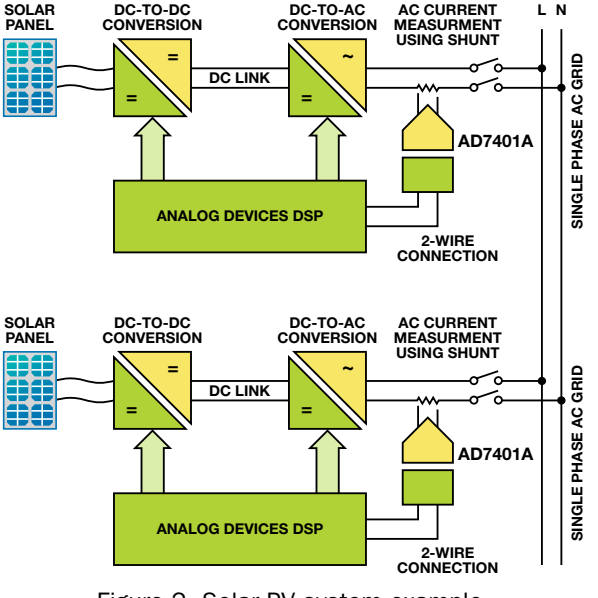

Figure 2. Solar PV system example.

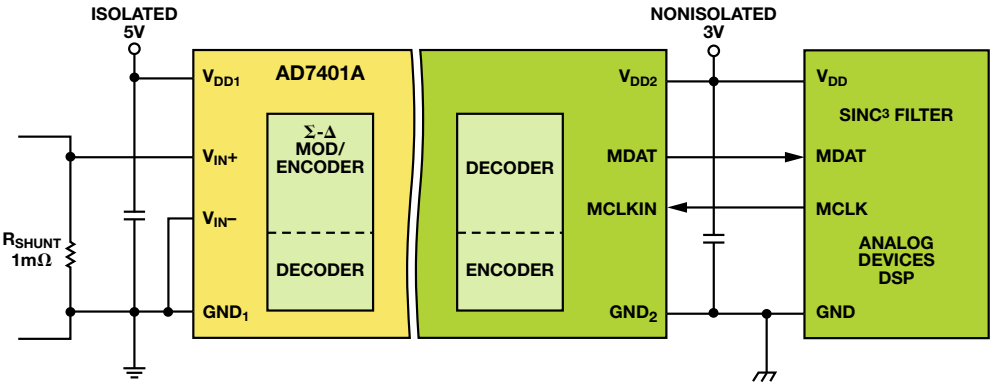

Figure 3. Isolated AD7401A ADC.

A *digital signal processor* (DSP) controls the process. The AD7401A isolated ADC measures ac output current of the order of 25 A. Solar PV inverter systems may or may not have an isolation transformer at the output. If the transformer is omitted to save cost, the solar PV inverter must also measure any dc component of the output current. The presence and magnitude of this *"dc injection"* is a critical matter, as too much dc current injected onto the grid may saturate any transformers in its path. This value must be limited to the low milliampere range, so the AD7401A must measure both ac current in the 25-A range and low-millliampere dc.

The AD7401A *i*Coupler-isolated Σ-Δ-modulator ADC, continuously samples the voltage across the current shunt, as shown in Figure 3. Its output is a 1-bit data stream, which is isolated and fed directly into a DSP. The density of ones in the output stream represents the input amplitude, which can be reconstructed with a digital filter implemented in the DSP.

Isolation is required within solar PV inverter systems, primarily because of the high voltages appearing on an ac grid. The ac voltage, even in single-phase systems, can peak at 380 V. The AD7401A's isolation can handle bipolar voltage up to 561 V, which makes it highly suitable for this application. A key advantage to using the AD7401A is that its small package allows the ADC to be located very close to the actual ac current shunt, whereas the DSP may be some distance away—or even on another board in the system. This improves the accuracy and reliability of data in the measurement and control system. The ADC output data is sent to the DSP serially via a single-bit stream at a 16-MHz clock rate, supplied by the DSP.

This system can measure ac currents up to 25 A and dc injection in the low milliampere range. Figure 4 illustrates offset and linearity errors of the AD7401A SMS solar module. This shows the offset current in the shunt at ±20 mA over temperature. Thus, the module can measure dc injection down to 20 mA, as well as 25-A (or greater) system currents using a single solution. Current transformers and other types of measurement systems might require two devices, one for large ac currents (25-A range) and one for small dc currents (300-mA range). This is one example of how *i*Coupler technology can provide smart grid integration with cost savings.

To minimize power loss (and thermal errors due to self-heating) in the shunt, its resistance needs to be kept to as low a value as possible, at typically 1 mΩ. The very high resolution of Σ-Δ converters allows current shunt losses to be kept on par with traditional magnetic transducer solutions while achieving better accuracy and lower offset, as shown in Figure 4.

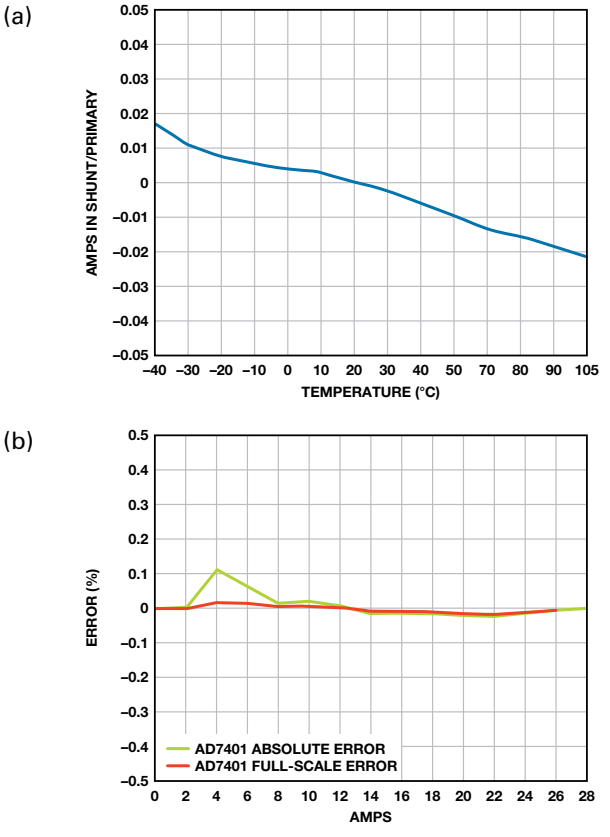

Figure 4. Offset and linearity of the AD7401A SMS solar module. a. Offset vs. temperature. b. Error vs.output current.

Although *full-scale accuracy* is extremely good, the real test of a device's *linearity* is its absolute error, especially at low ranges. *Absolute error* is the error associated with the measurement over its range of values, as opposed to simply the error at full scale. Some current transformers specify their devices as 0.1% full-scale range. While this looks good, it may not tell the full story.

From the data shown in Figure 4, the absolute error of current measurement using the AD7401A is quite low over the entire range, indicating low nonlinearity and reduced harmonic distortion of the waveform from the output of the solar PV inverter. This, in turn, helps reduce harmonic distortion when integrated with the grid, providing another example of how this new technology improves performance.

Isolated Gate Driver

The higher a solar PV inverter's efficiency, the more energy it can generate per year from a given solar input, which leads to a better return on investment for a solar farm. Due to their lower cost, the current trend is toward having transformerless electrical systems feed into the public utility grid. The correspondingly higher levels of efficiency in the inverter come with a need for more attention to internal isolation of its measurement and control electronics, that is, the isolation required between the power section of the inverter's MOSFET and/or gate drivers and the lower voltage circuitry.

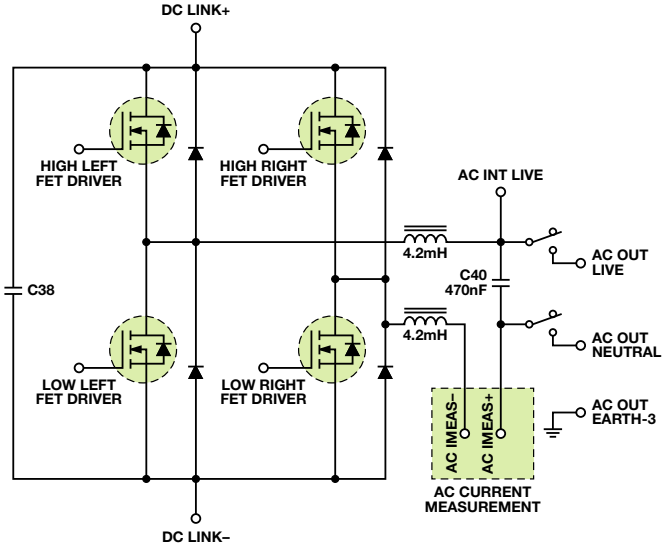

Figure 5. H-bridge circuit example for solar PV inverter.

Figure 5 shows one possible implementation of an H-bridge configuration for the dc-to-ac converter of a typical solar PV inverter. The dc link voltage in the circuit can range from 300 V up to 1000 V for the new SiC type JFETS on the market today. The current output waveform of the H-bridge is filtered using inductors and capacitors. Output relays connect the filtered output to the grid in a controlled manner. A gate driver is required to drive the *gate* and *source* terminals of the MOSFETs in a high-voltage environment—one more occasion for isolation in solar PV inverters.

As an example, the ADuM4223 4-A isolated, dual-channel gate driver with two independent isolation channels is shown in Figure 6. It has a maximum propagation delay of 60 ns and a common-mode transient immunity of >100 kV/µs (max). This device meets various standards, such as the relevant sections of DIN VDE0110, DIN VDE 088410, and UL1577, as described in the data sheet.

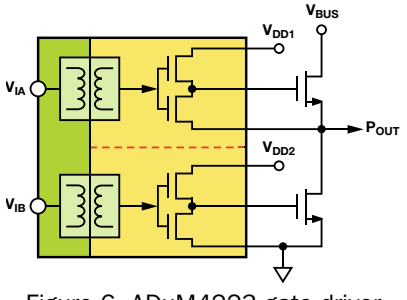

Figure 6. ADuM4223 gate driver.

The following are some of the most important isolation parameters of the ADuM4223:

- Maximum continuous working voltage
  - AC unipolar and dc 1131 V
  - AC bipolar 565 V
- Surge isolation voltage 6 kV
- Rated dielectric insulation voltage 5 kV

The device has two channels in one package, one each for the high-side and low-side MOSFETs. Having both channels in one package saves both cost and space on a PCB.

With conventional optocouplers, either a single optocoupler with level shifting on the isolated gate is required, or two optocouplers may be needed (see the MS-2318 technical article for further details)—another example of how this new isolation technology can reduce cost.

Another important issue for solar PV inverters is the high *common-mode transient immunity* required to ensure that any large transients (*dV*/*dt*) in the system do not cross the isolation barriers, whether coupled capacitively or otherwise, as this would make it possible for both high-side and low-side MOSFETs to turn on simultaneously (and catastrophically). The ADuM4223 has a high common-mode transient immunity: >100 kV/µs (max), providing yet another example of how this new technology can improve safety in the system.

Conclusion

Galvanic isolation is an important requirement for the measurement and control systems needed to implement smart grids that integrate large numbers of solar photovoltaic inverters. Analog Devices isolated ADCs, with their ability to measure both large currents and dc injection currents in a single solution, can contribute compactly and efficiently to smart grid integration circuitry. ADI isolated gate drivers, with good common-mode transient immunity specifications, contribute to safety and reliability of these new PV inverter systems.

New technology will be a major factor contributing to smart grid integration and the safe and efficient production of green energy—with key roles in grid stabilization and improved safety for all personnel working on grid systems. The isolation products discussed here are salient examples of innovations available from the broad Analog Devices portfolio of products for industrial measurement and control—for both current and future designs.

References

[1]Photograph: First Solar.

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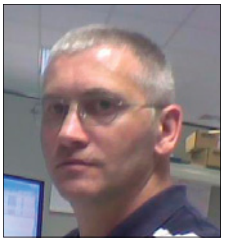
"'Smart' PV Inverter Shipments to Grow to 27 GW by 2015—Grid Integration the Key Driving Factor." http://www.pvmarketresearch.com/press-release/Smart_Inverter_Shipments_to_Grow_to_27_GW_by_2015_Grid_Integration_the_Key_Driving_Factor/4

Technical Article MS-2318, *Design Fundamentals of Implementing an Isolated Half-Bridge Gate Driver.* http://www.analog.com/static/imported-files/tech_articles/TA10756-0-5_12.pdf

Author

Martin Murnane [martin.murnane@analog.com] is a solar PV systems engineer in the Industrial and Instrumentation segment, focusing on energy/ solar PV applications. Prior to joining Analog Devices, he held several roles in power electronics in energy recycling systems (Schaffner Systems), Windows based application software/ database development (Dell Computers), and HW/FW product development using strain gauge technology (BMS). Martin has a bachelor's degree in electronic engineering from the University of Limerick.



Designing Robust Isolated RS-232 Data Interfaces for Harsh Industrial Applications

By Maurice O'Brien

Introduction

A key requirement in *industrial and instrumentation* (I&I) applications is a reliable data interface for inspecting connected systems via a diagnostic port. The RS-232 bus standard is one of the oldest and most widely used physical-layer bus designs in I&I applications. First introduced in 1962, RS-232 is a single-ended data transmission standard; yet despite rumors of its early demise, it continues to be widely used throughout the industry for communications over a short cable.

To achieve a robust data communications link in harsh industrial environments, the RS-232 diagnostic port must provide an isolated interface between the RS-232 cable network and the connected systems to protect against voltage spikes and ground loops within the noisy environment and improve system reliability (Figure 1). Power isolation of the RS-232 communication link is obtained by using an isolated dc-to-dc power supply or Analog Devices, Inc., *iso*Power® integrated dc-to-dc converter technology. Signal isolation of the RS-232 communication link is implemented using *optocouplers* or Analog Devices *i*Coupler® technology.

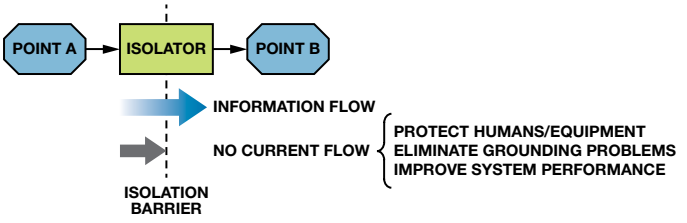


Figure 2. Isolation function.

As shown in Figure 2, an isolation barrier galvanically isolates the RS-232 bus from each system connected to it, allowing digital data to travel between two points but preventing the flow of ground loop currents; this reduces signal distortion and errors by removing noise that gets coupled onto the communications cable.

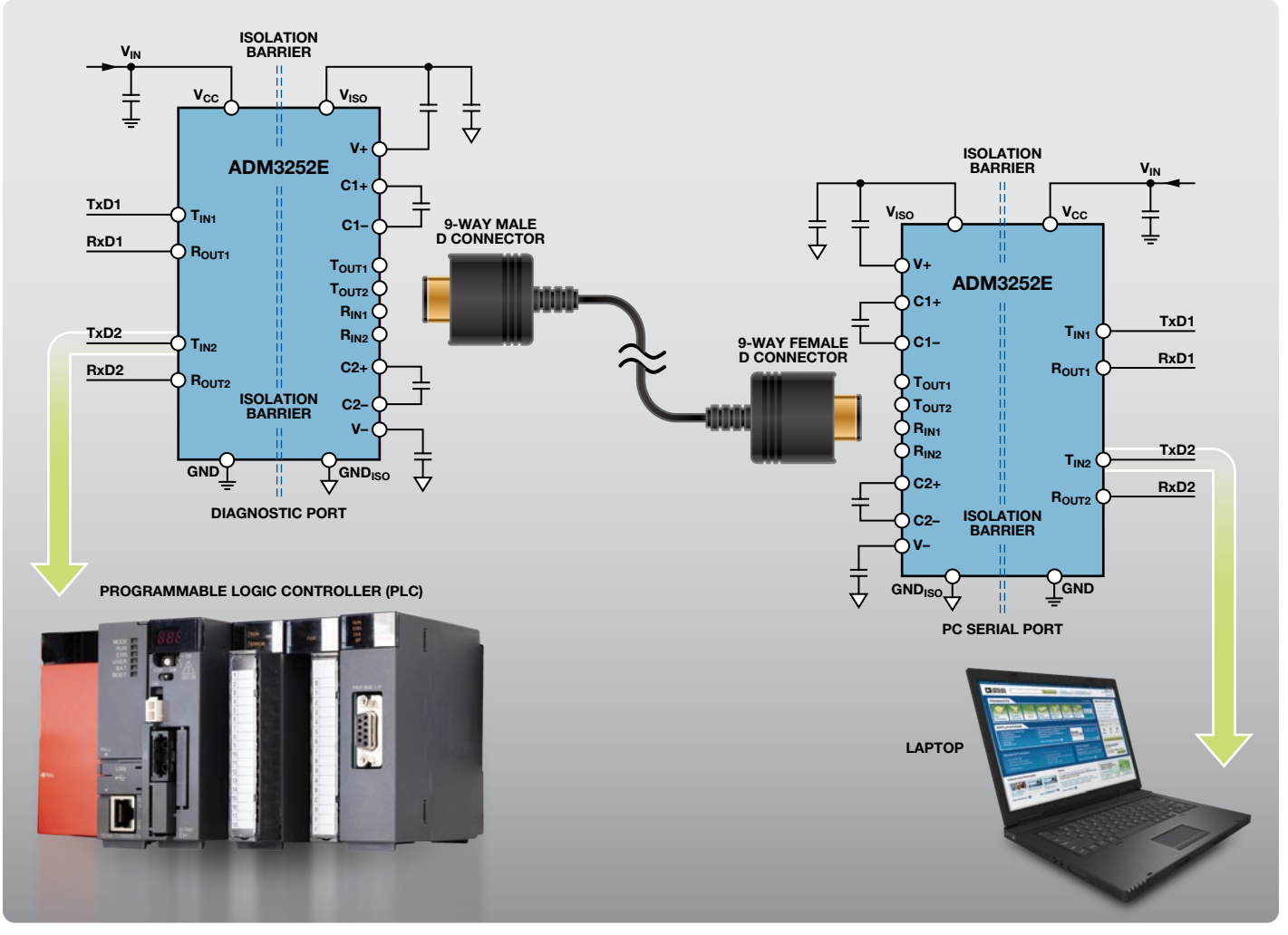


Figure 1. Typical isolated RS-232 communications link.

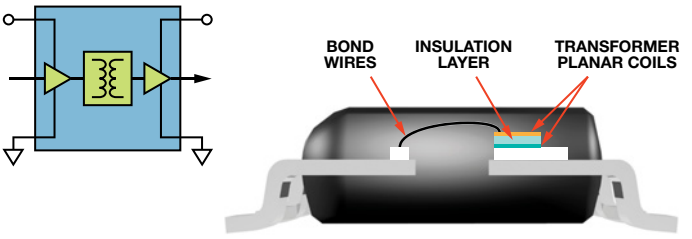
Implementing an Isolated RS-232 Interface

To provide an isolated RS-232 communications interface, the devices at both ends must be isolated from the RS-232 cable that connects them. To isolate a *data link*, both the data signal lines and the power required to drive the cable must be isolated. The data coming from the UART on the diagnostic port needs to cross the isolation barrier to the RS-232 transceiver on the isolated bus side. The local 5-V/3.3-V power supply also needs to cross the isolation barrier to power the RS-232 transceiver on the isolated bus side. This also needs to happen on the industrial PC side: both the data and power need to cross the isolation barrier (Figure 3).

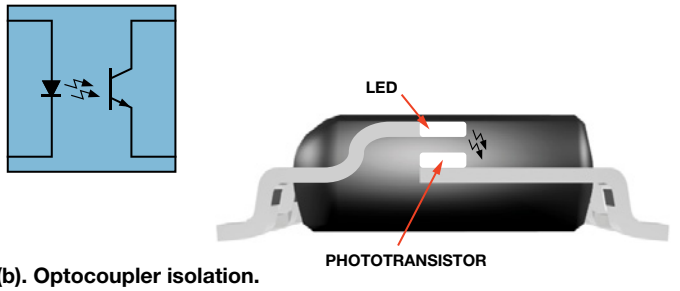
By isolating both devices from the RS-232 cable network, both the diagnostic port and the industrial PC circuitry are protected from transients that may get coupled onto the RS-232 cable in harsh environments. Ground loops that might occur due to different ground potentials at the diagnostic port and industrial PC side are interrupted by the isolation. The high common-mode voltages that might appear on the RS-232 bus are not allowed across the isolation barrier, protecting human users of the isolated data.

Isolation Technology: Data and Power

Figure 4 compares two principal isolation technologies. *i*Coupler technology, Figure 4(a), provides signal isolation in an RS-232 system by using thick-film processing techniques to build micro-scale on-chip transformers that achieve 2.5-kV isolation. The older, but widely employed, *optocoupler* solution, Figure 4(b), uses light-emitting diodes (LEDs) and photodiodes. The LEDs convert electrical signals to light, and photodetectors convert the light back to electrical signals. The intrinsically low conversion efficiency for electrical-to-light conversion leads to relatively high power consumption, the slow response of photodetectors limits their speed, and aging limits their lifetime.



(a). *i*Coupler isolation.



(b). Optocoupler isolation.

Figure 4. Isolation technologies compared.

Fabricating transformers directly on chip, using *wafer-level processing*, allows low-cost integration of *i*Coupler channels with each other and with other semiconductor functions. An example of this is the ADM3252E, an isolated two-channel RS-232 transceiver in a single compact device. *i*Coupler isolation overcomes the limitations imposed by the older optocoupler solution in at least five ways: *integration*—which reduces overall solution size and system cost due to the bidirectional operation of *i*Coupler—higher *performance*, lower *power consumption*, *ease of use*, and higher *reliability*.

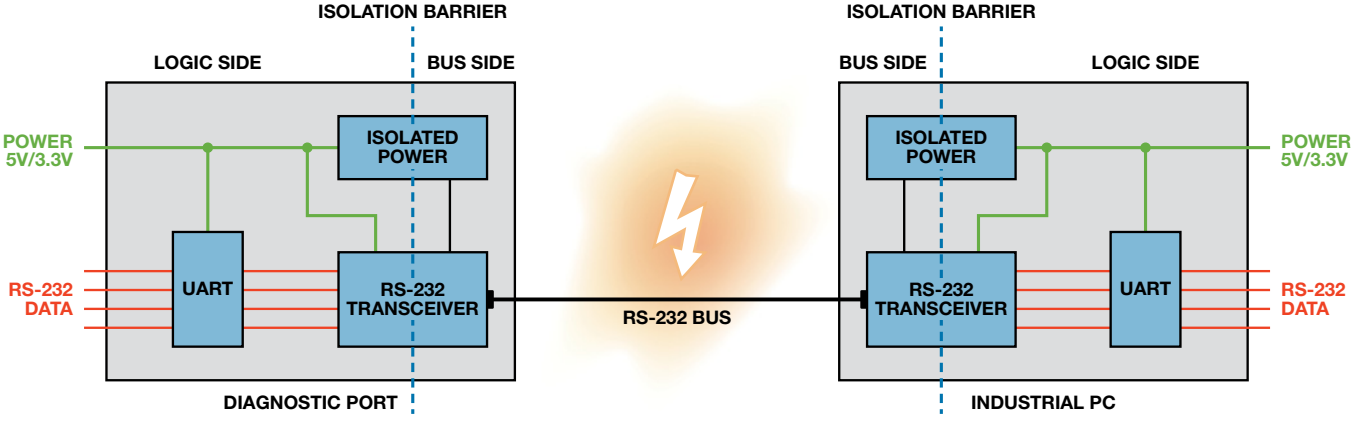


Figure 3. Isolated RS-232 interface.

Until recently, transferring power across an isolation barrier required either a separate dc-to-dc converter, which is relatively large, expensive, and has insufficient isolation, or a custom discrete approach, which is both bulky and difficult to design. These approaches have been the only viable alternatives, even in applications such as isolated RS-232 data communications, where only a small amount of isolated power is needed.

To solve this problem, Analog Devices developed and manufactured a complete, fully integrated solution that combines signal and power transfer across an isolation barrier using microtransformers. This extension of our well established *i*Coupler technology, termed *iso*Power, is a breakthrough alternative. Signal and power isolation within a single component—good up to 2.5 kV—eliminates the need for an isolated power supply that is bulky, expensive, and difficult-to-design. It can significantly reduce board space, design time, and total isolation system cost for a typical isolated RS-232 interface. The following sections describe two typical RS-232 design situations where this technology is applicable.

Isolated, High-Speed Dual-Channel RS-232 Interface

Figure 5 compares a legacy solution using discrete components with a fully integrated solution.

The traditional way of implementing a fully isolated 2-channel RS-232 interface, Figure 5(a), is to use optocouplers to provide data isolation of the RS-232 link. One optocoupler is needed for each data line (TIN1, TIN2, ROUT1, ROUT2), along with an external buffer for each one. The isolated power supply uses a transformer driver IC to drive a discrete transformer, along with a simple rectification circuit and an LDO (low-dropout regulator) to clean up the isolated 5-V or 3.3-V ISO V_{CC} rail. For implementation, this design requires eight ICs and a number of passive components—plus significant board space.

In a single-chip solution, Figure 5(b), a fully isolated (2.5-kV) two-channel RS-232 interface for all four signals can be implemented with just one IC (ADM3252E), plus two decoupling capacitors and four charge-pump capacitors.

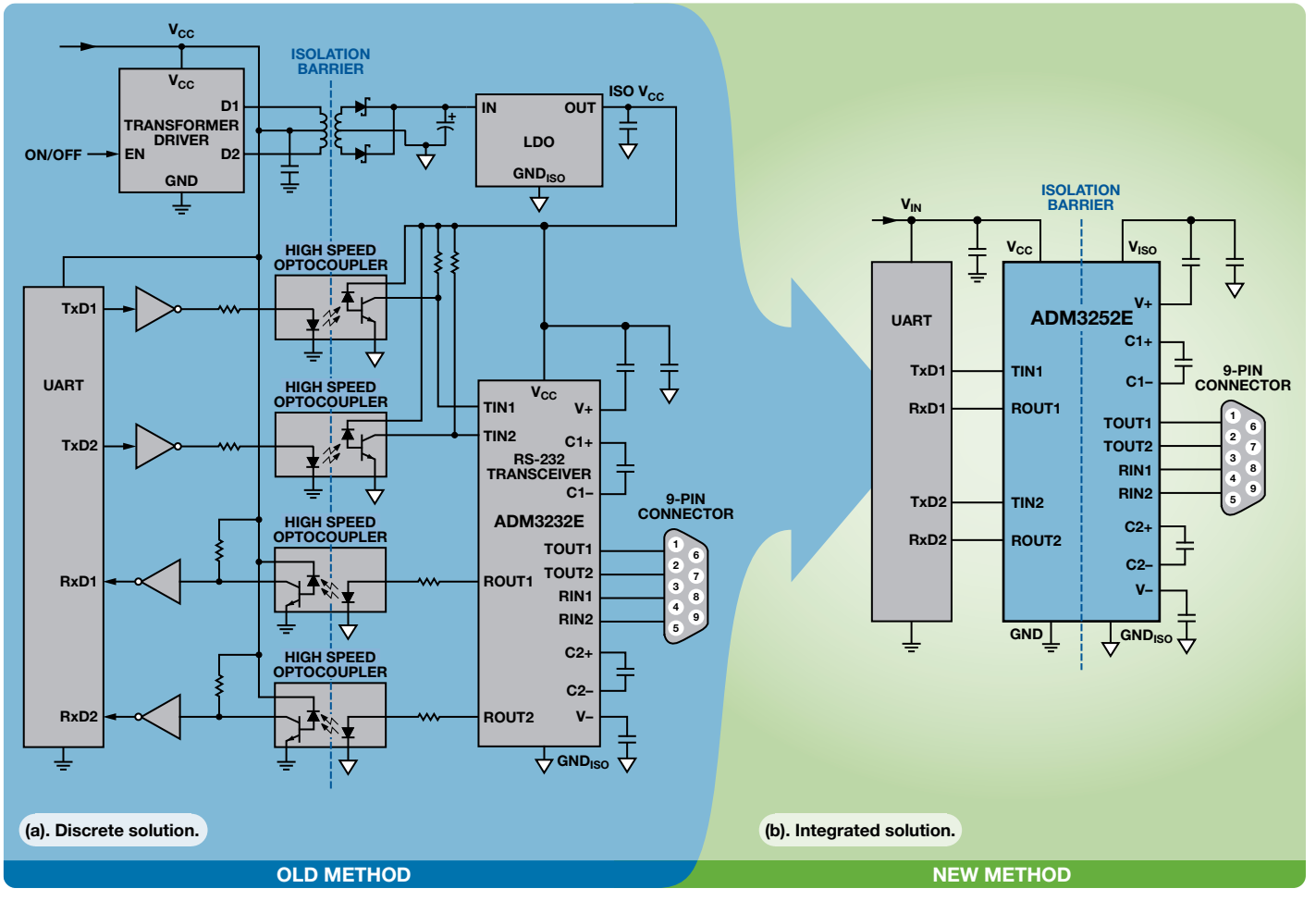


Figure 5. Isolated RS-232 designs compared.

The ADM3252E (Figure 6) combines a standard RS-232 transceiver with a 4-channel *i*Coupler, providing signal isolation of the RS-232 data signals. It also integrates *iso*Power technology to provide on-chip power isolation. Integrating the RS-232 transceiver by combining *i*Coupler and *iso*Power isolation technologies enables the ADM3252E to provide a fully isolated RS-232 interface with 2.5-kV rms isolation in a single package (12 mm × 12 mm), requiring only six external capacitors.

This single-chip solution significantly reduces the design time and board space required for an isolated RS-232 interface. Reliability is enhanced and cost is reduced because of the significantly smaller number of components to be placed on the PCB, which reduces manufacturing costs and improves reliability. Furthermore, the ADM3252E can be used in 5-V or 3.3-V applications without any modification, avoiding the design changes that would be necessary with a discrete design.

The *iso*Power technology provides 2.5-kV power isolation directly on chip within the 44-BGA package, eliminating the need for the expensive discrete transformer used in the traditional solution. In addition, *i*Coupler technology provides the signal (data) isolation, eliminating the need for the four discrete optocoupler channels.

ESD Protection

Because the RS-232 cable is physically connected and disconnected by a user, ESD (*electrostatic discharge*) protection of the RS-232 transmit (Tx) and receive (Rx) pins (TxD1, TxD2, RxD1, RxD2) is very important, to ensure a robust and reliable interface. The ADM3252E is specified with ESD protection to IEC 1000-4-2 (801.2) on RINx and TOUTx pins as follows:

- Contact discharge: ±8 kV
- Air gap discharge: ±15 kV

Transient Protection

To allow the isolated RS-232 transceiver to operate in very harsh operating conditions in industrial applications, the isolation technologies (both *i*Coupler and *iso*Power) are specified with a high (>25 kV/µs) common-mode transient immunity, which is the maximum slew rate of common-mode voltage (potential difference between the logic and bus sides) that can be sustained while maintaining specification-compliance. The *transient magnitude* is the range over which the common-mode voltage is slewed. The common-mode voltage slew rate applies to both rising and falling common-mode edges. This specification ensures that any transients that are coupled onto the RS-232 cable in a harsh environment cannot damage the RS-232 transceiver or cause erroneous data to be communicated, thereby enabling a very high reliability data link.

2.5-kV Isolation Protection and Approvals

The isolated transceivers are specified to 2.5-kV isolation between the logic and bus side of the device. This isolation rating ensures that no current can flow into or out of the logic side onto the RS-232 cable. It also ensures that no voltages or transients that get coupled onto the RS-232 cable are allowed to reach the logic side. The 2.5-kV isolation protection also means that users on the logic side are protected from high voltages or transients that might appear on the RS-232 cable. Approval is pending for the 2.5-kV isolation rating of the ADM3252E at the following agencies: Underwriters Laboratories (UL), *Verband Deutscher Elektrotechniker* (VDE), and Canadian Standards Association (CSA). The UL 1577 approval requires the isolation barrier of all ADM3252E devices (as with optocouplers) to be 100% production tested:

- UL recognition
  - 2500 V rms for one minute per UL 1577
- VDE certificate of conformity
  - IEC 60747-5-2 (VDE 0884, Part 2)
  - VIORM = 560 V peak
- CSA Component Acceptance Notice #5A

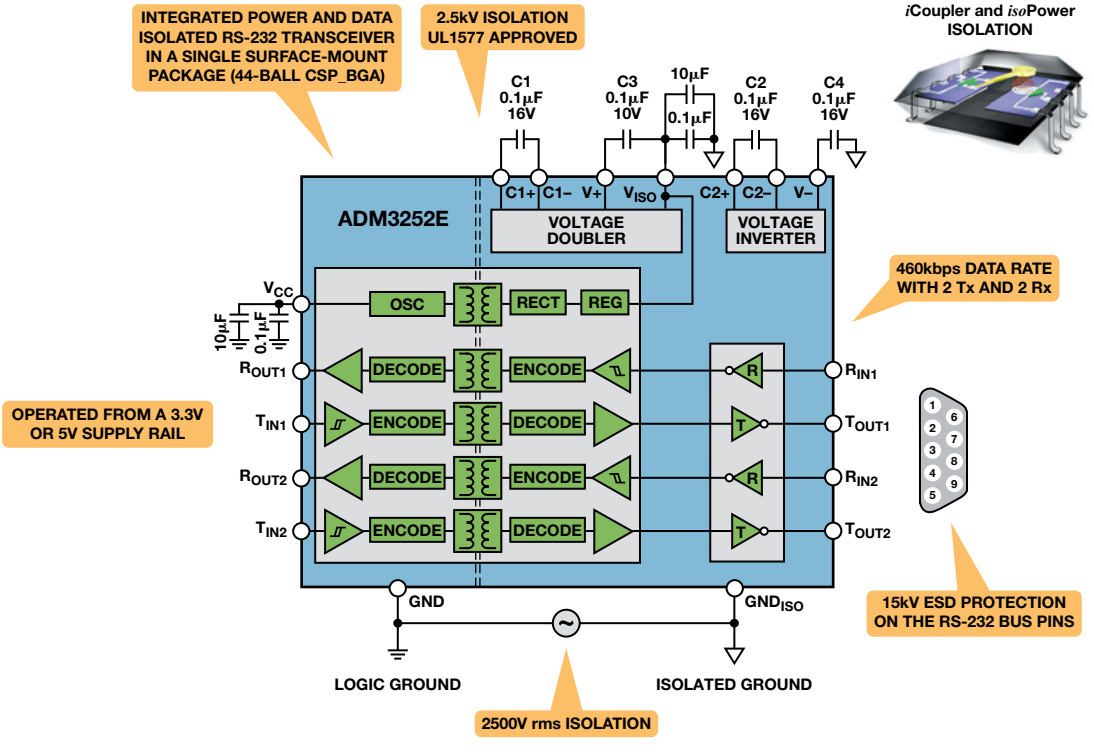


Figure 6. ADM3252E isolated, two-channel RS-232 transceiver.

ADM3252E Specifications

The ADM3252E 2-channel, high-speed, fully isolated (data and power) RS-232 transceiver is ideally suited to operate in electrically harsh environments—or where RS-232 cables are frequently plugged in and unplugged. Integrating four independent *i*Coupler digital isolation channels (two transmit, two receive) and an *iso*Power chip-scale dc-to-dc converter, it provides 2.5-kV rms isolation, 25-kV/µs transient immunity, and ±15-kV ESD protection. Communicating at data rates up to 460 kbps, it conforms to TIA/EIA-232E specifications. An on-chip voltage doubler and inverter enable single-supply operation. Operating on a single 3.0-V to 5.5-V supply, the ADM3252E draws 20 mA with no load. Available in a 12-mm × 12-mm, 44-ball CSP BGA package, it is specified from –40°C to +85°C and priced at $8.49 in 1000s.

PCB Layout

The PCB layout of the isolated transceiver is critically important to ensure that the specified 2.5-kV isolation is achieved in an actual design. The principal considerations are the *creepage* (shortest distance along the surface between two conductors) and the *clearance* (shortest distance through the air) between the logic side GND and the bus side GND. The ADM3252E requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (Figure 7). Further information on guidelines for PCB layout and construction for controlling radiated emissions (EMI) can be found in the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices*.

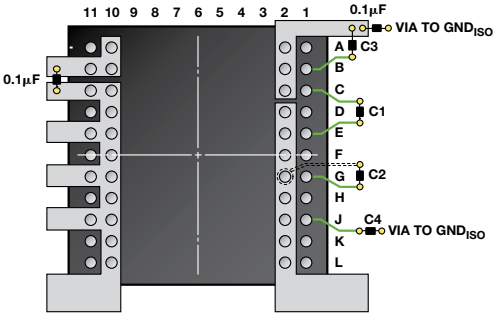


Figure 7. ADM3252E recommended printed circuit board layout.

Isolated, High-Speed Single-Channel RS-232 Interface

For transceiver applications requiring only a single channel (1 Tx, 1 Rx), 5-V isolated RS-232 interface, the ADM3251E provides a single-chip solution in a 20-lead wide-body SOIC. The ADM3251E transceiver incorporates *i*Coupler and *iso*Power isolation technologies; it was the first surface-mount RS-232 transceiver to feature full isolation of both the data lines and power. With a 2.5-kV isolation rating, it complies with industry-standard isolation requirements (UL1577 and DIN VDE 0884-10). This ensures that it will meet the robustness levels required in noisy operating environments, such as isolated RS-232 diagnostic data ports in industrial automation and control applications. The SMT package reduces board space by 45% compared with traditional ICs—and helps to accelerate the manufacturing process and lower system development costs (Figure 8).

Conclusion

Today's RS-232 interface links in industrial and instrumentation applications need to be small, robust, and inexpensive, as well as isolated. By integrating chip-scale transformer isolation with a standard RS-232 interface transceiver, single-chip, fully isolated RS-232 transceivers (including isolated power) can be made available to provide these benefits. The two-channel ADM3252E and single-channel ADM3251E significantly reduce design time and provide a compact, reliable, low-cost, high-performance solution for these demanding applications.

For More Information

- Digital Isolators
- Digital Isolator Product Selection and Resource Guide

Author

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(a)

Part Number	Min Positive Supply (V)	Data Rate (kbps)	Isolation (kV rms)	No. of Tx	No. of Rx	ESD Protection (kV)	Low Power Shutdown	Package	Price ($U.S.)[1]
ADM3251E	4 .5	460	2 .5	1	1	15	No	20-lead, wide-body SOIC	2 .99

[1]1000 to 4999

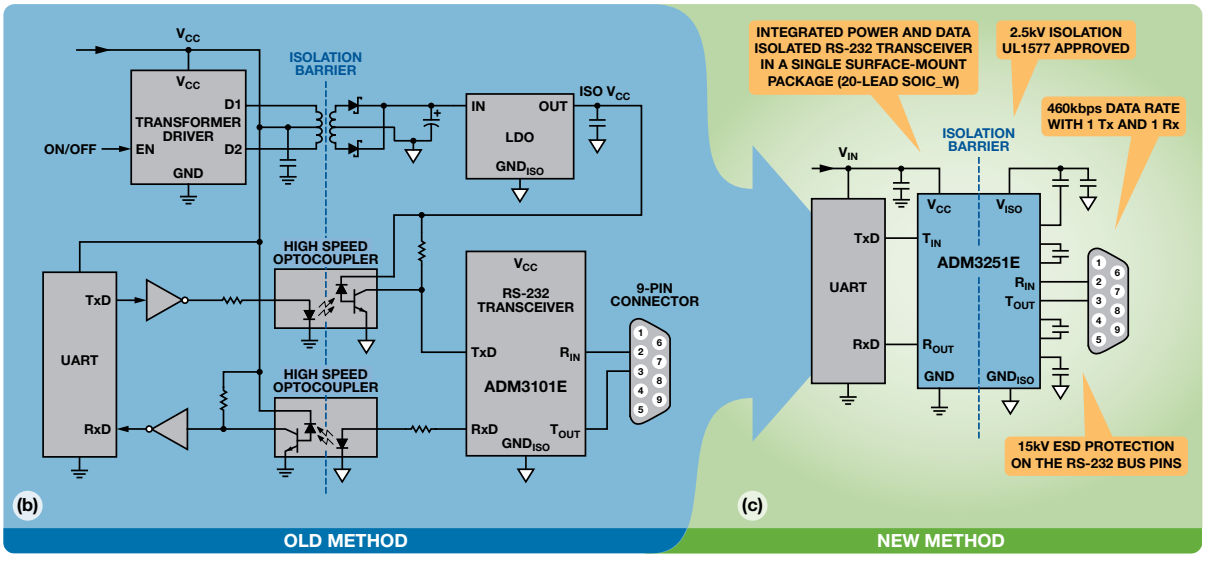

Figure 8. Single-channel RS232 transceiver application. (a) ADM3251E specifications. (b) legacy approach. (c) *i*Coupler + *iso*Power approach.

ADuC7026 Provides Programmable Voltages for Evaluating Multiple Power Supply Systems

By Steven Xie, Karl Wei, Claire Croke

Introduction

High-voltage switches, bipolar ADCs, and other devices with multiple power supplies often require that supply voltages be applied or removed in a particular sequence. This article proposes an easy, cost-effective method for determining the behavior of a system when subjected to supply transients, interruptions, or sequence variations. An example of a device using multiple supplies is the AD7656-1 (Table 1), a 16-bit, 250 kSPS, 6-channel, simultaneous-sampling, bipolar-input ADC. The ADuC7026 precision analog microcontroller's four 12-bit DACs provide the DUT's programmable supply voltages. Using the AD7656-1 evaluation board and the ADuC7026 evaluation board, prototyping can be performed with a minimum of hardware and software development.

Table 1. AD7656-1 Typical Supply Voltages and Maximum Supply Currents

Supply	AV_{CC}, DV_{CC}	V_{DRIVE}	V_{DD}	V_{SS}
Voltage (V)	5	3.3	10	–10
Current (mA)	30	10	0.25	0.25

Table 1 shows the typical voltage and maximum current for each of the ADC's power supplies. The programmable sequence-controllable voltage waveforms generated by the four DACs on the ADuC7026 are scaled by the ultralow noise-and-distortion AD797 op amps on the AD7656-1 evaluation board to provide the specified supply voltages and currents. The microcontroller's speed and programmability facilitate control of voltage level, period, pulse width, and ramp time of the power supply voltages.

For example, using external power supplies, the AD797 amplifiers on the AD7656-1 evaluation board, configured for a gain of 5, can generate a voltage range of 0 V to 12.5 V to drive the ADC's V_{DD} supply rail. The high output drive capability of the AD797 allows up to 50 mA to be provided to each supply rail. Figure 1 shows the connections to the ADC.

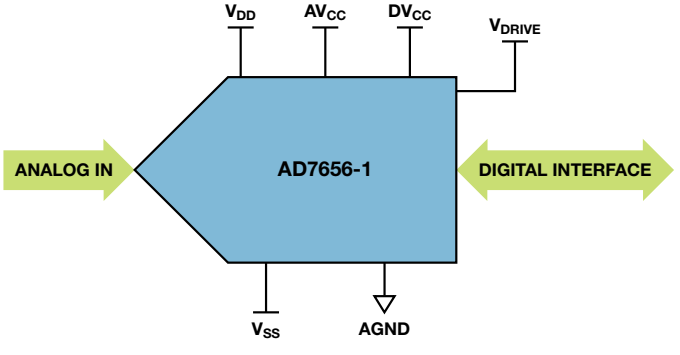

Figure 1. AD7656-1 connection diagram.

The ADuC7026 DAC data register can be updated at 7 MHz with a 41.78-MHz core clock, which maximizes the voltage update rate. The following sections describe the development process and provide measurement results obtained using the evaluation boards.

Hardware Development and Setup

The hardware connection and test setup are shown in Figure 2. Four DAC output pins and AGND on the ADuC7026 evaluation board are connected separately to the four AD797 inputs and AGND on the AD7656-1 evaluation board. An Agilent E3631A external power module provides ±15 V for the AD797. A computer connected via USB to the ADuC7026 evaluation board provides the 5-V power supply and serial communications.

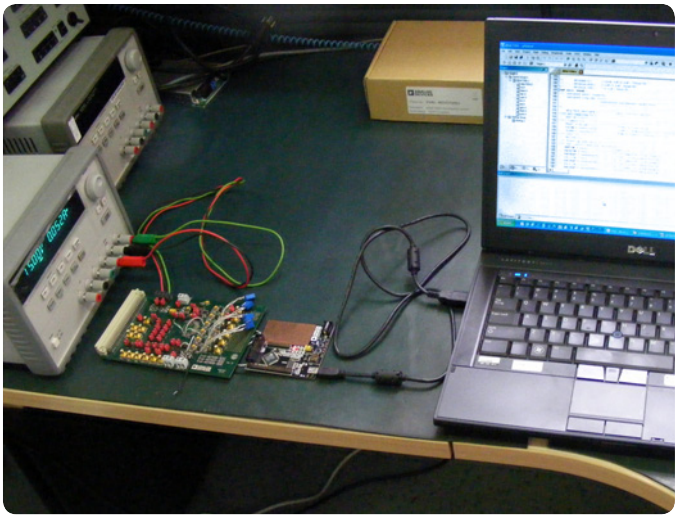

Figure 2. Hardware connections and test bench.

Schematic Design

The only hardware changes required on the AD7656-1 evaluation board relate to the AD797. R1 and R2 can be selected for different gain and bandwidth requirements. Figure 3 shows the AD797 set for gain = 4 to provide a 0-V to 10-V output from the 0-V to 2.5-V output of the ADuC7026 DAC. R3 and C1 form a low-pass filter to reduce high frequency noise. CL is used as a load capacitor on the power rail.

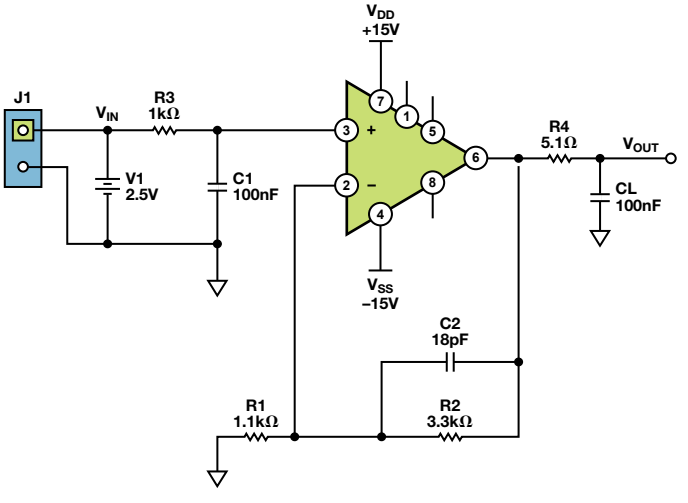

Figure 3. AD797 schematic design with gain = 4.

Figure 4 shows the frequency response of the AD797 with gain = 4, from an NI Multisim™ simulation. The 1.0-MHz bandwidth and 73° phase margin provide fast transient response and stable operation.

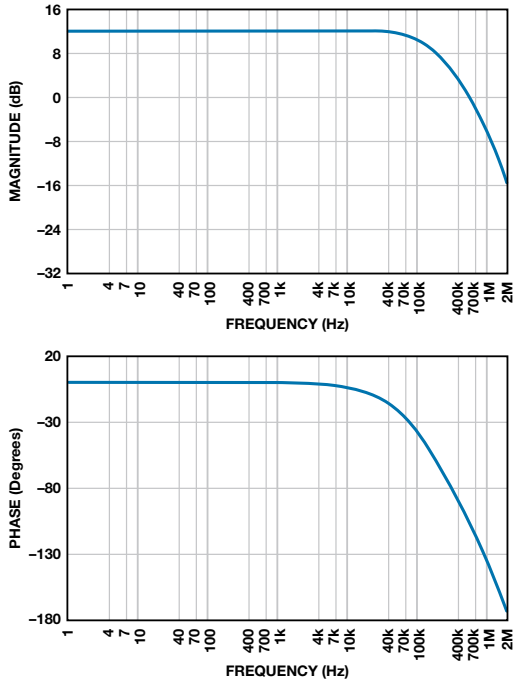

Figure 4. Frequency response of the AD797 with gain = 4.

AD797 Design Notes

The AD797 ultralow-distortion, ultralow-noise op amp features 80-µV maximum offset voltage, excellent dc precision, 800-ns settling time to 16 bits, 50-mA output current, and ±13-V output swing with ±15-V power supplies, making it well suited to driving power-supply rails.

It is not internally compensated for substantial capacitive loads though, so external compensation techniques must be used to optimize this application. Figure 5 shows oscillation on the AD797 output caused by driving capacitive loads.

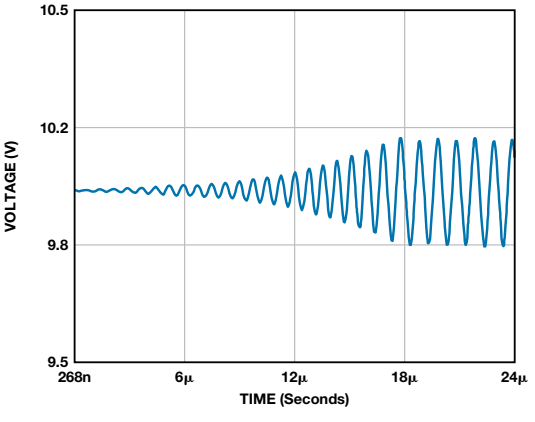

Figure 5. Oscillations without compensation.

For stable drive with capacitive loads on the power rail, Resistor R4 is placed between the output and the load. This resistor isolates the op amp output and feedback network from the capacitive load and introduces a zero in the transfer function of the feedback network, reducing the phase shift at higher frequencies.[1] The feedback capacitor, C2, compensates for the capacitive loading, including C1, at the input of the op amp.

Applying the DACs

The ADuC7026 precision analog microcontroller features four 12-bit voltage-output DACs with rail-to-rail output buffers, three selectable ranges, and 10-µs settling time.

Each DAC has three selectable ranges: 0 V to VREF (internal band gap 2.5-V reference), 0 V to DACREF (0 V to AV_{DD}), and 0 V to AV_{DD}. The range is set using the control register DACxCON. The DAC accepts an external reference with a range of 0 V to AV_{DD}. When using the internal reference, a 0.47 µF capacitor must be connected from the VREF pin to AGND to ensure stability.

Each of the four DACs is independently configurable through control register DACxCON and data register DACxDAT. Once the DAC is configured through the DACxCON register, data can be written to DACxDAT for the required output voltage level.

The four DAC outputs are easy to control using C or assembly language. This C-code example shows how to choose the internal 2.5-V reference and set the DAC0 output to 2.5 V.

```
//connect internal 2.5 V reference to VREF pin
REFCON = 0x01;
//enable DAC0 operation
DAC0CON = 0x12;
//update DAC0DAT register with data 0xFFF
DAC0DAT = 0x0FFF0000;
```

Using assembly language,

```
DAC0CON[5] is cleared to update DAC0 using core
clock (41.78 MHz) for fast update rate;
DAC0CON[1:0] is set to '10' to use 0 V to VREF
(2.5 V) output range
'DAC0DAT = 0x0FFF0000' can be compiled to assembly
code with two instructions:
MOV      R0, #0x0FFF0000
STR       R0, [R1, #0x0604]
```

These two instructions take a total of six clock cycles to execute, corresponding to a 7-MHz update rate with a 41.78-MHz core-clock frequency. Thus, the time delay between voltage rails can be as accurate as 144 ns.

Measurement Results

The four DACs in the ADuC7026 supply four power supplies to the AD7656-1 to test its behavior with power-supply transients or sequence variations. Table 2 shows the ADC's power supplies and voltage levels.

Table 2. Power Supplies for AD7656-1

DAC Channel	DAC0	DAC1	DAC2	DAC3
Output Range	0 V to 1.250 V	0 V to 0.825 V	0 V to 2.500 V	0 V to 2.500 V
AD797 Gain	4	4	5	–5
AD797 Output Swing	0 V to 5.00 V	0 V to 3.30 V	5.00 V to 12.50 V	–12.50 V to –5.00 V
Nominal Voltage	5.00 V	3.30 V	10.00 V	–10.00 V
AD7656-1 Power Supply	AV_{CC}, DV_{CC}	V_{DRIVE}	V_{DD}	V_{SS}

The waveforms from the four DAC outputs, as described in Table 2, were captured using a scope and are shown in Figure 6. The voltage level, period, pulse width, and ramp time of each channel are each programmable and easy to control. The specific parameters are measured and described in the following sections.

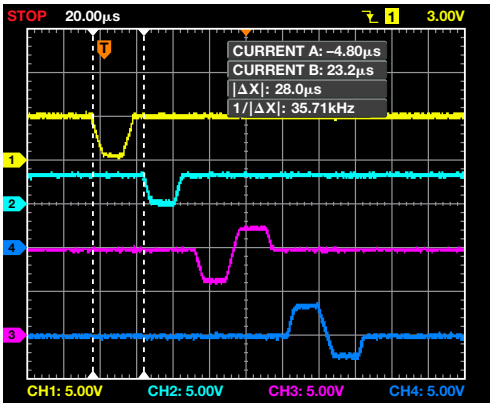

Figure 6. Four-channel voltage waveform.

To achieve an accurate voltage level for each power supply, an adjustable resistor can be used for R1 in Figure 3. The voltage level was calibrated by adjusting R1 with an Agilent 34401A digital multimeter.

Rising and falling ramp time are measured to determine the maximum frequency of the voltage waveforms. The ramp time is related to the value of Resistor R4 and the capacitive load, CL. For slower ramp times, larger resistor and capacitor values can be used for R4 and CL. The rising and falling ramp time of AV_{CC} and DV_{CC} were tested with different load capacitors, with the results shown in Table 3. The rising waveform with a 1-µF capacitor is shown in Figure 7. The ramp time is measured between 10% and 90% of 10 V.

Table 3. Ramp Time with Capacitive Load

Capacitive Load	10 nF (V/µs)	0.1 µF (V/µs)	1 µF (V/µs)	10 µF (V/µs)
Rising Edge	6.90	0.97	0.07	0.01
Falling Edge	5.71	0.93	0.06	0.01

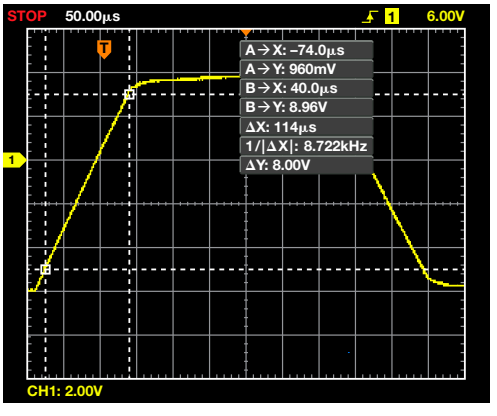

Figure 7. Rise time with 1-µF capacitive load.

Power-Supply Ripple

The excellent dc precision of the AD797 makes it easy to provide accurate nominal voltage levels for the AD7656-1 by adjusting the feedback resistor, R1. The peak-to-peak ripple of the power supplies was measured at nominal voltage levels with 200-MHz and 20-MHz bandwidths, a 0.1-µF capacitive load, and a DS1204B scope. Table 4 shows that the ripple is less than 1% of the nominal voltage, so the four supplies are qualified.

Table 4. Ripple of Each Power Supply

Power Supply	AV_{CC}, DV_{CC} (5.00 V)	V_{DRIVE} (3.30 V)	V_{DD} (10.00 V)	V_{SS} (–10.00 V)
200 MHz (mV)	20.8	28.0	25.6	30.4
20 MHz (mV)	12.8	24.8	15.2	18.4

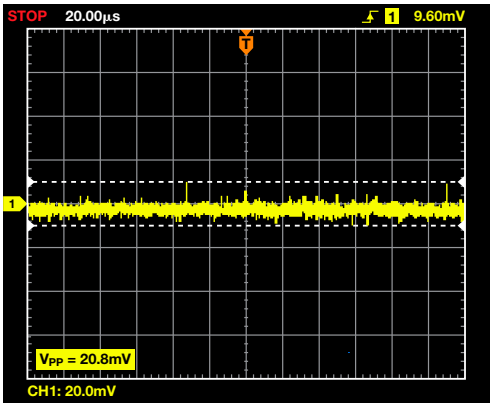

Figure 8. Ripple of 5-V supply on AV_{CC} and DV_{CC}.

Generating Waveforms

With simple modifications to the ADuC7026 source code, many different sequences of voltage waveforms can be generated for a variety of different applications that require evaluation of device operation under different supply conditions. Typical waveforms that can be generated are shown in Figure 9 and Figure 10.

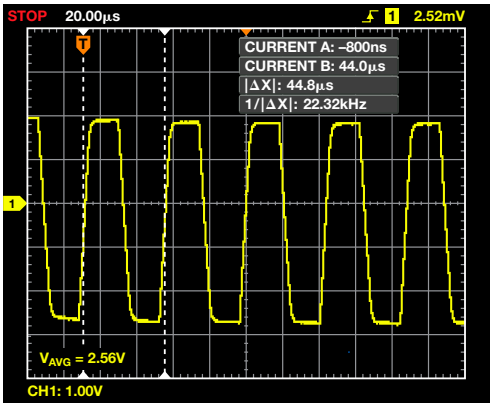

Figure 9. 22.32 kHz square waveform.

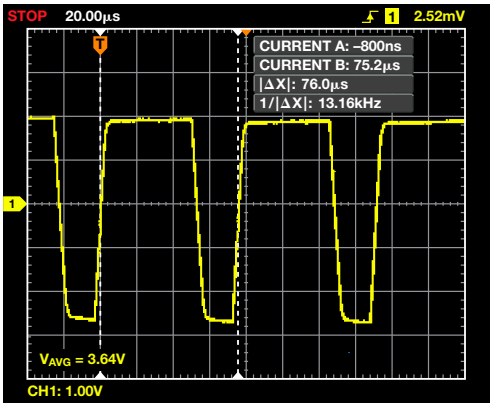

Figure 10. 13.16 kHz pulse waveform.

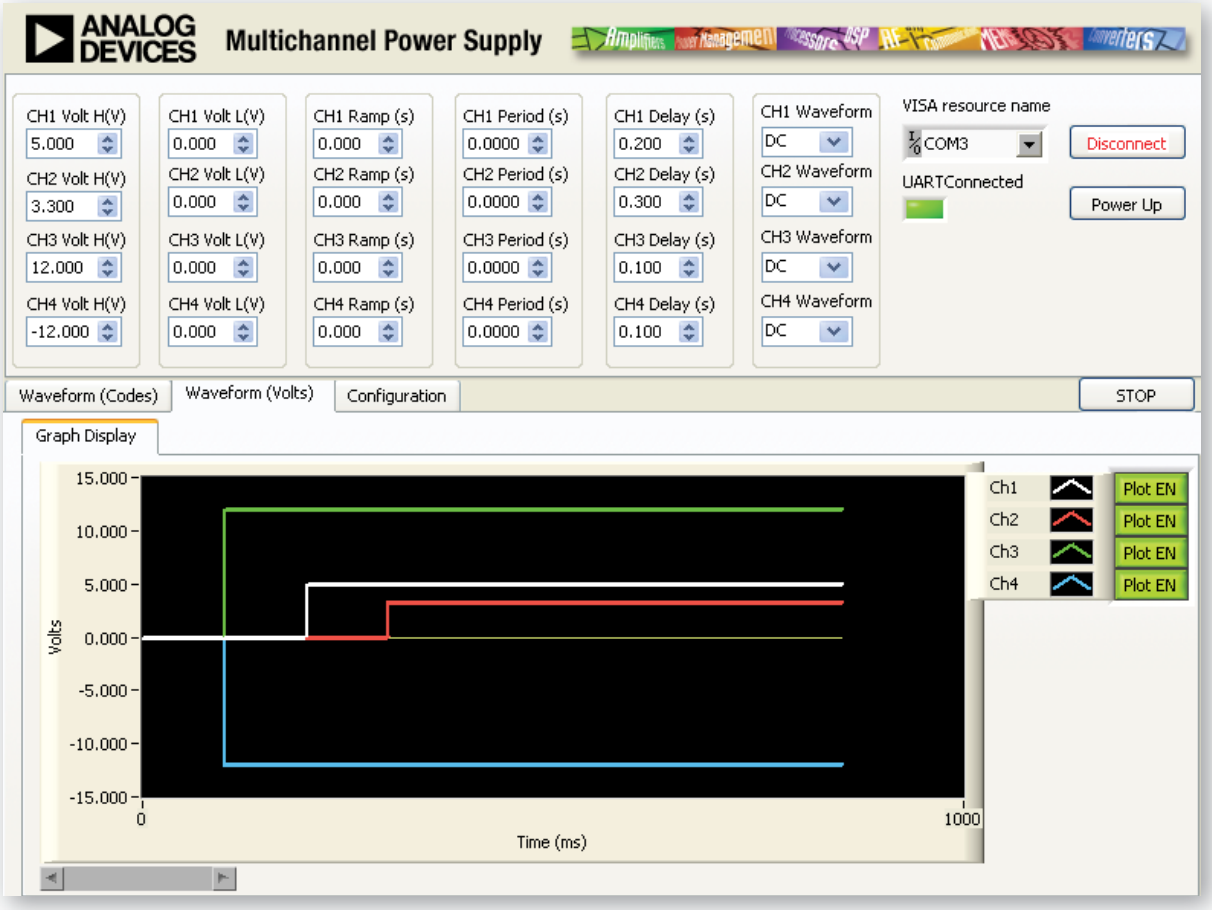

Figure 11. Power supply configuration GUI.

The LabVIEW® GUI shown in Figure 11 can be used to generate the power supply waveforms. The voltage level, ramp time, period, and sequence delay time of the four channels are easy to configure. The serial port is used for communication between GUI and the ADuC7026.

Conclusion

An easy, cost-effective way to evaluate the effects of supply sequencing was developed and verified using the AD7656-1 and ADuC7026 evaluation boards. The ADuC7026 evaluation board generates a controllable programmable sequence for four voltage supplies to evaluate the operation of the ADC under different supply sequence/ramp conditions. The 3-phase, 16-bit PWM generator in the microcontroller can provide a total of seven voltage channels.

With a standard ±15-V dc power module, this portable power supply evaluation systems allows designers to evaluate ADCs, especially for those with larger number of supplies.

Acknowledgments

The authors would like to thank Aude Richard (ADuC applications engineer) for her great advice and help.

[1]Bendaoud, Soufiane and Giampaolo Marino, Practical Techniques to Avoid Instability Due to Capacitive Loading (Ask the Applications Engineer—32), *Analog Dialogue*, Volume 38, Number 2 (2004).

Authors

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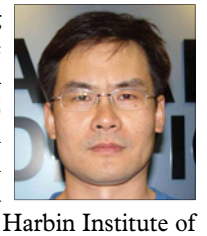

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Making Batteries Last Longer with Fast, High-Precision SAR Analog-to-Digital Converters

By Shane O'Meara

Low power consumption is a key requirement for today's battery-powered analog-to-digital converter applications, as portable handheld instruments for the medical, consumer, and industrial markets trend towards reduced size and weight, longer operating time per battery (or per battery charge), and lower cost, often accompanied by an increased feature set. The benefits of low power, even in non-battery-powered applications, should not be overlooked because low power systems can operate without heat sinks or fans, making them smaller, lower cost, more reliable—and "greener." In addition, many designers are faced with the challenge of designing products with enhanced features or performance while reducing, or at least not exceeding, existing power budgets.

The huge selection of ADCs on the market today makes choosing the best part to meet specific system requirements ever more challenging. Besides evaluating common converter performance characteristics, such as speed and accuracy, even more specifications need to be considered if low power is a must. Understanding these specifications and how design decisions affect the power budget is essential for determining system power consumption and battery life calculations.

The average power consumption for an ADC is a function of the power used during conversion, the power used while not converting, and the amount of time spent in each mode. This can be expressed by Equation 1.

$$P_{AVG} = (P_{CONV} \times \frac{t_{CONV}}{t_{CONV} + t_{STBY}}) + (P_{STBY} \times \frac{t_{STBY}}{t_{CONV} + t_{STBY}}) \quad (1)$$

P_{AVG} = average power dissipated.

P_{CONV} = power dissipated during conversion.

P_{STBY} = power dissipated during standby or shutdown mode.

t_{CONV} = time spent converting.

t_{STBY} = time spent in standby or power-down mode.

The power used during conversion is usually much greater than the standby power, so the average power can be greatly reduced if the time in standby mode is increased. Successive-approximation (SAR) converter types are particularly amenable to such modes of operation.

One of the biggest factors affecting system power usage is the choice of on-board power supplies. For portable applications, the system will often be powered directly by a 3-V lithium coin cell. This avoids the need for a low dropout voltage regulator, thus saving on power, space, and cost. Nonbattery applications also benefit from converters that have low V_{DD} supply ranges, as power consumption scales with input voltage. Choosing the lowest acceptable V_{DD} for the ADC will result in lower power consumption.

All ADCs that are targeted at low power applications have power-down or standby modes to conserve energy during periods of inactivity. The ADC can be powered down between single conversions, or a burst of conversions can be performed at a high throughput rate, with the ADC powered down between these bursts. For single-channel converters, control of the operating modes can be integrated into the communication interface or can occur automatically once a conversion is complete.

The advantage of integrating the mode control into the communication interface is a reduced pin count. This results in lower power consumption, as there are fewer inputs to drive and less leakage current. Smaller pin counts also lead to smaller package sizes and less I/O required by the MCU. Whatever the control method, careful use of these modes will provide considerable power savings.

Power is reduced in power-down modes, as the name suggests, by turning off parts of the ADC's circuitry. The time required for the circuitry that was shut down to restart conversion determines the throughput rate at which such modes can be used effectively. For an ADC with an internal reference, the restart time will be determined by the time taken to recharge the reference capacitor. Analog-to-digital converters using an external reference require enough time to track the analog input correctly on restart.

For all ADCs on the market today, power scales with throughput. The power consumed is a combination of static and dynamic power. Static power is constant, while the dynamic power scales linearly with throughput. Power savings will, therefore, be made by choosing the lowest possible throughput rate to suit the application.

Figure 1 shows the typical power consumption for the AD7091R, the most recent ultralow power ADC from Analog Devices, as a function of throughput rate. It also shows a comparison of how utilizing the device's power-down mode can provide additional power savings, especially with lower throughput rates. The throughput rate and utilization of the power-down mode of the AD7091R is determined by the device restart time and, as the AD7091R has an on-chip reference, the reference capacitor recharge time. The time it takes to recharge the reference capacitor depends on the capacitance and the level of charge remaining on the capacitor when the on-chip reference restarts.

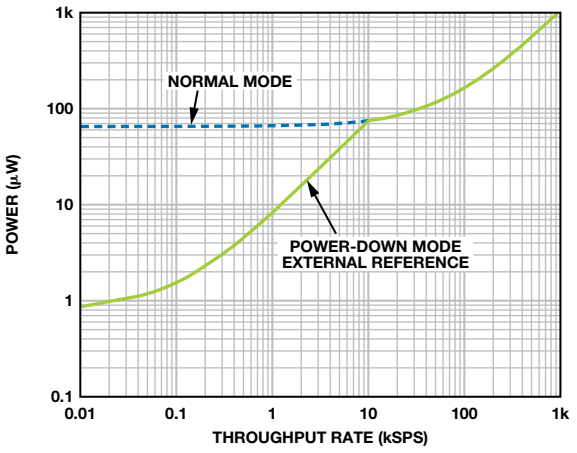

Figure 1. Power vs. throughput for the AD7091R ADC.

The most common methods to initiate conversion requests in ADCs are a dedicated conversion input pin or control via the serial interface. With a dedicated input pin ($\overline{\text{CONVST}}$), a conversion is initiated by a falling edge. The conversion is then controlled by an on-chip oscillator, and the result can be read back via the serial interface once the conversion is complete. Therefore, the conversion is always run at a constant optimum speed, allowing the device to enter low power mode the moment a conversion is complete, thus saving power.

With ADCs where the sampling instant is initiated by a falling edge on chip select ($\overline{\text{CS}}$), the conversion is controlled by the internal sampling clock (SCLK) signal. The SCLK frequency will affect the conversion time and the achievable throughput rate—and, therefore, the power consumption. The faster the SCLK rate, the shorter the conversion time. With shorter conversion time, the proportion of time available for the device to be in low power mode increases compared to normal mode; therefore, significant power savings can be achieved. That is, if each conversion requires N cycles of the SCLK, then for S conversions per second, the total time the SCLK is switching is $S \times N/f_{SCLK}$, and the quiescent time per second is shown in Equation 2.

$$(1.00 - \frac{S \times N}{f_{SCLK}}) \quad (2)$$

Thus, for a given number of samples per second, as f_{SCLK} increases, the quiescent time per second also increases.

For example, assuming 16 SCLK cycles to complete a conversion and read the results, a system sampling at 100 kSPS with a 30 MHz SCLK will be quiescent 94.67% of the time, that is, it will spend 5.33% of the time converting (53.3 ms per second). The same system operating with a 10-MHz SCLK will be quiescent only 84% of the time, that is, it will spend 160 ms converting. Therefore, to achieve the optimum power consumption, the converter should be operated at the highest allowable SCLK frequency.

An important but frequently overlooked parameter when designing for low power is the capacitive load seen at the output pins, especially the communication interface pins, such as SCLK, $\overline{\text{CS}}$, and SDO, as these I/O variables are constantly changing state during the conversion process. The capacitive load seen at an output is the pin capacitance of the driver IC itself, plus the pin capacitance of the input pin, plus the PCB trace capacitance. The trace capacitance can generally be kept small, in the femtofarad range, and is not significant. The power required to charge a capacitive load (P_L) is a function of the load (C_L), the drive voltage (V_{DRIVE}), and the frequency of change (f), as defined by Equation 3.

$$P_L = C_L \times V_{DRIVE}^{\ 2} \times f \quad (3)$$

The power for a complete system is, therefore, the sum of the products of the load capacitance (C_{Ln}) times the switching frequency (f_n) multiplied by the square of the drive voltage.

$$P_L = \sum (C_{Ln} \times f_n) \times V_{DRIVE}^{\ 2} \quad (4)$$

As the ADC drives the SDO pin, and the host microcontroller drives the $\overline{\text{CS}}$, $\overline{\text{CONVST}}$, and SCLK pins, the lowest power consumption will be achieved by minimizing pin capacitance for all devices.

For the $\overline{\text{CS}}$ and $\overline{\text{CONVST}}$ pins, the switching frequency is determined solely by the throughput rate. The SCLK frequency, as already discussed, should be set to the maximum allowable frequency to reduce power. This is not a contradiction: the important point is that the SCLK is not free running—it should be active for only the minimum possible time to propagate the result on the SDO line for each bit trial and to control the conversion process. This is device- and resolution dependent but is typically one cycle per bit, plus some overhead, or about 16 SCLK cycles per sample for 12-bit converter SPI interfaces. The minimum frequency for the SCLK is, therefore, the number of cycles required multiplied by the throughput rate.

The frequency of the SDO line depends on both the throughput rate and the conversion result. While this is not controllable, designers should understand how it can affect power consumption for a conversion. The highest power consumption will occur when the result is a 101010… sequence; the lowest will occur when the result is all 1s or all 0s.

Besides lower throughput rate, decreased V_{DRIVE} voltage will also reduce power consumption considerably. Analog-to-digital converters have either a single-supply pin or separate supplies for the analog circuitry and digital interface. A separate V_{DRIVE} supply gives more design flexibility and avoids the need for level shifters, as the analog-to-digital interface voltage can be matched to that of the SPI master. Choosing the lowest voltage available for V_{DRIVE} will correspond to the lowest system power consumption.

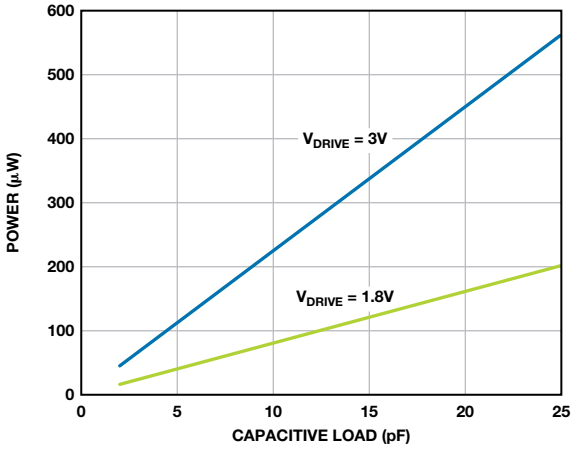

Figure 2. Typical interface power consumption vs. capacitive load.

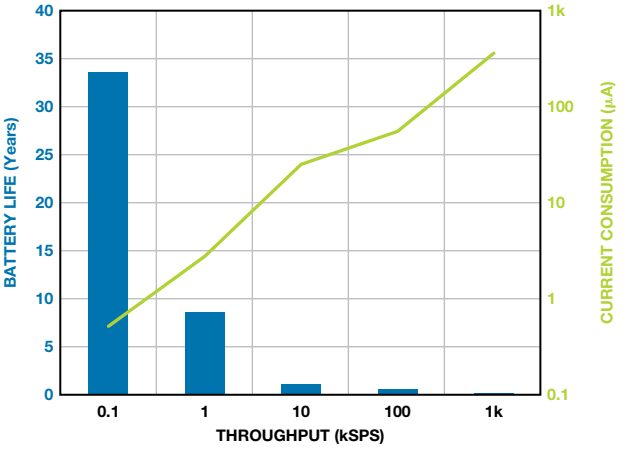

Figure 3. Battery life and current consumption vs. throughput for the AD7091R.

Figure 2 compares the typical power requirement of a standard SPI interface—with $\overline{CS}$, SDO, and SCLK—as a function of total capacitive load for V_{DRIVE} values of 3 V and 1.8 V, throughput rate of 100 kSPS, 16 SCLK cycles per conversion, and a worst case SDO output of 1010… for a 12-bit ADC.

Other typical constituents of an ADC circuit design are a voltage reference and an operational amplifier. It goes without saying that these components should also be chosen carefully for low power. Some references are available with power-down modes to reduce consumption during periods of inactivity. The choice of amplifier is application dependent, so the system throughput rate should be considered to ensure that the chosen amplifier maximizes the ADC performance and minimizes power consumption.

The 12-bit AD7091R, specifically designed for low power applications, features an SPI interface, an on-chip precision 2.5-V voltage reference, and a 1-MSPS sampling rate. Conversions are initiated via a $\overline{CONVST}$ pin. An on-chip oscillator controls the conversion process, making it possible to optimize power consumption. The pin capacitance is a low 5 pF maximum. A wide input voltage range (2.7 V to 5.25 V) allows for integration into a wider range of applications than just battery-powered ones. A separate V_{DRIVE} supply of 1.65 V to 5.25 V allows for reduced power and greater system integration capabilities.

When operating at 1 MSPS, the AD7091R draws 349 µA typical at 3-V V_{DD}. Since its power scales with throughput, 55-µA quiescent current is achievable at 100 kSPS. Static current when not converting, but with the reference active, is 21.6 µA; in power-down mode, only 264 nA is drawn. The AD7091R is available in 10-lead MSOP or LFCSP packages.

Typical amplifiers to drive the AD7091R would include the AD8031—for fast throughput applications—and the AD8420 for lower bandwidth applications. The quiescent current consumption of the AD8031 is 750 µA typical with a 2.7-V supply; that of the AD8420 is 70 µA typical when used with a 5-V supply.

Figure 3 shows typical current consumption and calculated battery life for the AD7091R when supplied via a CR2032 lithium battery. It can be clearly seen that as throughput decreases, battery life can be greatly extended.

When the AD7091R is compared to most other ADCs, significant savings can be achieved in the power budget. For example, when matched against the nearest available competition, a part with no internal reference, for a 1-MSPS throughput rate, the AD7091R achieves better than a 3× reduction in power consumption (1 mW typical compared to 3.9 mW typical for a 3-V supply). This corresponds to extending the battery life of a CR2032 battery by 400 hours. When the other device's need for an external voltage reference is taken into account, the savings are further increased.

Conclusion

There are many benefits of reduced power consumption other than increased battery life. Less heat is generated, which leads to smaller form factors. Reliability improves due to the lower temperature stress. System costs can be lowered, as PCB size can be reduced due to the smaller components—with a reduction in number of components, as there is no need for such accessories as heat sinks.

This article has outlined several important considerations and advantages that the system designer should take into account regarding optimization of power consumption in their designs employing ADCs.

References

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Author

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Diagnostic Technique Detects Open and Short Circuits in Wiring Harnesses

By Don Nisbett

As a vital part of modern cars, wiring harnesses containing thousands of assembly components connect various electronic systems, enabling them to work together. A single failure in any harness can affect the entire system. Nevertheless, to accommodate the growing demand for in-car electronics, the complexity of automotive wiring harnesses continues to grow, increasing the need to detect broken or shorted wires quickly and easily. Wire diagnostics are important throughout the entire life of the car. Starting with the installation phase, diagnosing and repairing wiring faults can cause extensive manufacturing delays. During the operational phase, diagnosing and repairing wiring faults can cause prolonged visits to the repair shop, adding significant costs to manufacturers in the form of warranty repairs.

Active safety systems, including lane detection and parking assist (front and rearview cameras)—and infotainment systems, including navigation and rear seat entertainment—are some of the more highly sought automotive electronics systems. For these systems to be effective, video data transmitted via cable from all corners of the car must reliably get to the driver and passengers. Cable health is crucial for maintaining proper operation of these systems.

This article offers a circuit idea that provides a robust, cost-effective technique for implementing wire diagnostics on the video and audio transmission lines in automotive applications.

The circuit shown in Figure 1 can effectively detect short-to-battery (STB), short-to-ground (STG), open-circuit, and short-circuit faults. The circuit uses an ADA4433-1 (U1) fully integrated video reconstruction filter as part of the video transmission signal chain and an ADA4830-1 (U2) high-speed difference amplifier as the detection circuit. The ADA4433-1 features a high-order filter with a −3-dB cutoff frequency of 10 MHz, 45-dB rejection at 27 MHz, and an internally fixed gain of 2 V/V. It has excellent video specifications, overvoltage protection (STB) and overcurrent protection (STG) on its outputs, and low power consumption. The ADA4830-1 provides an attenuating gain of 0.50 V/V and a fault detection output flag that can indicate the presence of an overvoltage condition on its inputs. It features input overvoltage protection of up to 18 V, a wide common-mode input voltage range, and excellent ESD robustness.

In the example circuit shown in Figure 1, U1 represents the differential output buffer that transmits the video signal from a rearview camera or engine control unit (ECU) to the receiver. The input would typically be driven by a CMOS imager or video encoder. The primary function of U1 is to provide the active filtering function (reconstruction) and to drive the video signal through the cable to the display. The inputs of U2 are connected across the outputs of U1 to provide the fault detection features listed in Table 1 and described in the following paragraphs.

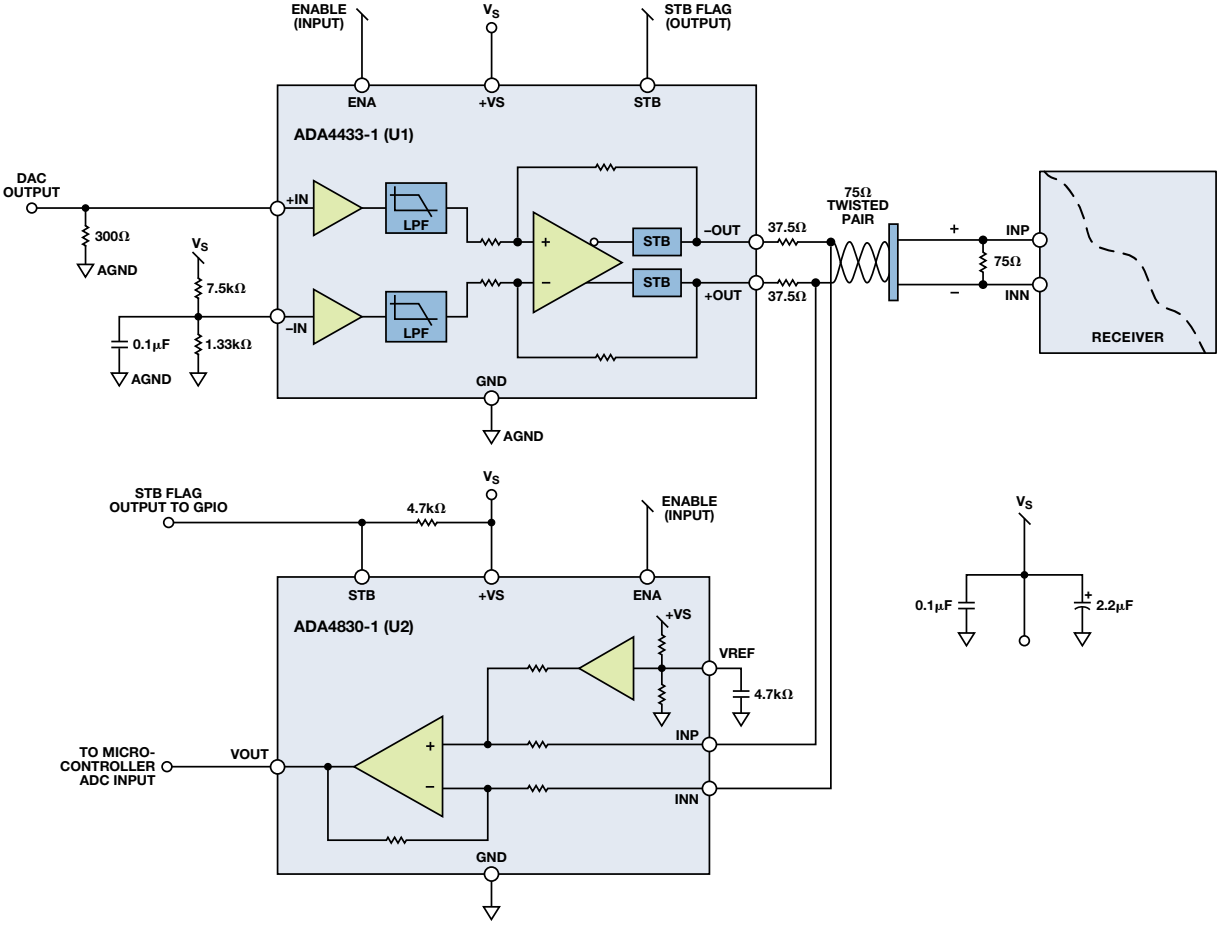

Figure 1. Wire diagnostic circuit using the ADA4433-1 (U1) and ADA4830-1 (U2).

(continued on Page 23)

Analyzing Frequency Response of Inertial MEMS in Stabilization Systems

By Mark Looney

Introduction to Stabilization Systems

UAV-mounted surveillance equipment, maritime microwave receivers, vehicle-mounted infrared imaging sensors, and similar instrument systems require stable platforms for best performance, but they are often used in applications that experience vibration and other undesirable kinds of motion. Vibration and normal vehicular movements cause communication loss, blurry images, and many other behaviors that degrade the instrument's performance and ability to perform its desired function. *Platform stabilization systems* employ closed-loop control systems to actively cancel this type of motion, thus preserving mission-critical performance objectives for these instruments. Figure 1 is a generic block diagram of a platform stabilization system that uses servo motors to correct for angular motion. The feedback sensor provides dynamic orientation information for the instrument platform. The feedback controller processes this information and translates it into corrective control signals for the servo motors.

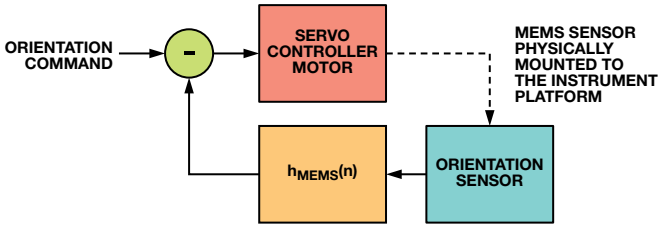

Figure 1. Basic platform stabilization system.

Since many stabilization systems require more than one axis of active correction, *inertial measurement units* (IMUs) often include at least three axes of gyroscopes (measuring angular velocity) and three axes of accelerometers (measuring acceleration and angular orientation) to provide the feedback sensing function. The ultimate goal of the feedback sensor is to provide accurate measurements of the platform's orientation, even when it is in motion. Since there is no "perfect" sensor technology that can provide accurate angle measurements under all conditions, the IMUs in platform stabilization systems often employ two or three sensor types on each axis.

An accelerometer responds to both *static* and *dynamic acceleration* in the direction of each of its axes. "Static acceleration" may seem like a strange term, but it encompasses an important sensor behavior: response to gravity. Assuming that no dynamic acceleration exists, and that sensor errors have been removed through calibration, each accelerometer output will represent the orientation of its axis, with respect to gravity. To determine the actual average orientation in the presence of the vibration and rapid acceleration often experienced in stabilization systems, *filters* and *fusion routines* (combining readings from multiple sensor types to obtain a best estimate) are often applied to the raw measurements.

Another type of sensor is the *gyroscope*, which provides angular rate measurements. Gyroscope measurements contribute to the angle measurements through integration of the angular-rate over finite time periods. When performing integration, bias errors will cause a proportional angle drift that accumulates with respect to time. Therefore, gyroscope performance often relates to the sensitivity of a device's bias to different environmental factors, such as temperature variation, supply variation, off-axis rotation, and linear acceleration (linear-g and rectified-$g \times g$). A calibrated high-quality gyroscope, with high rejection of linear acceleration, enables these devices to provide wideband angle information to complement the low-frequency information provided by accelerometers.

A third type of sensor is the 3-axis *magnetometer*, which measures magnetic field intensity. Magnetic field measurements from three orthogonal axes enable estimates of orientation angle, with respect to the local direction of the earth's magnetic field. When the magnetometer is near motors, monitors, and other sources of dynamic field disturbance, managing its accuracy can be challenging, but in the right circumstances its angular data can augment the measurements from accelerometers and gyroscopes. While many systems use only accelerometers and gyroscopes, magnetometers can improve measurement accuracy in some systems.

The generic block diagram of Figure 2 shows how gyroscope and accelerometer measurements can be employed in a manner that uses their basic strengths but minimizes the impact of their weaknesses. The pole locations of the low-pass accelerometer and high-pass gyroscope filters are typically application-dependent, with accuracy goals, phase delay, vibration, and "normal" motion expectations, all contributing to these decisions. System-dependent behaviors will also affect the weighting factors, which also have an impact on how these two measurements are combined. The extended Kalman filter is one example of an algorithm that combines the filtering and weighting functions to calculate dynamic angle estimates.

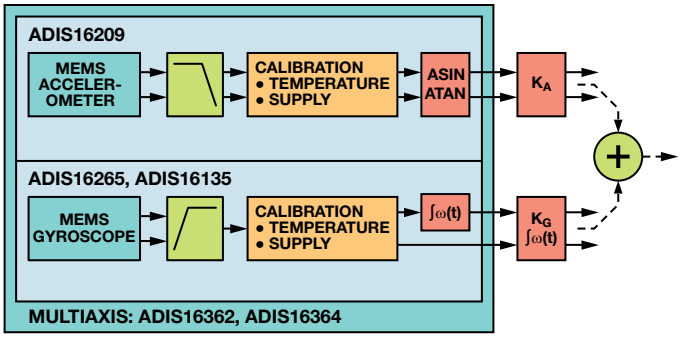

Figure 2. Combining single-axis sensor outputs.

MEMS IMU Frequency Response Analysis

When developing a stabilization system around a new MEMS IMU, it is important to understand the frequency response in the early stages of system design, since the IMU's frequency response will have a direct impact on the controller design and can help identify potential stability issues—especially when considering wider-bandwidth solutions for next generation designs. This information is also useful for predicting the gyroscopes' responses to vibration.

A strategy for evaluating IMU bandwidth is determining what information is available in product documentation, analyzing the impact of this information on the system's response to inertial motion, and stabilizing the system's response. This analysis, and any corrective actions it entails, will become the basis for preliminary testing.

Frequency response is often represented as "bandwidth" in specification tables for IMUs and gyroscopes. As a performance parameter, it represents the frequency at which the output magnitude drops to about 70% (–3 dB) of the actual magnitude of motion that the sensor is experiencing. In some cases, bandwidth may also be defined by the frequency at which the output response lags the actual motion by 90 degrees (for a 2-pole system). Both of these metrics can directly impact an important stability criterion for a control loop: *unity-gain phase margin*—the difference between the actual phase angle of the loop response and –180° at a loop gain of 1. Understanding the frequency response of the feedback sensor is a key factor in optimizing the trade-off between stability assurance and system response. In addition to managing stability criteria, the frequency response also has a direct impact on vibration rejection and establishing a sampling strategy that allows all critical transient information on an inertial platform to be measured.

Analyzing frequency response in a system starts with a high-level, "black box" view, which describes the system's response to inputs over the entire frequency range of interest. In electronic circuits, where the input and output are defined in common terms, such as signal level (volts), this typically involves developing a *transfer function,* using *s*-domain representation and circuit-level relationships, such as Kirchhoff's voltage and current laws. For an inertial MEMS system, the input is the inertial motion that the IMU experiences, and the outputs are often represented by digital codes. While *s*-domain analysis techniques are valuable, developing a complete transfer function for this type of system often requires additional techniques and consideration.

The analysis process starts with understanding all of the components associated with a sensor signal chain. Figure 3 offers an overall diagram of the typical functions. The signal chain starts with a core sensor element, which translates the inertial motion into a representative electrical signal. If the bandwidth is not limited in the sensor element, it is often limited by filters in the signal-conditioning circuit preceding the ADC. After the signals are digitized, a processor typically applies correction (calibration) formulas and digital filtering. The secondary digital filters reduce the bandwidth and sample rates that the feedback systems use in their control routines. All of these stages can influence the gain and phase of the sensor signal, with respect to frequency. Figure 3 provides an example of an IMU that has multiple filters in a mixed-signal processing system. This system will serve as an example for illustrating some useful analysis techniques.

Core MEMS Sensor Element

This analysis is driven by the understanding that all behaviors that can be quantified, should be; then, educated assumptions can be made on those things that cannot be easily quantified. Once the "known" variables are well-understood, it is often easier to revisit these assumptions for review and clarification. The specification table for the ADIS16488 (Figure 3) shows a –3-dB bandwidth of 330 Hz. Assume that the core sensor is critically damped and is not a key contributor at bandwidths well below its resonance (16 kHz to 20 kHz). This may not always be the case, but it is a good starting point that can be tested later in the process using noise-density or full-motion tests.

Interface Circuit/Analog Filter

In addition, each gyroscope sensor goes through a 2-pole, low-pass filter prior to the ADC. This provides enough information to use Laplace transforms to develop a transfer function representation in the *s*-domain. The first pole (f_1) is at 404 Hz, and the second pole (f_2) is at 757 Hz.

$$H_G(s) = \frac{\omega_1}{s+\omega_1} \times \frac{\omega_2}{s+\omega_2} = \frac{808\pi}{s+808\pi} \times \frac{1514\pi}{s+1514\pi}$$

$$\text{Magnitude} = |H_G(s)|_{s=j\omega}$$

$$\text{Phase} = \arctan(H_G(s))_{s=j\omega}$$

$$f_1 = 404\ Hz, \text{ filter pole \#1}$$

$$\omega_1 = 2\pi f_1 = 808\pi$$

$$f_2 = 757\ Hz, \text{ filter pole \#2}$$

$$\omega_2 = 2\pi f_2 = 1514\pi$$

The accelerometer's single-pole (f_1) transfer function is.

$$H_A(s) = \frac{\omega_1}{s+\omega_1} = \frac{660\pi}{s+808\pi}$$

$$\text{Magnitude} = |H_A(s)|_{s=j\omega}$$

$$\text{Phase} = \arctan(H_A(s))_{s=j\omega}$$

$$f_1 = 330\ Hz, \text{ filter pole \#1}$$

$$\omega_1 = 2\pi f_1 = 660\pi$$

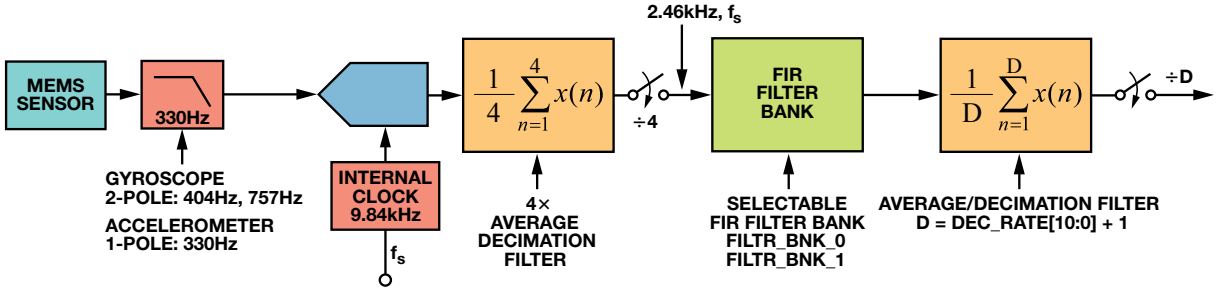

Figure 3. ADIS16488 sensor in a signal chain for frequency analysis.

These formulas provide the basis for numerical analysis in programs that can manage the complex numbers associated with the "$s = j\omega$" identity. In MATLAB, the following *m*-script will produce both magnitude (ratio, no units) and phase (degrees) information:

```
Fmax = 9840/2; % one-half of the sample rate
for f = 1:Fmax
 w(f) = 2*pi*f;
end
p1 = 404; % pole location = 404Hz
p2 = 757; % pole location = 757Hz
NUM1 = 2*pi*p1;
DEN1 = [1 2*pi*p1];
NUM2 = 2*pi*p2;
DEN2 = [1 2*pi*p2];
H1 = tf(NUM1,DEN1); % transfer function for first pole
H2 = tf(NUM2,DEN2); % transfer function for second pole
H488a = H1 * H2; % transfer function for 2-pole filter
[maga,phasea] = bode(H488,w);
for f = 1:Fmax
 Mag488a(f) = maga(1,1,f);
 Phase488a(f) = phasea(1,1,f);
end
```

For a quick assessment of the time delay associated with these filters, notice that the phase delay of a single-pole filter is equal to 45° at its −3-dB frequency, or $^1/_8$ of the corner frequency's period. In this case, the time delay of the accelerometer's filter is approximately equal to 0.38 ms. For the gyroscope, the delay is equal to the sum of the time delays of the two stages, or about 0.47 ms.

$$t_A = \frac{45}{360} \times \frac{1}{330\ Hz} = 0.38\ ms$$

$$t_G = \frac{45}{360} \times \left(\frac{1}{404\ Hz} + \frac{1}{757\ Hz} \right) = 0.47\ ms$$

Averaging/Decimating Filter Stage

Figure 3 illustrates the use of two averaging/decimating filter stages, which lower the stage's output sample rate and provide additional filtering. In digital filters that have a *finite impulse response* (FIR), the phase delay is equal to one-half of the total number of taps, divided by the sample rate of each tap. In the first filtering stage, the sample rate is 9.84 kHz. There are four taps, which, in this style of filter, is equal to the number of averages. The phase delay is approximately 0.2 ms. The magnitude response of the averaging filter follows this relationship.

$$H(f) = \left| \frac{\sin\left(4 \times \pi \times f / 9840\right)}{4 \times \sin\left(\pi \times f / 9840\right)} \right|$$

When using MATLAB for analysis, use a sample rate (f_s) of 9.84 kSPS and four taps (N), along with the same frequency array (f) used to analyze the analog filter. Using a common frequency array will make it easier to combine the results of each stage. Use the following code to analyze this first stage:

```
Fmax = 9840/2; % one-half of the sample rate
f = 1:Fmax;
NUM(f) = sin(4*pi*f/9840);
DEN(f) = 4 * sin(pi*f/9840);
for fq = 1:Fmax
 Hda(fq) = abs(NUM(fq)/DEN(fq));
end
```

Analyzing the second averaging/decimating filter will require prior knowledge of the control system's sample rate but will use the same relationships. For example, if a control loop requires a sample rate that is close to 400 SPS, the second filter's average and decimation rate would be equal to six (for a sample rate of 410 SPS and four samples, 9840/[410 × 4] = 6). Use the same *m*-script code to analyze the magnitude response, with three exceptions: (1) change the sample rate from 9480 to 2460, (2) change the "4" to "6" in both locations, and (3) change F_{MAX} from 9840/2 to 2460/2. The phase is equal to one-half of the total number of taps, divided by the sample rate, approximately 1.22 ms (3/2460).

Composite Response

Figure 4 and Figure 5 provide the composite magnitude and phase response, which includes the gyroscope's analog filters and the two decimation filters. Figure 4 represents the result of multiplying the stages' magnitudes together, for each frequency in the array. Figure 5 represents the result of adding the stages' phase contributions together at each frequency. The plot labeled "Without Decimation" assumes that the output data rate is 2460 SPS and that the second decimation stage is effectively turned off. The plot labeled "With Decimation" assumes that the decimation rate is equal to 6 and that the final output data rate is 410 SPS. These two plots illustrate the difference in response for system-level trade-offs between control loop sample rate and the corresponding frequency response.

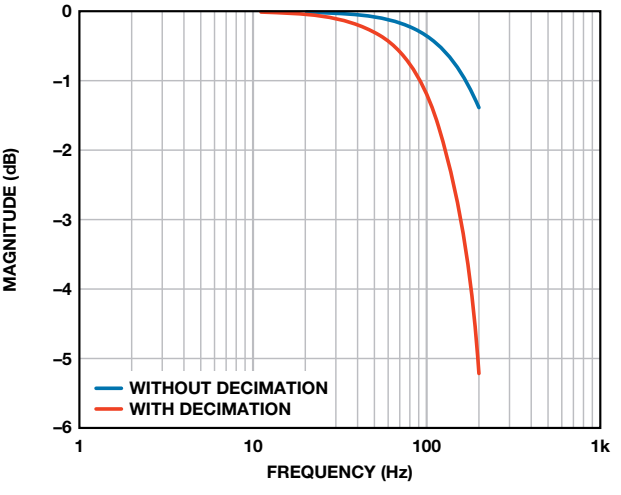

Figure 4. Analog filter and first decimation stage.

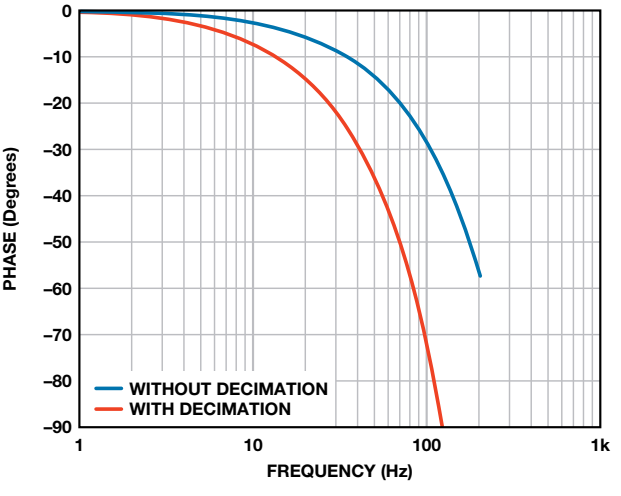

Figure 5. Composite response for 410-SPS data rate.

Programmable FIR Filter Analysis

Once the contributions of the analog and decimation filters are known, the trade-offs between using the on-board decimation filter and designing a custom FIR filter can be evaluated. In the ADIS16488, outlined in Figure 3, the FIR filter is included with the IMU, but some systems will implement this in their digital signal processing routines. A FIR filter's time-domain $f(n)$ representation is often expressed by a *difference equation*, where the z-transform offers an analytical tool for frequency analysis:

$$y(n) = \sum_{m=0}^{M-1} a_m \times x(n-m)$$

$$H(z) = \frac{Y(n)}{X(n)} = \sum_{m=0}^{M} a_m \times z^{-k}$$

$$z = e^{sT}$$

$$s = j\omega$$

Fortunately, many modern programs contain specific tools or commands for this type of analysis, based on these basic relationships. It is still useful to understand them when verifying results of the automatic assessment tools and in developing an intuitive feel for when to question the outputs of a FIR design tool. The MATLAB "fdatool" command launches its filter analysis and design package, which helps design and analyze the system FIR filter implementation.

Inertial Frequency Response Test Methods

The most direct approach for testing frequency response in a gyroscope is with an inertial rate table, which is capable of introducing the appropriate frequency content. Rate tables typically include a programmable servo motor and an optical encoder that verifies programmed rotation on the motor shaft. The advantage of this test approach is that it applies actual inertial motion. Its disadvantage is that it is not commonly available for engineers who are just getting started with MEMS.

For early analysis validation without a rate table, measuring the spectral noise over the frequency band of interest can provide useful insights. This simplified approach does not require sophisticated test equipment but only a secure mechanical connection to a stable platform and data collection instrumentation. However, it does rely on the mechanical noise having a "flat" noise magnitude with respect to frequency.

Figure 6 illustrates two examples that both use the same 2-pole, low-pass filter. The first example (ADIS16375) uses a gyroscope that has a flat response over its usable frequency range. The second example (ADIS16488) uses a gyroscope that has a modest amount of peaking at 1.2 kHz, which actually extends the –3-dB frequency to approximately 380 Hz. Recognizing this resonant behavior can be valuable for those in the process of modeling and simulating a control loop. Identifying this behavior in a simple test can also help explain noise levels that are higher than expected when performing a more thorough system characterization. When understood and identified early in a project, these behaviors can normally be managed with adjustments to the filter poles.

When measuring noise density, make sure that the sample rate is at least twice the highest frequency of interest to meet the Nyquist criterion. Also, take enough data samples to reduce the uncertainty of the measurements. The plots in Figure 6 were derived from FFT analysis of a time record with a length of 256k samples at a maximum rate of 2.46 kSPS.

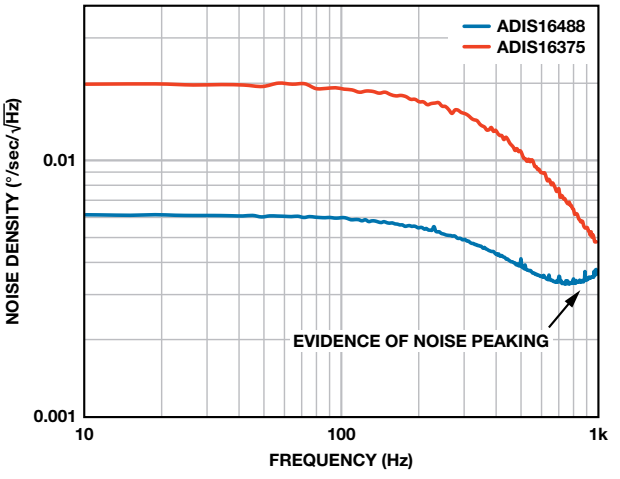

Figure 6. Noise density comparison.

Another approach uses a gyroscope's self-test function. The self-test function provides an opportunity to stimulate the sensor's mechanical structure, using an electrical signal, without requiring the device to be subjected to external inertial motion. The self-test function forces a change in the sensor core that simulates its response to actual motion, producing a corresponding change in the electrical output. Not all products provide real-time access to this, but it can be a useful tool when available, or if the manufacturer can provide data from this type of frequency-response test. In the simplest approach, the self-test, which simulates response to a step, is compared with the analytical expectation. Repeating the self-test assertion at specific frequencies provides a direct method for studying the magnitude of the sensor response at each frequency. Consider the two different responses in Figure 7. At the lower frequency, the gyroscope output looks like a square wave, with the exception of the transient response at each transition. The transient response follows the expectation of a "step response" for the filter network in the sensor signal chain. In the second example, where the frequency of the self-test is high enough to prevent full settling, a decrease in magnitude occurs. Notice the difference in magnitudes between the blue and black-dotted responses, on the bottom signal in this figure. There are a number of methods for estimating the magnitude

of these time records. A discrete Fourier transform (DFT) separates the primary frequency content (self-test frequency) from the harmonic content, which can contribute errors to the magnitude/frequency response.

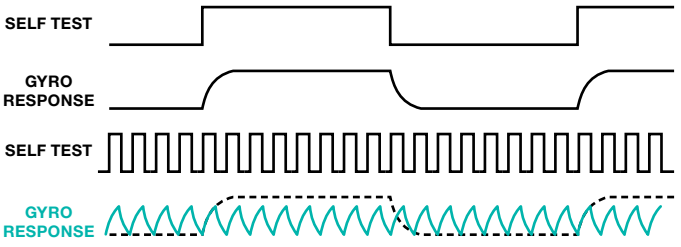

Figure 7. Self test.

Conclusion

A trend towards wider-bandwidth IMUs provides significant advantages in design of feedback stabilization systems. The wider bandwidth enables better time alignment and phase margin management for multisensor systems. Filter capacitors can have a wide variation in their value and response to temperature, which can cause proportional changes in the pole frequencies. Since the phase delay is dependent on the pole location, understanding and managing this can be very important. For example, when the feedback sensor's cut-off frequency is two times greater than the unity-gain feedback of the controller, it will add approximately 22.3° of phase delay to the loop response. If the cut-off frequency decreases by 20%, the phase delay increases by approximately 5.6°. Increasing the ratio of cut-off frequency in a unity gain bandwidth reduces these influences by a factor of 4.

Developing an understanding of an IMU's bandwidth and its role in system stability should employ analysis, modeling, test data, and iteration of these factors. Start by quantifying the information available, make assumptions to close any gaps, and then develop a plan to refine these assumptions.

For More Information

- MEMS Inertial Sensors
- WEBCAST: Using MEMS Sensors for Industrial Platform Stabilization Systems
- The Five Motion Senses: Using MEMS Inertial Sensing to Transform Applications
- Improving Industrial Control with Integrated MEMS Inertial Sensors

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(continued from Page 18)

Short-to-Battery Fault Detection

Both U1 and U2 have integrated short-to-battery detection and an STB output flag. During a short-to-battery event, the output flag of U2 will signal a logic *low* that can be easily read by a microcontroller's general-purpose input/output (GPIO) port.

Short-to-Ground Fault Detection (Single Output)

Connect the positive input (INP) of U1 to the negative input (INN). The differential output between +OUT and −OUT should be 0 V. If either output is shorted to ground, the differential voltage at the output of U2 will be greater than 500 mV.

Short-to-Ground Fault Detection (Both Outputs)

Set the positive input (INP) of U1 to 0 V. The differential output between +OUT and −OUT should be approximately 1 V. If both outputs are shorted to ground, the differential voltage at the output of U2 will be approximately 0 V.

Open Circuit

Set the positive input (INP) of U1 to 0 V. The differential output between +OUT and −OUT should be approximately 1 V. If there is an open connection, the resulting differential voltage at the output of U2 will be approximately 500 mV.

Short to Adjacent Output

Set the positive input (INP) of U1 to 0 V. The differential output between +OUT and −OUT should be approximately 1 V. If both outputs are shorted together, the differential voltage at the output of U2 will be approximately 0 V.

Normal Operation (No Cable Faults)

Set the positive input (INP) of U1 to 0 V. The resulting differential output between +OUT and −OUT should be approximately 1 V. The resulting differential voltage at the output of U2 will be approximately 250 mV.

Author

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Table 1. Summary of Diagnostic Output Indicators

Fault Condition	U1 Input Configuration	U2 Output Indicator	Voltage Level at Indicator[1]
Short to Battery		Pin 5	85 mV
Short to Ground (Single Output)	INP = INN	Pin 6	530 mV
Short to Ground (Both Outputs)	INP ≠ INN	Pin 6	10 mV
Open Circuit	INP ≠ INN	Pin 6	500 mV
Short to Adjacent Output	INP ≠ INN	Pin 6	0 mV
Normal Operation (No Cable Faults)		Pin 6	250 mV

[1] *All voltage levels are approximate and should be characterized for a particular design.*

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