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Analog Dialogue

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ANALOG DEVICES

Editors' Notes

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Many industries need electronics that can operate reliably in harsh environments, including extremely high temperatures. Traditionally, engineers had to rely on active or passive cooling when designing electronics that must function outside of normal temperature ranges, but cooling may not be possible in some applications, or its high cost and low reliability may make it undesirable in others. Page 3.

Simple Circuit Provides Adjustable CAN-Level Differential-Output Signal

The *controller area network* (CAN) serial-bus topology allows devices and microcontrollers to communicate with each other without a host computer. Featuring arbitration-free transmission, it places a controller and a host processor at each device node, eliminating the more complex wiring harness that would be necessary to interconnect devices with a host computer. Page 10.

ADI Capacitance-to-Digital Converter Technology in Healthcare Applications

Recent advances in technology have enabled many innovations in the healthcare industry. Challenges for healthcare equipment include developing new diagnostic methods, simplifying remote monitoring and home healthcare, improving quality and reliability, and enhancing flexibility. *Capacitance-to-digital converter* technology brings high-performance capacitance sensing to healthcare applications. Page 11.

Understanding Microphone Sensitivity

Sensitivity, the ratio of the analog output voltage or digital output value to the input pressure, is a key specification of any microphone. This article will discuss the distinction in sensitivity specifications between analog and digital microphones, how to choose the best microphone for an application, how to get the fullest performance from that device, and why adding a bit (or more) of digital gain can enhance the microphone signal. Page 14.

Staying Well Grounded

Grounding is one of the most complex subjects in system design. Although the basic concepts are simple, implementation can be difficult. No single approach will guarantee good results, but a few things will probably cause headaches if not done well. This article presents a number of techniques, depending upon the particular mixed-signal devices used. When laying out the PC board, it is helpful to provide for as many options as possible. Page 17.

Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors

When using very low value current-sense resistors, the solder resistance becomes a substantial portion of the total resistance, adding to the measurement error. High-accuracy applications use 4-terminal resistors and Kelvin sensing, but this can be expensive. This article describes an approach that enables precision Kelvin sensing using a standard, low-cost, 2-pad sense resistor with a 4-pad layout. Page 25.

Dan Sheingold [dan.sheingold@analog.com]

Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 46, NUMBER 2

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

April

Amplifier, audio, 2 × 10-W, Class-D.....**SSM3302**
Amplifier, headphone, high-efficiency, Class-G.....**SSM2932**
Amplifier, instrumentation, micropower, rail-to-rail.....**AD8420**
Amplifier, variable-gain, dual, 1-MHz to 31-MHz **ADRF6516**
Demodulator, quadrature, 700-MHz to 1050-MHz.....**ADRF6807**
Driver, white LED, four-string, LCD backlight.....**ADD5207**
Energy Meter, one voltage- and six current channels.....**ADE7816**
Modems, HART, low-power.....**AD5700/AD5700-1**
Regulator, step-down, synchronous, dual 5-A, 20-V.....**ADP2325**
Transceivers, M-LVDS, 100-Mbps, half-/full-duplex.....**ADN4690E/ADN4692E**
VGAs, IF, cascadable, programmable rms detectors **ADL5336**

May

Amplifier, RF driver, 0.5-W, 400-MHz to 4000-MHz **ADL5324**
Controller, digital, isolated power supply.....**ADP1046**
DACs, quad, 16-/14-/12-bit, 2-ppm/°C reference.....**AD568xR/AD569xR**
Driver/Receiver, line, RS-232, 2-channel, isolated **ADM3252E**
Receiver, HDMI, quad, 12-bit, 170-MHz **ADV7844**
Transceivers, M-LVDS, 100-Mbps, half-/full-duplex.....**ADN4694E/ADN4695E**
Transceivers, M-LVDS, 200-Mbps, half-/full-duplex.....**ADN4691E/ADN4693E**

June

Amplifier, instrumentation, low-power, 3-nV/√Hz.....**AD8421**
Amplifier, JFET, dual, 17-MHz, rail-to-rail outputs.....**AD823A**
Amplifier, operational, quad, micropower, RRIO.....**AD8548**
Converters, dc-to-dc, step-down, 800-mA.....**ADP2370/ADP2371**
Driver, current/voltage, programmable, industrial.....**AD5750-2**
Driver, vertical, CCD cameras **ADDI9023**
Drivers, half-bridge, isolated, 4-A peak output.....**ADuM3223/ADuM4223**
Filter, video, SD, short-to-battery protection **ADA4433-1**
Isolators, digital, 2-channel, 1-kV rms isolation **ADuM7240/ADuM7241**
Isolators, digital, 2-channel, 3-kV rms isolation.....**ADuM128x**
Processor, SHARC **ADSP-21477**
References, voltage, high-accuracy, low-noise **ADR45xx**
Regulator, step-down, 6-A, 20-V, low-side driver.....**ADP2381**
Regulator, switching, isolated.....**ADuM3070**
Sensor, inertial, tactical-grade, six-DOF.....**ADIS16485**
Synthesizer, wideband, integrated VCO.....**ADF4351**

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High-Temperature Electronics Pose Design and Reliability Challenges

By Jeff Watson and Gustavo Castro

Introduction

Many industries are calling for electronics that can operate reliably in harsh environments, including extremely high temperatures. Traditionally, engineers had to rely on active or passive cooling when designing electronics that must function outside of normal temperature ranges, but in some applications, cooling may not be possible—or it may be more appealing for the electronics to operate hot to improve system reliability or reduce cost. This choice presents challenges that affect many aspects of the electronic system, including the silicon, packaging, qualification methodology, and design techniques.

High-Temperature Applications

The oldest, and currently largest, user of high-temperature electronics (>150°C) is the *downhole* oil and gas industry (Figure 1). In this application, the operating temperature is a function of the underground depth of the well. Worldwide, the typical geothermal gradient is 25°C/km depth, but in some areas, it is greater.

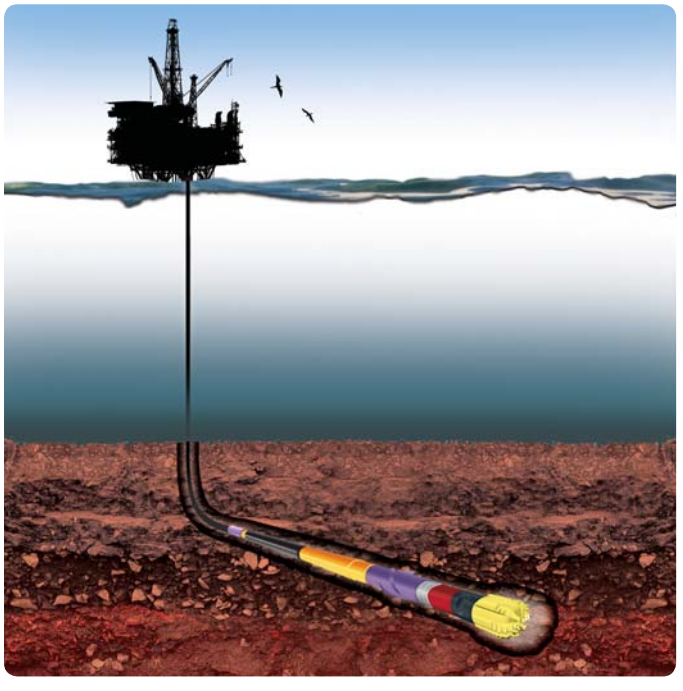


Figure 1. Downhole drilling operation.

In the past, drilling operations have maxed out at temperatures of 150°C to 175°C, but declining reserves of easily accessible natural resources coupled with advances in technology have motivated the industry to drill deeper, as well as in regions of the world with a higher geothermal gradient. Temperatures in these *hostile* wells can exceed 200°C, with pressures greater than 25 kpsi. Active cooling is not practical in this harsh environment, and passive cooling techniques are not effective when the heating is not confined to the electronics.

The applications for high-temperature electronics in the downhole industry can be quite complex. First, during a drilling operation, electronics and sensors steer the drilling equipment and monitor its health. With the advent of directional drilling technology, high-performance geosteering instrumentation must guide the borehole position to an exact geologic target.

While drilling, or soon thereafter, sophisticated downhole instruments acquire data about the surrounding geologic formations. This practice, known as *well logging*, measures resistivity, radioactivity, acoustic travel time, magnetic resonance, and other properties to determine characteristics of the formation, such as lithology, porosity, permeability, and water/hydrocarbon saturation. This data allows the geologist to make judgments about the types of rock in the formation, the types of fluids present and their location, and whether adequate amounts of hydrocarbons can actually be extracted from fluid-bearing zones.

Finally, during the completion and production phases, electronic systems monitor pressure, temperature, vibration, and multiphase flow—and actively control valves. Meeting these needs requires a complete signal chain of high-performance components (Figure 2). System reliability is of utmost importance, as the cost of downtime due to equipment failure can be quite severe. A failed electronics assembly on a drill string operating miles underground can take more than a day to retrieve and replace—and the rate for operating a complex deep-water offshore rig is of the order of $1M per day!

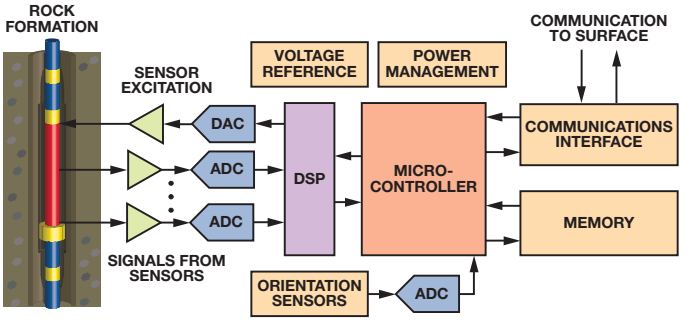


Figure 2. Simplified downhole logging instrumentation signal chain.

Other users: Besides the oil and gas industries, other applications, such as *avionics*, are emerging for high-temperature electronics. The aviation industry now has a growing movement toward the "more electric aircraft" (MEA). Part of this initiative seeks to replace traditional centralized engine controllers with distributed control systems.[1] Centralized control requires large, heavy wire harnesses with hundreds of conductors and multiple connector interfaces. Moving to a distributed control scheme places the engine controls closer to the engine (Figure 3), reducing the complexity of the interconnections by a factor of 10, saving hundreds of pounds of aircraft weight,[2] and increasing the reliability of the system (estimated in part as a function of *connector pin count* (per MIL-HDBK-217F).[3]

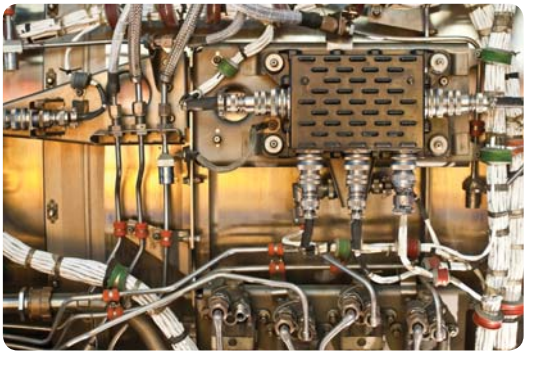


Figure 3. Controls mounted on aircraft engine.

The trade-off, however, is that the ambient temperature, in close proximity to the engine, ranges from –55°C to +200°C. Although electronics can be cooled in this application, it is undesirable for two reasons: cooling adds cost and weight to the aircraft, and, most importantly, failure of the cooling system could lead to failure of the electronics that control critical systems.

Another aspect of the MEA initiative is to replace hydraulic systems with power electronics and electronic controls to improve reliability and reduce maintenance costs. The control electronics ideally need to be very close to the actuators, which again produce a high-ambient-temperature environment.

The *automotive industry* provides another emerging application for use of high-temperature electronics. As with avionics, the auto industry is migrating from purely mechanical and hydraulic systems to electromechanical or *mechatronic* systems.[4] This requires locating sensors, signal conditioning, and control electronics closer to heat sources.

The maximum temperature and exposure time varies by vehicle type and location of the electronics on the vehicle (Figure 4). For example, higher integration of electrical and mechanical systems, such as collocation of the transmission and transmission controller, could simplify the manufacture, test, and maintenance of automotive subsystems.[5] Electric vehicles and hybrid-electrics require power electronics with high energy density for converters, motor controls, and charging circuits that are also associated with high temperatures.

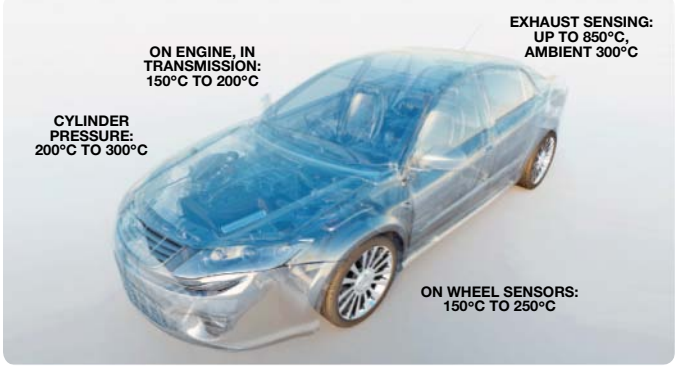


Figure 4. Typical automotive maximum temperature ranges.[5]

Using ICs Beyond Data Sheet Temperature Specifications

In the past, high-temperature electronics designers, such as those in the oil and gas industry, were compelled to use standard-temperature components well above their rated specification due to the unavailability of high-temperature ICs. Some standard-temperature ICs will indeed work at elevated temperatures, but it is an arduous and risky endeavor to use them. For example, engineers must identify potential candidates, completely test and characterize performance over temperature, and qualify the reliability of the part over a long period of time. Performance and lifetime of the part are often substantially derated. This is a challenging, expensive, and time-consuming process:

- Qualifying components requires testing in a lab oven with a high-temperature printed-circuit board (PCB) and fixtures, for at least as long as the mission profile requires. It is difficult to accelerate testing because new failure mechanisms may be encountered. Failures during testing require another iteration of component selection and long-term test, delaying project timelines.
- Operation outside of data sheet specifications is not guaranteed, and performance may vary between component lots. In particular, IC process changes can result in unexpected failures at temperature extremes.
- Plastic packages are only robust up to about 175°C—with reduced operating life. Near this temperature limit, it can be difficult to distinguish between a packaging-related failure and silicon-related failure without costly and time-consuming laboratory failure analysis. Availability of standard components in ceramic packages is scarce.
- Often, components used in harsh environments must survive not only high temperature but also severe shock and vibration. Many engineers prefer to use packages with leads, such as a DIP or a gull-wing SMT, because they provide a more robust attachment to the PCB. This further limits device selection, as other industries trend toward smaller, leadless packages.
- It could be desirable to obtain parts in die form, especially if a component is otherwise only available in a plastic package. The die can then be repackaged in a high-temperature compliant hermetic package or multichip module. However, of the few components that will work at elevated temperature, yet a smaller subset is readily available as *tested* dice.
- Due to time constraints and test-equipment limitations, engineers in the industry may tend to restrict qualification of a device to a specific application circuit, without covering all key device parameters, thus limiting component reuse for other projects without further testing.
- Key non-data-sheet IC properties, such as *electromigration* in metal interconnects, could lead to failures at high temperatures.

ICs Designed and Qualified for High Temperature

Fortunately, recent IC technology has produced devices that can operate reliably at elevated temperature with guaranteed data sheet specifications. Advances have been made in process technology, circuit design, and layout techniques.

Managing many key device characteristics is crucial for successful, high-performance operation at elevated temperatures. One of the most important and well-known challenges is posed by increased *substrate leakage current*. Some others are decreased *carrier mobility*, variation in device parameters, such as V_T, β, and V_{SAT}, increased *electromigration* of metal interconnects, and decreased *dielectric breakdown strength*.[6] Although standard silicon can operate well beyond the military requirement of 125°C,[7] leakage in standard silicon processes doubles for every 10°C increase, making it unacceptable for many precision applications.

Trench isolation, *silicon-on-insulator* (SOI), and other variations on the standard silicon process greatly decrease leakage and enable high-performance operation to well above 200°C. Figure 5 illustrates how an SOI bipolar process reduces the leakage area. Wide-band-gap materials, such as silicon carbide (SiC), raise the bar even higher; silicon carbide ICs have operated at up to 600°C in laboratory investigations. However, SiC is an emerging process technology, and, currently, only simple devices such as power switches are commercially available.

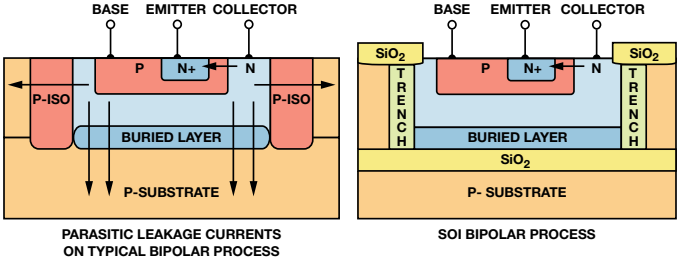


Figure 5. Junction leakage mechanisms in bulk silicon and SOI compared.

Instrumentation amplifier: Instrumentation amplifiers require high precision in downhole drilling applications to amplify very weak signals in the noisy environments commonly present. This specialty amplifier type is generally the first component at the measurement front-end, so its performance is critical to performance of the entire signal chain.

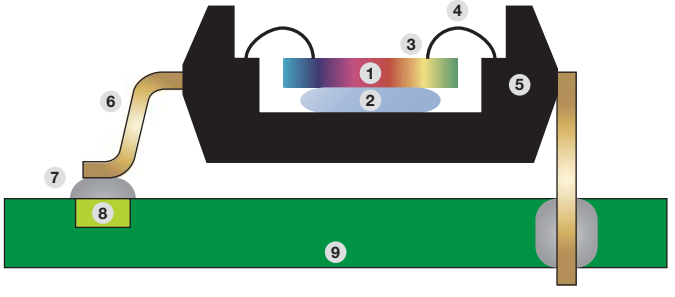
The Analog Devices development team targeted the AD8229 instrumentation amplifier for high-temperature operation from its inception and designed it for this purpose from the ground up. To meet its unique performance requirements, a proprietary SOI bipolar process was the technology of choice. The designers implemented special circuit techniques to guarantee operation over a wide variation of device parameters, such as base-emitter voltage and forward current gain.

The IC layout also critically affects the AD8229's performance and reliability. To maintain low offset and high CMRR over the entire temperature range, the layout compensates for variations in interconnect and temperature coefficient. In addition, careful analysis of the current flow densities in key sections mitigated the effects of electromigration, contributing to increased reliability under extreme conditions. Likewise, the designers anticipated fault conditions to prevent premature breakdown.

The combination of robust process, circuit-design, and layout techniques enables the device to meet the most stringent precision and reliability requirements over temperature.

Packaging Considerations

Once high-temperature functional silicon is in hand, the battle is only half won. Packaging the die, and then attaching the package to the PCB, is not trivial at high temperatures. Many factors affect package integrity at temperature (Figure 6).



[1]SILICON
[2]DIE ATTACH
[3]BOND-PAD METALLIZATION
[4]BOND WIRES
[5]PACKAGE
[6]PINS
[7]PIN SOLDER INTEGRITY
[8]PCB TRACES
[9]PCB-THERMAL INTEGRITY

Figure 6. Elements of IC packaging and mounting.

The *die-attach* material secures the silicon to the package or substrate. Many materials proven for use in standard temperature ranges have a low glass transition temperature (T_G) and are not suitable for high-temperature operation. Particular attention needs to be paid to matching the *coefficient of thermal expansion* (CTE) between the die, die-attach, and substrate—so that the die is not stressed or fractured over cycles of wide temperature span. Even slight mechanical stress on the die can cause electrical parameters to shift to unacceptable levels for precision applications. For power devices that require thermal and electrical connection to the package substrate, metallic die-attach materials may be necessary.

Wire bonding is a method for interconnecting the die to the pins by attaching metallic wires from the lead frame to bond pads on the die surface. When considering wire bond reliability at elevated temperatures, the compatibility of the metals used for the wire and bond-pad metallization is of major concern. Failures related to poor compatibility of bonding metals are twofold: *intermetallic compound* (IMC) growth at the boundary interface, which creates a brittle bond; and *diffusion* (Kirkendall effect), which creates voids at the interface, weakening the bond's strength and increasing its resistance. Unfortunately, one of the most popular metal combinations in industry—gold wire and aluminum bond-pad metallization—is prone to these phenomena at elevated temperatures. Figure 7, a section through an Au/Al bond, shows IMC growth, which is compromising bond integrity after 500 hours at high temperature.

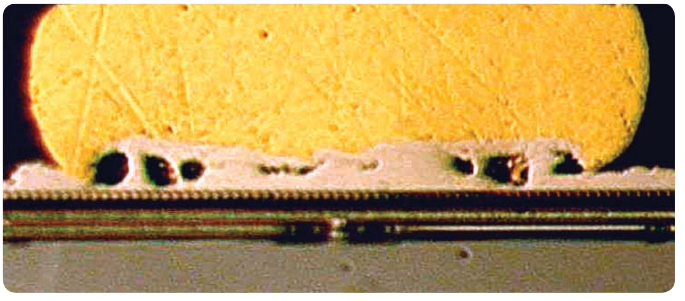


Figure 7. Au/Al bond after 500 hours at 195°C.

Figure 8 shows substantial Au/Al intermetallic growth and Kirkendall voids after bond failure at high temperature. To make matters worse, halogens such as bromine and chlorine—sometimes found in molding compounds—can cause corrosion at the boundary interface at elevated temperature, accelerating the time to failure (although fortunately, the industry is shifting to "green" halogen-free molding compounds). Thus, there is a strong incentive to use the same metal for the bond wire and bond pad (a *monometallic* bond) to avoid these negative effects. If this is not possible, engineers should select metals that have slow enough IMC growth and diffusion rates to be reliable over the required lifetime.

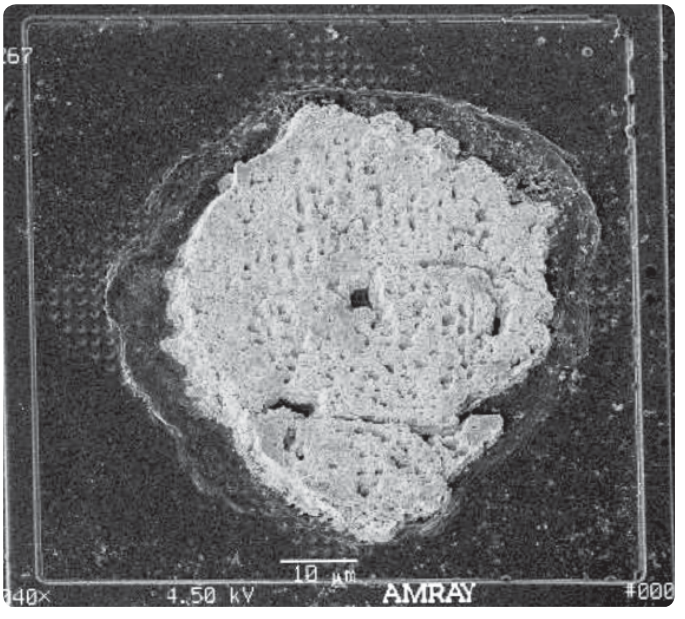


Figure 8. Intermetallic growth with voids.

Figure 9 illustrates the robustness of the monometallic bond at elevated temperature. The bond section shows no sign of IMC growth after 3000 hours at 195°C.

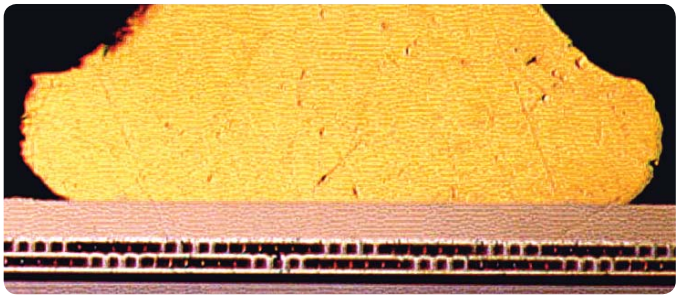


Figure 9. Monometallic bond after 3000 hours at 195°C.

The IC *package* must also withstand stresses imposed by harsh environments. Plastic packages, although the industry standard, have historically only been rated to 150°C for sustained use. With recent interest in high-temperature applications, investigations have shown that this rating can stretch to 175°C but only for relatively short durations. Depending on package construction, 175°C is the point at which some materials, such as the molding compound, exceed the glass-transition temperature. Operating above T_G can cause significant mechanical changes in key parameters, such as CTE and flexural modulus, and lead to failures such as delamination and cracking from the increased thermal strain.[8]

For this reason, hermetic ceramic packages are preferred for high-temperature applications (Figure 10). The hermetic seal provides a barrier to the moisture and contamination ingresses that cause corrosion. Unfortunately, hermetic packages are normally larger, heavier, and significantly more expensive than their plastic counterparts. In applications with less extreme temperature requirements (<175°C), plastic packages may be preferred to conserve PCB area, reduce cost, or provide better vibration compliance. For systems requiring hermetic packaging *and* high component density, *high-temperature multichip modules* may be an appropriate solution. However, this solution requires that known good dice be available.

Figure 10. Hermetically sealed side-brazed ceramic DIP package.

Package lead configuration and metallization must also be evaluated. Surface-mount components depend solely on the bond pad area and quality of the adhesive between the copper layer and the preimpregnated material (prepreg). On the other hand, the throughhole DIP configuration, one of the most proven and reliable packages in industry, also provides robust shock and vibration performance. In extreme cases, attachment strength can be improved further by bending the pins on the bottom side of the board to "staple" it to the PCB, but the throughhole pinout does not allow component population of the bottom side of the board—possibly a major concern for applications such as downhole instruments, which have tight space constraints.

Gull-wing SMT lead configuration is a viable alternative in many cases, but leadless SMT may not be robust enough under high shock and vibration conditions encountered in many high temperature environments. When using SMT components, the designer should consider their height and mass. The application of high-temperature epoxies will improve attachment robustness but increase manufacturing costs and limit the ability to perform repairs. In all cases, the lead metallization must be compatible with high-temperature solders.

The most popular standard solder alloys have melting points below 200°C. However, there are some readily available alloys that fall within the category of "high melting point" (HMP), with melting points well above 250°C. Even in such cases, the maximum recommended operating temperature for any solder subjected to stress is about *40°C below its melting point*. For example, the standard HMP solder alloy composition of 5% tin, 93.5% lead, and 1.5% silver has a melting point of 294°C but is recommended for use only up to about 255°C.[9] Note that *BGA* (ball-grid array) *packages* have solder balls attached by the factory that may not have a high melting point.

Finally, the *PCB itself* is a potential source of failure. Standard FR4 reaches glass transition anywhere from 130°C to 180°C, depending on the specific composition. If used above this temperature—for even short time durations—it can expand and delaminate. A good proven alternative is *polyimide*, the same material used in Kapton, which has T_G as high as 250°C, depending on composition. However, polyimide suffers from very high moisture absorption, which can quickly lead to failure of the PCB by a variety of mechanisms, so it is important to control moisture exposure. In recent years, industry has introduced exotic laminates that absorb less moisture and maintain integrity at high temperatures.

Verification, Qualification, and Test

Verification of high-temperature components in the laboratory is not a trivial task, as it requires engineers to incorporate all the previously mentioned techniques to test performance at temperature extremes. In addition to using special materials in the construction of the test jig, test engineers must operate the environmental chambers carefully, allowing the system to adjust to the required temperature changes. Due to the mismatch in expansion coefficients, fast temperature changes can result in damage to the solder joints on the PC board, warping, and ultimately, premature system failure. A guideline employed in the industry is to maintain the temperature rate of change below 3°C per minute.

To accelerate testing of life and reliability, an accepted practice for electronic components is to perform the tests at an elevated temperature. This introduces an acceleration factor, α, defined by the Arrhenius equation:

$$\alpha = e^{\frac{E_a}{k}\left(\frac{1}{T_a}-\frac{1}{T_s}\right)}$$

where E_a is the activation energy, k is the Boltzmann's constant, T_a is the expected operating temperature during use, and T_s is the stress temperature. Although accelerated aging works well for standard products, increasing the stress temperature well above the rated temperature may introduce new failure mechanisms and yield inaccurate results. Therefore, to guarantee the lifetime reliability of high-temperature devices like the AD8229, the *high-temperature operating life* test (HTOL) was run at the maximum rated temperature of 210°C for 1000 hours (approximately six

weeks). For lower temperatures, the expected lifetime can be predicted using the acceleration relationship shown in Figure 11.

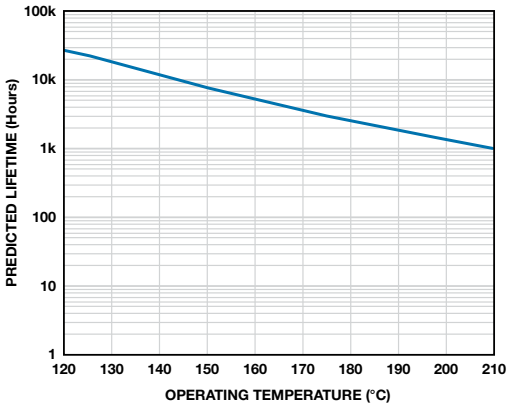


Figure 11. AD8229 lifetime vs. operating temperature, 1000 hours @ 210°C.[11]

There are additional hindrances to reliable characterization of high-temperature ICs. For example, the test and measurement system used is only as reliable as its weakest link. This means that every element exposed to elevated temperatures over a long period must be inherently more reliable than the IC itself. An unreliable system will yield data that does not represent the long-term reliability of the component and will result in costly and time-consuming repetitions of the process. Statistical techniques for increasing the success rate include accurately *oversizing* the test sample to add a margin of error for premature system failures not caused by a DUT (device under test) failure.

Another hurdle is imposed by production steps required to guarantee performance parameters at the extremes, such as test, probing, and trimming. The development team needs to customize these steps for high-temperature products.

High-Temperature System Design Considerations

The designer of circuits that operate at high temperature must account for changes in IC parameters and passive components over a wide temperature range, paying close attention to their behavior at the temperature extremes to ensure circuit operation within the target limits. Examples include offset and input bias drift, gain errors, temperature coefficients, voltage ratings, power dissipation, board leakage, and intrinsic leakage of other discrete devices—such as those used in ESD and overvoltage protection devices. For example, in situations where high source impedance is in series with an amplifier input terminal, undesired leakage currents (other than the amplifier's own bias current) can create offsets that will induce bias-current measurement error (Figure 12).

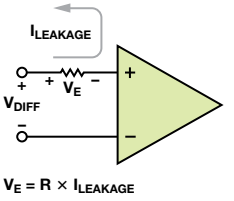


Figure 12. How bias and leakage induce offset errors.

In all cases, high-temperature operation exacerbates board leakages introduced by contaminants such as solder flux, dust, and condensation. Proper layout can help minimize these effects by providing adequate spacing between sensitive nodes—separating amplifier inputs from noisy power rails, for example.

The standard pinout for operational amplifiers and instrumentation amplifiers places one of the input terminals next to the negative supply terminal. This dramatically reduces the tolerance for post-assembly PCB flux residues that can produce increased leakage. To reduce leakage and increase high-frequency CMRR, the AD8229 employs the same high-performance pinout as other precision instrumentation amplifiers built by Analog Devices (Figure 13).

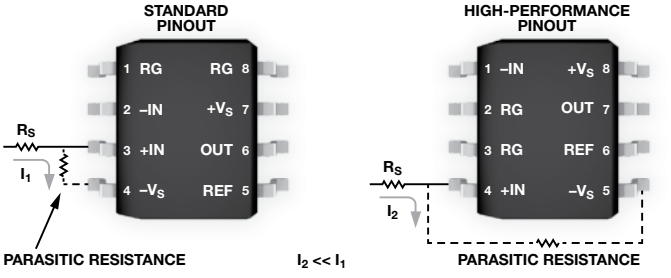


Figure 13. Modification of device pinout helps minimize parasitic leakage.

The leakage of diodes, transient-voltage suppressors (TVS), and other semiconductor devices increases exponentially with temperature, and, in many cases, can be many orders of magnitude larger than the input bias current of the amplifier. In such cases, the designer must ensure that the leakage at extreme temperatures will not degrade the circuit specifications beyond the desired limits.

Nowadays, several passive components are available for high-temperature operation. Resistors and capacitors are ubiquitous in any circuit design. Some commercially available options are shown in Table 1.

Table 1. Examples of High-Temperature Resistors and Capacitors

Capacitors	Max Rated Temperature	Comments
MLCC (ceramic) C0G/NP0	200°C	Low values, low TC, available in SMT or throughhole
MLCC (ceramic) X7R	200°C	Higher TC than C0G/NP0, lower cost
Electrolytic Wet Tantalum	200°C	High capacitance values, mostly throughhole
Electrolytic Tantalum	175°C	High capacitance values, SMT packages available

Resistors	Max Rated Temperature	Comments
Wire-Wound	275°C	High surge capability, stable
Metal Film	230°C	High precision
Metal Oxide	230°C	General-purpose
Thick Film	275°C	General-purpose, wide resistance range
Thin Film	215°C	Compact, low TC, high stability, resistor arrays available
Ceramic Composition	220°C	High-temperature replacement for carbon composition

Note that surface-mount components are prone to leakage between terminals if their bodies sit against the PC board, as flux residues tend to remain trapped underneath after the assembly process. Such residues wick moisture, which, at high temperature, increases their conductivity. In this situation, a parasitic resistor (with rather unpredictable behavior) will appear across the surface-mount component, potentially introducing additional circuit errors. To overcome this problem, consider selecting larger chip sizes, gull-wing lead-forming, or throughhole components in areas of the circuit that are particularly sensitive. Ultimately, this undesired residue can be all but eliminated by adding an effective board wash step, typically employing ultrasound or a saponifier, at the end of the assembly process.

The designer of systems that will operate in harsh environments must keep thermal management in mind. Even with components designed for high ambient temperature, consider the self-heating associated with their power dissipation. In the case of the AD8229, its guaranteed operation up to 210°C assumes a small output current load. Additional power dissipation caused by driving heavy loads or permanent fault conditions (such as an output short circuit), will increase the junction temperature beyond the maximum ratings of the part, greatly reducing the operating life of the amplifier. It is important to follow the recommended guidelines for heat dissipation and to be aware of adjacent heat sources, such as power regulators.

Even high-temperature resistors have derated power ratings above 70°C. Pay special attention to resistor temperature ratings at the intended operating temperature, especially if they will dissipate a considerable amount of power. For example, if a 200°C-rated resistor is operating in an ambient temperature of 190°C, but if its self-heating due to power dissipation is 20°C, it will be exceeding its rating.

While many passive components can withstand high temperatures, their construction may not be suitable for long-term exposure to environments that may combine high temperature with shock and vibration. In addition, manufacturers of high-temperature resistors and capacitors specify the operating life at a given temperature. Matching the operating life specifications of all the components is important to obtain a high reliability system. Finally, do not overlook that many components rated for high temperature may need additional derating to achieve lasting operation.

Case Study: Mapping the Thermal Gradient in an Oven

As a demonstration of two suitable devices in a high-temperature application, the AD8229 and ADXL206 (dual-axis accelerometer) were operated in a high-temperature environment that was both portable and safe to use. The demonstration utilizes a small electric oven with a rotating assembly on which a high temperature PCB is mounted and continuously operated. The heating element inside the oven is located near the top. This arrangement creates a large temperature gradient inside the volume of the oven. The rotating mechanism lends itself to an experiment that can combine temperature and position measurements.

The AD8229 conditions the signal coming from a K-type thermocouple, which is constantly rotating inside the oven. The thermocouple probe extends about 6" beyond the PCB—the better to measure variation of the oven temperature. At the same time, the ADXL206 measures the angle of rotation. Three signals (temperature gradient, x-acceleration, and y-acceleration) are sent through a slip ring (rotary connector) rated for high-temperature operation. The slip ring maintains connection to the nonrotating harness, which connects to the data-acquisition board outside the oven. Since the "cold junction" is located inside the oven, a second thermocouple provides a static reference to the internal temperature. The AD8495 thermocouple amplifier (also *outside* the oven) uses its integrated cold-junction compensation to condition the signal of the additional thermocouple.

The board inside the oven is located near the center on the rotating assembly, where the approximate temperature is 175°C. The board's construction uses polyimide material. The tracks on the copper layers use a minimum width of 0.020" to improve copper adhesion to the prepreg material (Figure 14). The components were attached using standard HMP solder (5/93.5/1.5 Sn/Pb/Ag), and Teflon-coated wires were used to connect the board and the slip ring.

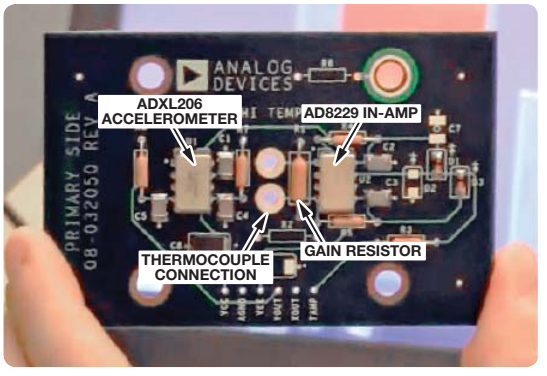


Figure 14. High temperature PCB with components mounted.

All precision components use throughhole mounting. A 25 ppm/°C metal-film resistor sets the gain of the instrumentation amplifier. The amplifier operates at high gain, so the trace length from the amplifier to the gain resistor is as short as possible to minimize copper resistance (4000 ppm/°C TC). The interface between the thermocouple and the amplifier is located at the center of the board, in order to maintain a constant temperature during rotation. The thermocouple terminals are as close together as possible to cancel undesired thermal EMF effects at the junction.

High-temperature tantalum capacitors and C0G/NP0 capacitors decouple the power supply and serve as filters for the output of the accelerometer.

A computer processes data from four different sources: the angle of rotation (the rectangular x and y components), the internal temperature gradient, and the reference temperature. All these measurements are combined together to map the temperature gradient (Figure 15). The analysis results show that the temperature variation can be as wide as 25°C. As expected, the highest temperature is near the heating element, which is located near the top of the back wall of the oven. Due to natural convection, the top portion of the oven is the second hottest area inside the oven. The lowest temperature is sensed when the thermocouple is opposite to the heating element.

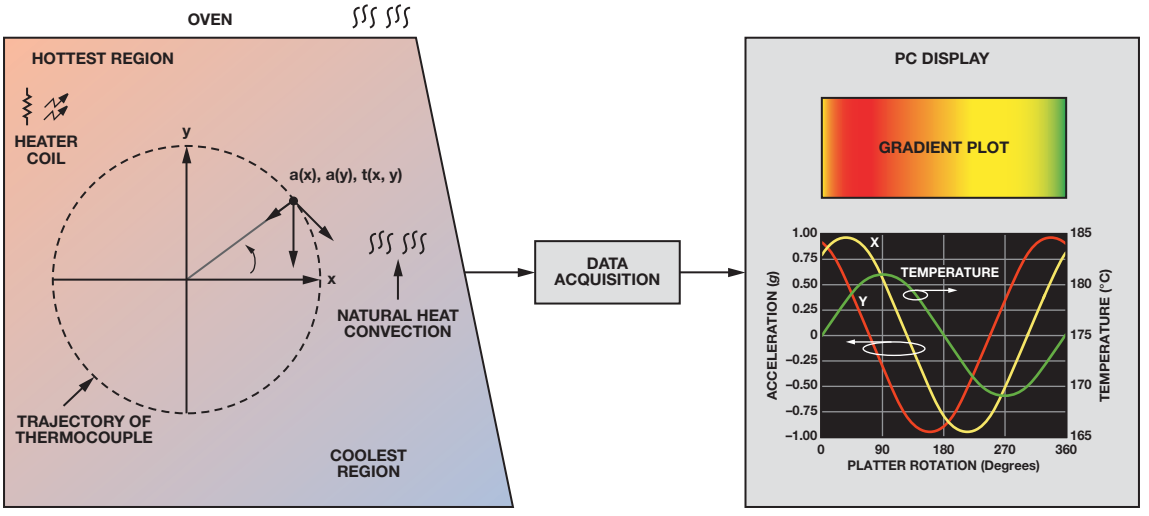


Figure 15. High temperature demo diagram.

This experiment suggests, in a simple way, how high-temperature components, integrated into a logging system, can extract valuable information while operating in a harsh environment.

Conclusion

Many applications, both established and emerging, require components that function in very high-temperature environments. In the past, it was challenging to design such systems reliably due to the lack of devices rated for these kinds of harsh environments. Now, ICs and supporting components designed and qualified to operate in these environments are available, saving engineering time and lowering the risk of failure. Leveraging this new technology and following high-temperature design practices will enable high-performance systems to operate reliably in even more extreme environments than were previously feasible.

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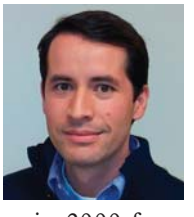
Authors

Jeff Watson [jeffrey.watson@analog.com] is a systems applications engineer in the Industrial and Instrumentation segment, focusing on high temperature applications. Prior to joining Analog Devices, he was a design engineer in the downhole oil and gas instrumentation industry and off-highway automotive instrumentation/controls industry. Jeff received bachelor's and master's degrees in electrical engineering from Penn State University.



Gustavo Castro [gustavo.castro@analog.com] is an applications engineer in the Precision Signal Conditioning Group in Wilmington, MA. Prior to joining Analog Devices in January 2011, he worked for 10 years designing high precision instrumentation, such as digital multimeters and dc sources. Gustavo received a bachelor's degree in electronics engineering in 2000 from Monterrey Institute of Technology, Mexico. He holds two patents.

Simple Circuit Provides Adjustable CAN-Level Differential-Output Signal

By Darwin Tolentino

The *controller area network* (CAN) serial-bus topology allows devices and microcontrollers to communicate with each other without the use of a host computer. Featuring arbitration-free transmission, it places a controller and a host processor at each device node, eliminating the more complex wiring harness that would be necessary to interconnect devices with a host computer.

By using the signals on CANH and CANL wires, the CAN bus has two states: *recessive* and *dominant*. The bus is in the dominant state if the differential voltage is greater than 0.9 V and in the recessive state if it is less than 0.5 V. CAN transceivers, such as the ADM3051, interface the CAN controller to the physical layer bus.

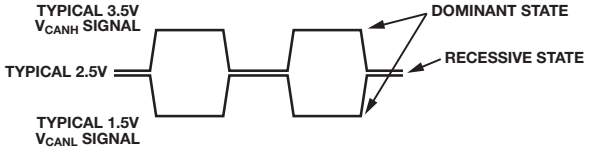


Figure 1. CAN bus signals and states.

A CAN transceiver can be characterized using automated test equipment (ATE) or dc signals on a bench. The circuit shown in Figure 2 uses a square wave signal from a function generator to provide adjustable CAN signals to a transceiver. The AD8138 high speed differential amplifier was chosen for its wide bandwidth and low distortion. A dc level shifter at the output enables the differential level of the output signals to be adjusted while maintaining their peak-to-peak levels. The amplitude and frequency are adjusted via the signal generator.

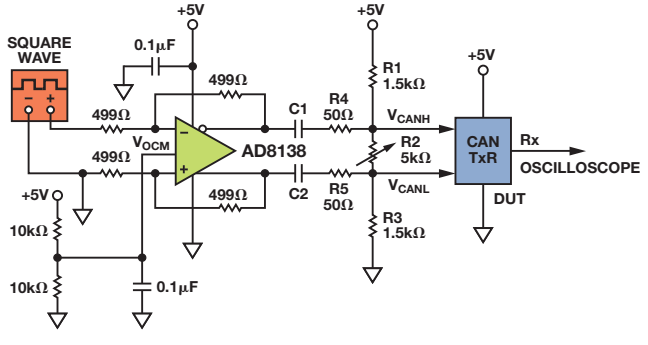


Figure 2. AD8138 drives CAN transceiver.

Operating from a single 5-V supply, the circuit is configured as a unity-gain single-ended-to-differential amplifier with common mode set at midsupply. R1, R2, and R3 form the dc biasing circuit that scales the output signals to CAN levels. By keeping R4 and R5 small compared to R2, the potentiometer conveniently adjusts the difference between the two output signals without significantly affecting their individual amplitudes, providing a CAN signal with a variable common-mode level to the DUT. Because R1 and R3 are equal, the ac common mode of the outputs is also unaffected when adjusting R2. Together with R2, R4 and R5 form part of the voltage divider at the output of the AD8138 amplifier. The smallest possible values are chosen for R4 and R5 to minimize the attenuation at the output and the effect of adjusting R2 on the peak-to-peak level of each output. If R2 is shorted, R4 and R5 will also provide the minimum load to protect the amplifier's output. Capacitors C1 and C2 isolate the dc bias from the amplifier's output common mode. These capacitors also form a high-pass filter with the resistor bias network; its cutoff frequency is:

$$f_c = \frac{1}{2\pi[(R_4 + R_5) + (R_2 \parallel R_L) \| (R_1 + R_3)]\frac{C}{2}}$$

where C = C1 = C2, and R_L is the load or DUT input resistance, typically around 20 kΩ to 30 kΩ.

To avoid distorting the square wave output signals, $C1$ and $C2$ should be chosen as large as possible so that the input signal frequency is 10 times the worst-case cutoff frequency, where $R_2||R_L$ is at minimum. For example, to achieve V_{CANH} and V_{CANL} signals with the levels shown in Figure 3(a), R_2 must be a minimum of 700 Ω, assuming no output (DUT) loading effect. A 0.1 µF or 1 µF coupling capacitor can accommodate a 1-MHz signal. Figure 3(b) demonstrates how R2 adjusts the differential output levels.

Using these output signals as V_{CANH} and V_{CANL} inputs to a transceiver enables bench scope measurements to characterize receiver parameters such as propagation delay, rise time, and thresholds on desired frequencies.

Author

Darwin Tolentino [darwin.tolentino@analog.com] is a senior test development engineer for the High Speed Group at ADI in the Philippines. He has worked on the test development for amplifiers and linear products and has supported high-speed interface products. Darwin joined ADI in 2000 and has 14 years of experience in the semiconductor industry.

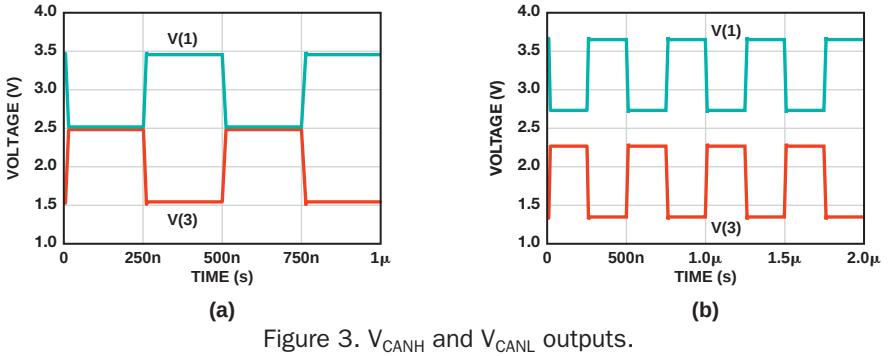


Figure 3. V_{CANH} and V_{CANL} outputs.

ADI Capacitance-to-Digital Converter Technology in Healthcare Applications

By Ning Jia

Introduction

In recent years, advances in electronic technology have made many innovations and improvements in the healthcare industry possible. The challenges for healthcare equipment include developing new diagnosis and treatment methods, enabling remote monitoring and home healthcare devices, improving quality and reliability, and enhancing flexibility and ease of use.

For more than 40 years, Analog Devices' comprehensive portfolio of linear, mixed-signal, MEMS, and digital signal-processing technologies have helped make a difference in healthcare designs in areas such as instrumentation, imaging, and patient monitoring. This article will focus on *capacitance-to-digital converter* (CDC) technology, which enables the use of high performance capacitance sensing in healthcare applications.

Capacitive Touch Sensor Controller—A Novel User Input Method

A *capacitive touch sensor* provides a user interface in the form of a push button, a slider bar, a scroll wheel, or other forms similar to the examples shown in Figure 1.

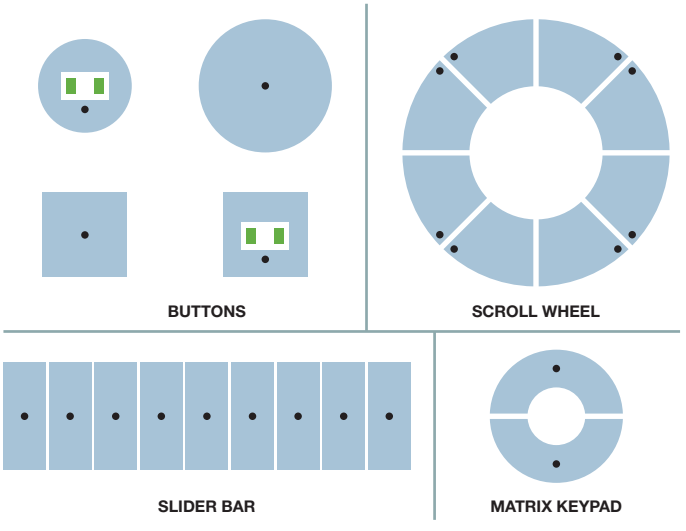


Figure 1. Examples of touch sensor layout.

Each blue geometric area represents a sensor electrode on a printed circuit board (PCB) that forms one plate of a virtual capacitor. The other plate is formed by the user's finger, which is essentially grounded with respect to the sensor input. The AD7147/AD7148 CapTouch™ controller family, designed to activate and interface with capacitive touch sensors, measures capacitance changes from single-electrode sensors. The device first outputs an excitation signal to charge the plate of the capacitor. When an object, such as the user's finger, comes close to the sensor, the virtual capacitor is formed, with the user acting as the second capacitor plate (Figure 2). The capacitance is measured using a capacitance-to-digital converter (CDC).

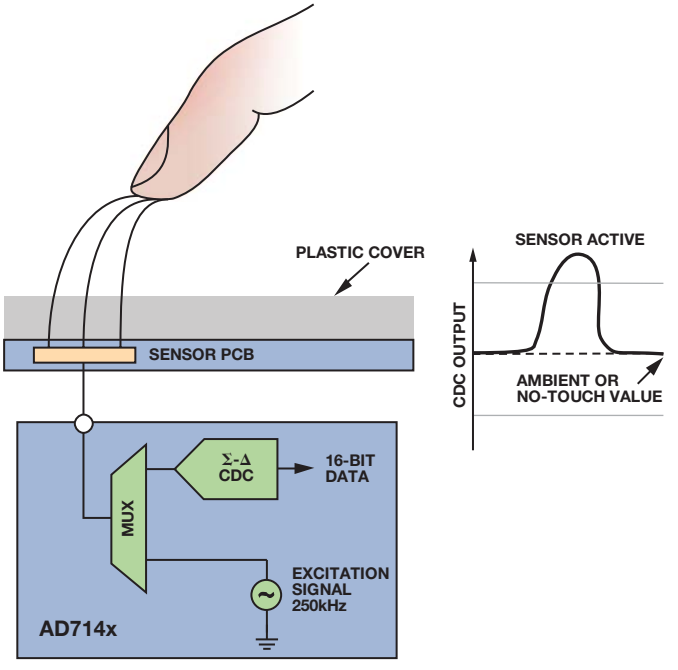


Figure 2. Capacitance sensing illustration and typical response.

The CDC, capable of sensing capacitance changes of the external sensors, uses this information to register a sensor activation. The AD7147 and AD7148, with 13 and eight capacitance sensor inputs, respectively, have on-chip calibration logic that compensates for measurement changes caused by changes in the ambient environment, thus ensuring that there are no false triggers on the external sensors due to changing temperature or humidity.

The AD7147 and AD7148 provide various operational modes, user-programmable conversion sequences, and very flexible control features. These features make them ideal for high-resolution touch sensor functions, such as slider bars or scroll wheels, with minimal software requirements. Furthermore, button-sensor applications can be implemented completely by on-chip digital logic without any software requirement.

Capacitance Detection and Measurement Basics

Capacitance is the ability of a capacitor to store energy in an electric field. In its nominal form—a parallel-plate capacitor—the capacitance, C, is a measure of the charge, Q, stored in a capacitor at a given voltage, V, and is calculated by $C = \frac{Q}{V}$.

The essence of capacitance detection and measurement technique is shown in Figure 3 for a parallel-plate capacitor.

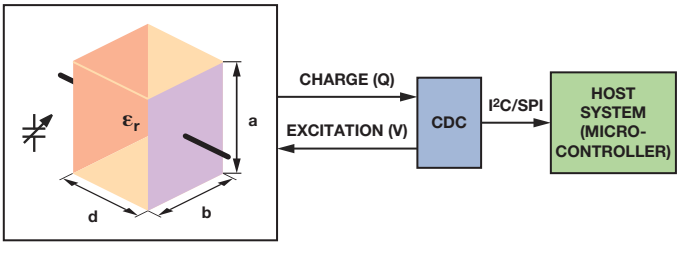


Figure 3. Measuring a parallel-plate capacitor's capacitance.

A parallel-plate capacitor consists of two conductors (metal plates) and is characterized by

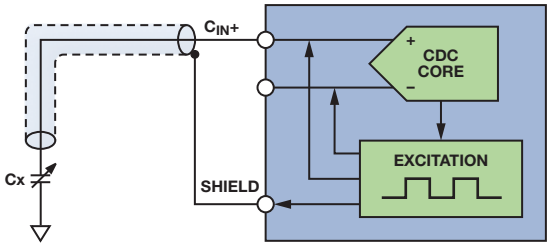
- Conductor *area*, $a \times b$
- *Distance*, d, between the two conductor plates
- Dielectric material between two conductors, characterized by the dielectric constant, ε_r

The capacitance, based on this geometry, is calculated by

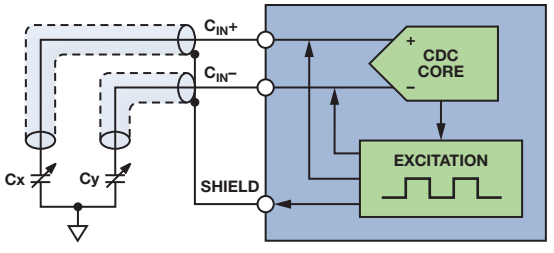
$$C = \varepsilon_0 \varepsilon_r \frac{a \times b}{d}$$

where ε_0 is the permittivity of free space.

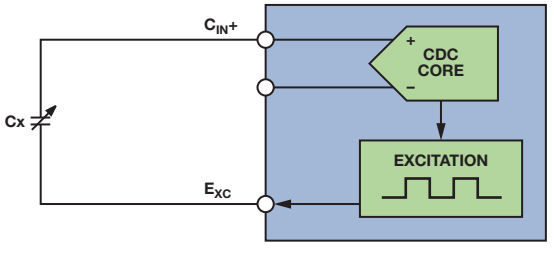
The CDC device applies an excitation to one plate of the capacitor and measures the charge stored in the capacitor; then, the digital result is available for the external host. Four types of capacitance sensors, shown in Figure 4, are differentiated by the way the excitation is applied.



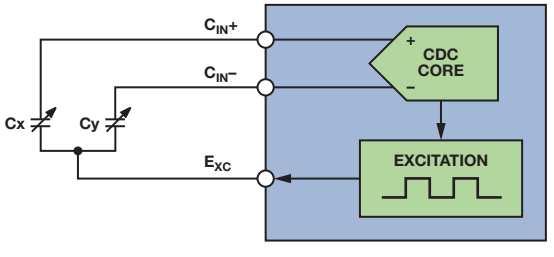
(a) SINGLE-ENDED GROUNDED SENSOR.



(b) DIFFERENTIAL GROUNDED SENSOR.



(c) SINGLE-ENDED FLOATING SENSOR.



(d) DIFFERENTIAL FLOATING SENSOR.

Figure 4. Sensor electrical configurations.

Because the sensor capacitance is determined by a, b, d, and ε_r, varying the values of these parameters, or observing variations in their values, allows CDC technology to be used for direct capacitance value measurement, as well as for many other kinds of applications, depending on the sensor types. For example, if a, b, and ε_r are constant, the CDC output is in inverse proportion to the distance between two conductors.

Applications

The AD714x, AD715x, and AD774x families of CDC products are suitable for a wide range of applications, involving various sample rates, resolutions, input ranges, and input sensor types. Although the possible applications of capacitance sensing are limited only by the user's creativity, here are a few ideas for applications in the healthcare field.

Liquid Level Monitoring

In many applications, such as transfusions, the amount of liquid used must be measured, or the flow must be shut down before the infusion bottle is empty. To save time for medical personnel, automatic liquid level sensing can help eliminate the need for manual checks.

The basic principle for liquid level sensing is shown in Figure 5. Build a parallel-plate capacitor with plates that tightly adhere to the outside wall of the infusion bottle and extend to near the bottom of the bottle. As the level of the infusion liquid changes, the amount of dielectric material between the plates changes, thus producing a change in capacitance. To allow the use of various infusion substances with different dielectric constants, a second capacitive sensor located near the bottom acts as a reference channel to produce ratiometric measurements.

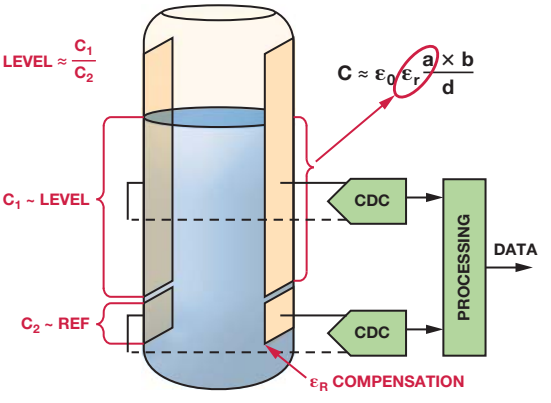


Figure 5. Liquid level sensing.

The 24-bit AD7746, with its two capacitance measurement channels, could be useful for this kind of application.

Connectivity Detection Between Electrodes and Human Body

For devices intended to operate in the vicinity of human skin, such as those shown in Figure 6, it is often beneficial to have information about the quality of contact between the device's surface area and the patient's skin—before the device is activated or a measurement is taken. The range of end uses could include a medical probe that needs to rest flush on the skin, a biopotential electrode sensor, or the housing holding a catheter tube in place. To obtain this additional information, several capacitive sensor electrodes, shown in blue, could be embedded directly into a device's plastic housing at the injection molding stage during manufacturing. Once the electrode information is available, a simple algorithm running on the host controller could be applied to determine if all sensor electrodes were making proper contact with the skin.

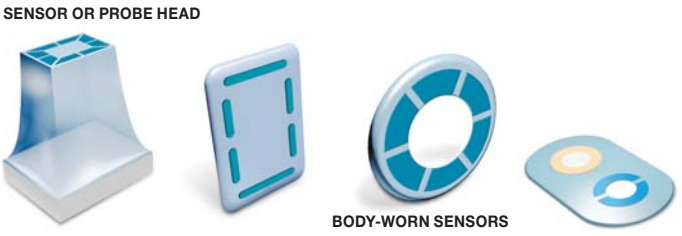


Figure 6. Devices using capacitive sensor electrodes.

The examples shown in Figure 6 use capacitive sensors in an unconventional way: a user positions a device containing the capacitive sensing electrodes on the human body, in contrast with the traditional capacitive sensing human interface applications, where a person typically initiates contact with the sensor electrodes by finger touch. Developing the type of applications shown in Figure 6 is rather straightforward using the AD7147/AD7148.

Sweat Detection

In some medical and fitness-testing equipment, there is a need to measure perspiration from a human body. This is typically performed by measuring the skin's electrical conductivity. However, if the measurement needs to be performed without galvanic contact, this function can be implemented by detecting the humidity near the human body using a capacitance sensor.

When people sweat, the humidity (dielectric constant) close to the human skin increases; a noncontacting electrode in this vicinity could be used to measure the resulting change in capacitance.

It may be useful to add a second capacitance sensor to measure the ambient humidity and use it for common-mode compensation.

Respiratory Rate Measurement

Respiratory rate measurement is an important module in patient monitoring systems.

In one approach, shown in Figure 7, an excitation plate is put on the back of the patient while the sensor electrode belt is fastened on the right side of the chest of the patient. As the lungs fill and empty, the resulting chest movements change the distance between two plates. The dielectric constant will also change because of the complex physiological activities during breathing. These capacitance changes can be measured by CDC devices.

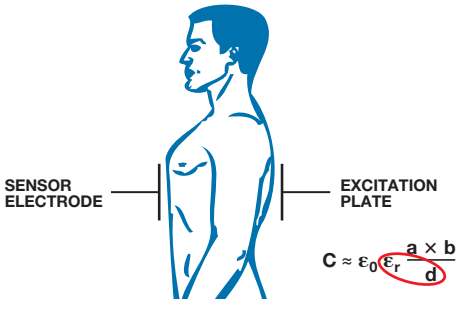


Figure 7. Respiratory rate measurement.

The reason the sensor electrode is placed on the right side of the subject's chest is that this position gets the least impact from other physiological activities. However, it might be possible to get more information on bodily functions by putting multiple sensor electrodes on different positions on the patient's chest. This may be an interesting topic for further research.

Blood Pressure Measurement

In blood pressure measurement applications using an inflatable cuff, an important task is to measure the pressure at the air valve. A capacitive sensor can be easily used in this kind of pressure sensing applications.

As shown in Figure 8, the diaphragm of the pressure sensor is basically made from two capacitive plates. As pressure is applied to the sensor, the capacitive plates move closer together. The reduced distance between the plates increases the capacitance.

A temperature sensor can be used to detect the temperature change of the sensor to compensate its characteristics change with temperature. The AD774x family has an internal temperature sensor to measure the on-chip temperature—and an additional ADC voltage channel that can be used to measure the temperature at the sensor site.

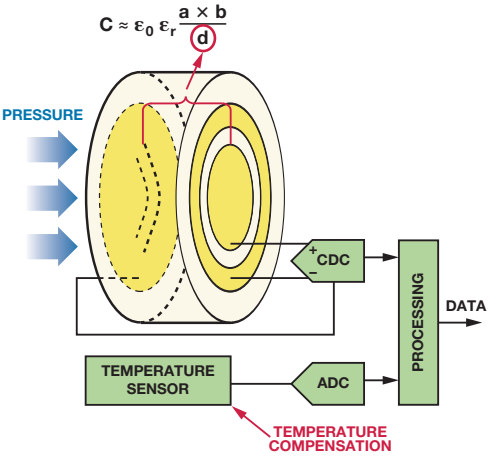


Figure 8. Pressure sensing with a capacitive sensor.

Conclusion

This article, a brief introduction to advances in CDC technology at Analog Devices, hints at the enormous potential of CDC techniques in healthcare applications. However, sensor design—including pattern, size, and position—the associated detailed electronic circuit design, and the need for deep research, comprehensive experiments, and effective testing, are critically dependent on the nature of each application, so we merely hope to stimulate creativity by suggesting some possibilities here.

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Information on all ADI products can be found at www.analog.com.

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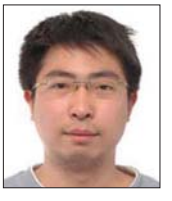

Ning Jia [ning.jia@analog.com] is an applications engineer in the Customer Applications Center, Asia. He is responsible for technical support of a broad range of analog products across Asia. Ning joined Analog Devices in 2007 after graduating from Beijing University of Posts and Telecommunications with a master's degree in signal and information processing.

Understanding Microphone Sensitivity

By Jerad Lewis

Sensitivity, the ratio of the analog output voltage or digital output value to the input pressure, is a key specification of any microphone. Mapping units in the acoustic domain to units in the electrical domain determines the magnitude of the microphone output signal, given a known input.

This article will discuss the distinction in sensitivity specifications between analog and digital microphones, how to choose a microphone with the best sensitivity for the application, and why adding a bit (or more) of digital gain can enhance the microphone signal.

Analog vs. Digital

Microphone sensitivity is typically measured with a 1 kHz sine wave at a 94 dB sound pressure level (SPL), or 1 pascal (Pa) pressure. The magnitude of the analog or digital output signal from the microphone with that input stimulus is a measure of its sensitivity. This reference point is but one characteristic of the microphone, by no means the whole story of its performance.

The sensitivity of an analog microphone is straightforward and easy to understand. Typically specified in logarithmic units of dBV (decibels with respect to 1 V), it tells how many volts the output signal will be for a given SPL. For an analog microphone, sensitivity, in linear units of mV/Pa, can be expressed logarithmically in decibels:

$$Sensitivity_{dBV} = 20 \times \log_{10}\left(\frac{Sensitivity_{mV/Pa}}{Output_{AREF}}\right)$$

where $Output_{AREF}$ is the 1000 mV/Pa (1 V/Pa) reference output ratio.

Given this information, with the appropriate preamplifier gain, the microphone signal level can be easily matched to the desired input level of the rest of the circuit or system. Figure 1 shows how the microphone's peak output voltage (V_{MAX}) can be set to match an ADC's full-scale input voltage (V_{IN}) with a gain of V_{IN}/V_{MAX}. For example, an ADMP504 with 0.25 V maximum output voltage could be matched to an ADC with 1.0 V full-scale peak input voltage by using a gain of 4 (12 dB).

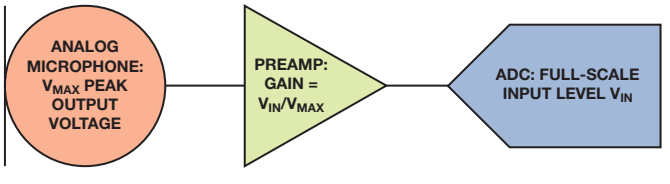

Figure 1. Analog microphone input signal chain with preamp to match microphone output level to ADC input level.

The sensitivity of digital microphones, with units dBFS (decibels with respect to digital full scale), is not so straightforward. The difference in units points to a subtle contrast in the definition of sensitivity of digital microphones compared to that of analog microphones. For an analog microphone with a voltage output, the only limit to the size of the output signal is the practical limit of the system's voltage supplies. Although it may not be practical for most designs, there is no physical reason why an analog microphone couldn't have 20 dBV sensitivity, with a 10 V output signal for a reference-level input signal. This sensitivity could be accomplished as long as the amplifiers, converters, and other circuits could support the required signal levels.

Sensitivity of a digital microphone is less flexible; it depends on a single design parameter, *maximum acoustic input*. As long as the full-scale digital word is mapped to the microphone's maximum acoustic input (the only sensible mapping, really), the sensitivity *must* be simply the difference between this maximum acoustic signal and the 94 dB SPL reference. So, if a digital microphone's maximum SPL is 120 dB, then its sensitivity will be –26 dBFS (94 dB – 120 dB). There is no way to tweak a design to make the digital output signal higher for a given acoustic input, unless the maximum acoustic input is lowered by the same amount.

For digital microphones, sensitivity is measured as a percentage of the full-scale output that is generated by a 94 dB SPL input. For a digital microphone, the conversion equation is

$$Sensitivity_{dBFS} = 20 \times \log_{10}\left(\frac{Sensitivity_{\%FS}}{Output_{DREF}}\right)$$

where $Output_{DREF}$ is the full-scale digital output level.

One last *very* confusing piece of this comparison is the inconsistent usage of peak and rms levels between digital and analog microphones. The microphone's acoustic input levels in dB SPL are always *rms* measurements, regardless of the type of microphone. The output of analog microphones is referenced to 1 V rms, as rms measurements are more commonly used for comparing analog audio signal levels. However, the sensitivity and output level of digital microphones are given as peak levels because they are referred to the full-scale digital word, which is a peak value. In general, this convention of using peak levels to specify the output of digital microphones must be kept in mind when configuring downstream signal processing that may rely on precise signal levels. For example, dynamic range processors (compressors, limiters, and noise gates) typically set thresholds based on rms signal levels, so a digital microphone's output must be scaled from peak to rms by lowering the dBFS value. For a sinusoidal input, the rms level is 3 dB (the logarithmic measure of (FS/√2) below the peak level; this difference between rms and peak may be different for more complex signals. For example, the ADMP421, a MEMS microphone with *pulse-density-modulated* (PDM) digital output, has a sensitivity of –26 dBFS. A 94 dB SPL sinusoidal input signal will give a –26 dBFS *peak* output level, or a –29 dBFS *rms* level.

As the outputs of digital and analog microphones have different units, comparing one type to another can be confusing; however, they share a common unit of measure in the acoustic domain, *SPL*. One may have an analog voltage output, another a modulated PDM output, and a third an I^2S output, but their maximum acoustic input and signal-to-noise ratio (SNR, the difference between the 94 dB SPL reference and the noise level) can be directly compared.

By referring to the acoustic domain, not the output format, these two specifications provide a convenient way to compare different microphones. Figure 2 shows the relationship between an acoustic input signal and the output levels of analog and digital microphones for a given sensitivity. Figure 2(a) shows the ADMP504 analog microphone, which specifies −38 dBV sensitivity and 65 dB SNR. Changing its sensitivity, relative to the 94 dB SPL reference point on the left, would result in sliding the dBV output bar up to decrease sensitivity or down to increase sensitivity.

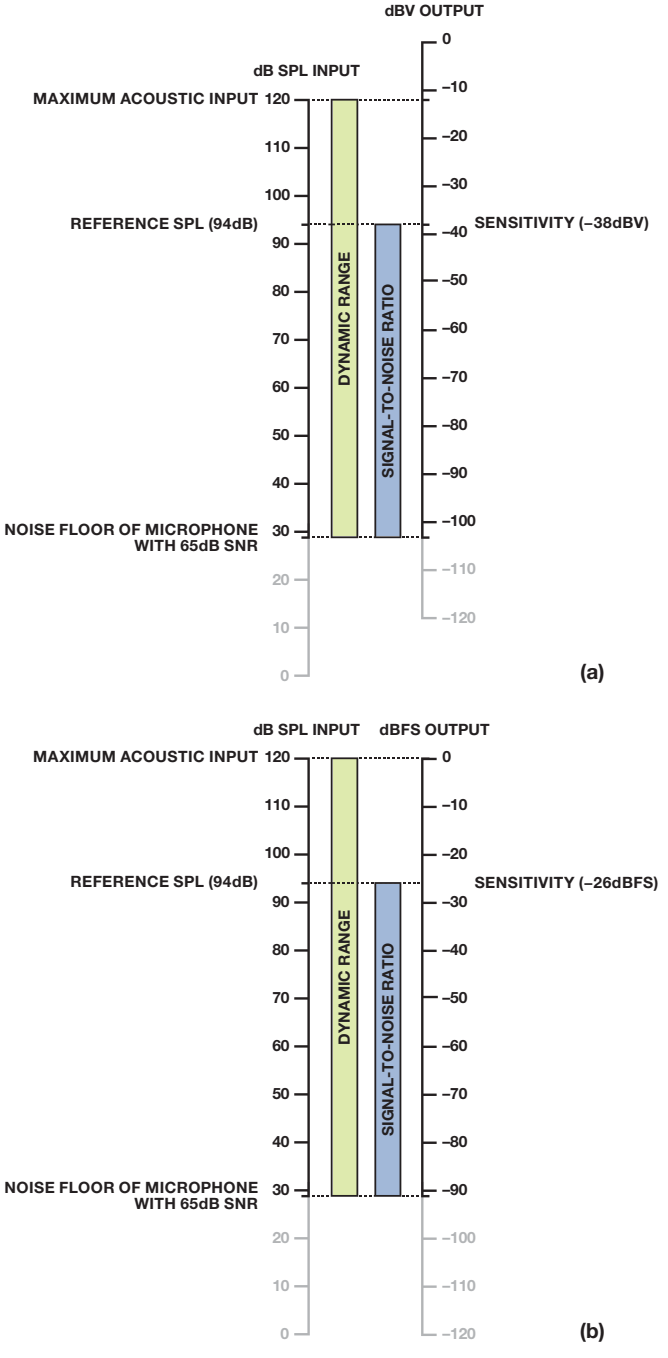

Figure 2. Mapping acoustic input level to (a) voltage output level for an analog microphone; (b) digital output level for a digital microphone.

Figure 2(b) shows the ADMP521 digital microphone, which specifies −26 dBFS sensitivity and 65 dB SNR. This illustration of the input-to-output level mapping for a digital microphone shows that the sensitivity of this microphone cannot be adjusted without breaking the mapping between the maximum acoustic input and the full-scale digital word. Specifications such as SNR, dynamic range, power supply rejection, and THD are better indicators of microphone quality than sensitivity.

Choosing Sensitivity and Setting Gain

A high sensitivity microphone isn't always *better* than a low sensitivity microphone. Sensitivity tells something about the *characteristics* of the microphone but not necessarily about its *quality*. A balance between the microphone's noise level, clipping point, distortion, and sensitivity determines whether a microphone is a good fit for a particular application. A microphone with high sensitivity may need less preamp gain before the analog-to-digital conversion, but it may have less headroom before clipping than a microphone with lower sensitivity.

In near-field applications, such as cell phones, where the microphone is close to the sound source, a microphone with higher sensitivity is more likely to reach the maximum acoustic input, clip, and cause distortion. On the other hand, a higher sensitivity may be desirable in far-field applications, such as conference phones and security cameras, where the sound is attenuated as the distance from the source to the microphone increases. Figure 3 shows how the distance of the microphone from the sound source can affect the SPL. The level of an acoustic signal decreases by 6 dB (one-half) each time the distance from the source is doubled.

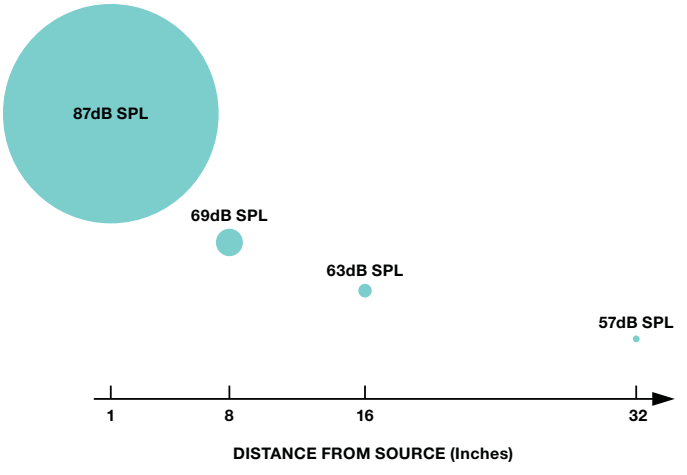

Figure 3. Sound pressure level at the microphone is reduced as the distance from the source increases.

For reference, Figure 4 shows the typical SPL of various sound sources, from quiet recording studios (below 10 dB SPL) up to the threshold of pain (above 130 dB SPL), the point at which the sound causes pain for the average person. Microphones can rarely cover all—or even most—of this range, so choosing the right microphone for the required SPL range is an important design decision. The sensitivity specification should be used to match the microphone's output signal level across the dynamic range of interest to the common signal level of the audio signal chain.

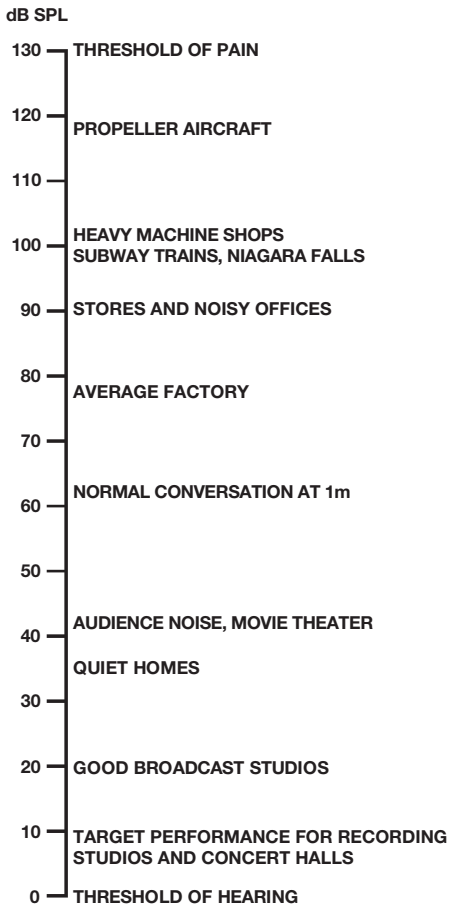

Figure 4. Sound pressure level of various sources.[1]

Analog microphones have a wide range of sensitivities. Some dynamic microphones might have sensitivity as low as –70 dBV. Some condenser microphone modules have integrated preamps so they have extra high sensitivity of –18 dBV. Most analog electret and MEMS microphones have sensitivity between –46 dBV and –35 dBV (5.0 mV/Pa to 17.8 mV/Pa). This level is a good compromise between the noise floor—which can be as low as 29 dB SPL for the ADMP504 and ADMP521 MEMS microphones—and the maximum acoustic input—which is typically about 120 dB SPL. An analog microphone's sensitivity can be tuned in the preamp circuit that is often integrated in the package with the transducer element.

Despite the perceived inflexibility of a digital microphone's sensitivity, the level of the microphone signal can be easily adjusted with gain in the digital processor. With digital gain, there is no danger of degrading the noise level of the signal as long as the processor has a sufficient number of bits to fully represent the dynamic range of the original microphone signal. In an analog design, every gain stage will introduce some noise into the signal; it is up to the system designer to ensure that each gain stage is quiet enough to keep its injected noise from degrading the audio signal. As an example, we can look at the ADMP441, a digital (I^2S) output microphone with a maximum SPL of 120 dB (–26 dBFS sensitivity) and an equivalent input noise of 33 dB SPL (61 dB SNR). The microphone's dynamic range is the difference between the largest (max SPL) and smallest (noise floor) signals it can faithfully reproduce (120 dB – 33 dB = 87 dB for the ADMP441). This dynamic range can be reproduced with a 15-bit data word. A 1-bit shift of the data in a digital word results in a 6 dB shift in the signal level, so even a 16-bit audio processor with a 98 dB dynamic range could use 11 dB of gain or attenuation before the original dynamic range is compromised. Note that in many processors, the digital microphone's maximum acoustic input is mapped to the DSP's internal full-scale level. In this case, adding any amount of gain reduces the dynamic range by an equal amount and lowers the system's clipping point. Using the ADMP441 as an example, adding 4 dB of gain in a processor with no headroom above full scale would cause the system to clip with a 116 dB SPL signal.

Figure 5 shows a digital microphone, with either I^2S or PDM output, connected directly to a DSP. In this signal chain, no intermediate gain stage is necessary because the microphone's peak output level already matches the DSP's full-scale input word.

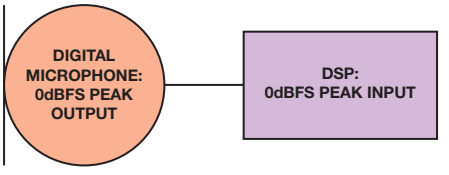

Figure 5. Digital microphone input signal chain connected directly to a DSP.

Conclusion

This article explained how to understand a microphone's sensitivity specification, how to apply it to a system's gain staging, and why, although sensitivity is related to SNR, it is not an indication of the microphone's quality as is SNR. Whether designing with an analog or digital MEMS microphone, this should help a designer choose the best microphone for an application and to get the fullest performance from that device.

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Author

Jerad Lewis [jerad.lewis@analog.com] is a MEMS microphone applications engineer at Analog Devices. He joined the company in 2001 after getting his BSEE from Penn State University. Since then, Jerad has supported various audio ICs, including SigmaDSP, converters, and MEMS microphones. He is currently pursuing an MEng degree in acoustics at Penn State University.

Staying Well Grounded

By Hank Zumbahlen

Grounding is undoubtedly one of the most difficult subjects in system design. While the basic concepts are relatively simple, implementation is very involved. Unfortunately, there is no "cookbook" approach that will guarantee good results, and there are a few things that, if not done well, will probably cause headaches.

For linear systems, the ground is the reference against which we base our signal. Unfortunately, it has also become the return path for the power-supply current in unipolar supply systems. Improper application of grounding strategies can cripple performance in high-accuracy linear systems.

Grounding is an issue for all analog designs, and it is a fact that proper implementation is no less essential in PCB-based circuits. Fortunately, certain principles of quality grounding, especially the use of ground planes, are intrinsic to the PCB environment. Since this factor is one of the more significant advantages to PCB-based analog designs, appreciable discussion here is focused on it.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or, simply, excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques, enable control of such parasitic voltages.

An important topic to be discussed is grounding techniques appropriate for a mixed-signal, analog/digital environment. Indeed, the single issue of quality grounding can—and must—influence the entire layout philosophy of a high-performance mixed-signal PCB design.

Today's signal processing systems generally require mixed-signal devices, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), as well as fast digital signal processors (DSPs). Requirements for processing analog signals that have a wide dynamic range impose the need to use high-performance ADCs and DACs. Maintaining a wide dynamic range with low noise in a hostile digital environment is dependent upon using good high-speed circuit design techniques, including proper signal routing, decoupling, and grounding.

In the past, "high-precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criterion. However, the following two examples show that, in practice, most of today's signal processing ICs are really "high-speed," and must, therefore, be treated as such in order to maintain high performance. While certainly true of DSPs, it is also true for ADCs and DACs.

All sampling ADCs (those employing an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high-speed clocks with fast rise and fall times (generally a few nanoseconds), so they must be treated as high-speed devices, even though throughput rates may appear low. For example, a medium-speed 12-bit successive-approximation (SAR) ADC may operate from a 10-MHz internal clock, while the sampling rate is only 500 kSPS.

Sigma-delta (Σ-Δ) ADCs also require high-speed clocks because of their high oversampling ratios. Even high resolution, so-called "low frequency" industrial measurement ADCs (such as the AD77xx-series), with throughputs of 10 Hz to 7.5 kHz, operate on 5-MHz or higher-frequency clocks and offer resolutions to 24 bits.

To further complicate the issue, mixed-signal ICs have both analog and digital ports, adding to the confusion with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types require different treatment for optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, so the purpose of this article is to describe a general grounding philosophy that will work for most mixed-signal devices, without the need to know the specific details of their internal circuits.

From the above, it should be clear that the issue of grounding cannot be handled in a "cookbook" approach. Unfortunately, we cannot provide a list of things to do that will guarantee success. We can say that not doing certain things will probably lead to difficulties. And what works in one frequency range may not necessarily work in another frequency range. And, often, there are competing requirements. The key to handling grounding is to understand how the currents flow.

Star Ground

The "star" ground philosophy builds on the theory that all voltages in a circuit are referred to a single ground point, known as the *star ground* point. This can be better understood by a visual analogy—the multiple conductors extending radially from the common schematic ground to resemble a star. The star point need not look like a star—it may be a point on a ground plane—but the key feature of the star ground system is that all voltages are measured with respect to a particular point in the ground network, not just to an undefined "ground" (wherever one can clip a probe).

The star grounding philosophy, while reasonable theoretically, is difficult to implement in practice. For example, if we design a star ground system, drawing out all signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, implementation problems arise. When the power supplies are added to the circuit diagram, they either add unwanted ground paths, or their supply currents flowing in the existing ground paths are large enough, or noisy enough (or both), to corrupt the signal transmission. This particular problem can often be avoided by having separate power supplies (and, thus, separate ground returns) for the various portions of the circuit. For example, separate analog and digital supplies with separate analog and digital grounds, joined at the star point, are common in mixed-signal applications.

Separate Analog and Digital Grounds

It is a fact of life that digital circuitry is noisy. Saturating logic, such as TTL and CMOS, draws large, fast current spikes from its supply during switching. Logic stages, with hundreds of millivolts (or more) of noise immunity, usually have little need for high levels of supply decoupling. On the other hand, analog circuitry is quite vulnerable to noise—on both power supply rails and grounds—so it is sensible to separate analog and digital circuitry to prevent digital noise from corrupting analog performance. Such separation involves separation of both ground returns *and* power rails—which can be inconvenient in a mixed-signal system.

Nevertheless, if a high-accuracy mixed-signal system is to deliver full performance, it is essential to have separate analog and digital grounds and separate power supplies. The fact that some analog circuitry will "operate" (function) from a single +5-V supply does *not* mean that it may optimally be operated from the same noisy +5-V supply as the microprocessor, dynamic RAM, electric fan, and other high-current devices! The analog portion must *operate at full performance from such a supply*, not just be functional. By necessity, this distinction will require very careful attention to both the supply rails and the ground interfacing.

Note that the analog and digital grounds in a system must be joined at some point to allow signals to be referred to a common potential. This *star point*, or analog/digital common point, is carefully chosen so as not to introduce digital currents into the ground of the analog part of the system—it is often convenient to make the connection at the power supplies.

Many ADCs and DACs have separate *analog ground* (AGND) and *digital ground* (DGND) pins. On the device data sheets, users are often advised to connect these pins together at the package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

There is, in fact, no conflict. The labels, "analog ground" and "digital ground," on these pins refer to the internal parts of the converter to which the pins are connected and not to the system grounds to which they must go. For an ADC, these two pins should generally be joined together and to the *analog* ground of the system. It is not possible to join the two pins within the IC package because the analog part of the converter cannot tolerate the voltage drop resulting from the digital current flowing in the bond wire to the chip. But they can be tied together *externally*.

Figure 1 illustrates this concept of ground connections for an ADC. If these pins are connected in this way, the digital noise immunity of the converter is diminished, somewhat, by the amount of common-mode noise between the digital and analog system grounds. However, since digital noise immunity is often of the order of hundreds or thousands of millivolts, this factor is unlikely to be important.

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be kept quite small, and they can be minimized by ensuring that the converter outputs don't see heavy loads. A good way to do this is to use a low input current buffer at the ADC output, such as a CMOS buffer-register IC.

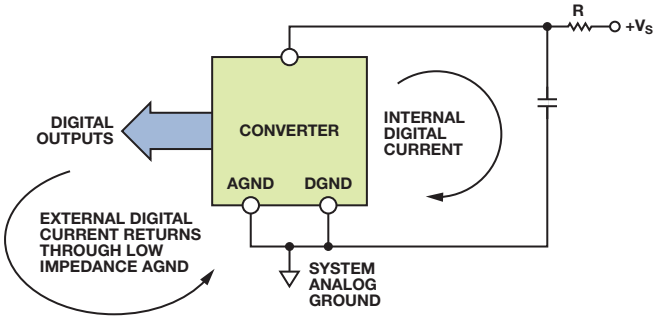

Figure 1. Analog ground (AGND) and digital ground (DGND) pins of a data converter should be returned to system analog ground.

If the logic supply to the converter is isolated with a small resistance, and decoupled to analog ground with a local 0.1-µF (100-nF) capacitor, all the fast-edge digital currents of the converter will return to ground through the capacitor and will not appear in the external ground circuit. If a low-impedance analog ground is maintained—as it should be for adequate analog performance—additional noise due to the external digital ground current should rarely present a problem.

Ground Planes

Related to the star ground system discussed earlier is the use of a *ground plane*. To implement a ground plane, one side of a double-sided PCB (or one layer of a multilayer one) is made of continuous copper and used as ground. The theory behind this is that the large amount of metal will have as low a resistance as is possible. Because of the large flattened conductor pattern, it will also have as low an inductance as possible. It then offers the best possible conduction, in terms of minimizing spurious ground difference voltages, across the conducting plane.

Note that the ground plane concept can also be extended to include *voltage planes*. A voltage plane offers advantages similar to a ground plane— a very low impedance conductor—but is dedicated to one (or more) of the system supply voltages. A system can thus have more than one voltage plane, as well as a ground plane.

While ground planes solve many ground impedance problems, they aren't a panacea. Even a continuous sheet of copper foil has residual resistance and inductance; in some circumstances, these can be enough to prevent proper circuit function. Designers should be wary of injecting very high currents in a ground plane because they can produce voltage drops that interfere with sensitive circuitry.

Maintaining a low impedance, large area ground plane is of critical importance to all analog circuits today. The ground plane not only acts as a low impedance return path for decoupling high-frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high-speed digital or analog signals using transmission line techniques (microstrip or stripline), where controlled impedances are required.

The use of "bus wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20 nH/in inductance. A transient current having a slew-rate of 10 mA/ns created by a logic signal would develop an unwanted voltage drop of 200 mV when flowing through one inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20\ \text{nH} \times \frac{10\ \text{mA}}{\text{ns}} = 200\ \text{mV} \quad (1)$$

For a signal having a 2-V peak-to-peak range, this translates into an error of about 200 mV, or 10% (approximately "3.5-bit accuracy"). Even in all-digital circuits, this error would result in considerable degradation of the logic noise-margins.

Figure 2 shows a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits; this causes the interaction and resulting error.

A possible solution is to make the digital return current path directly to the GND REF, as shown in the bottom figure. This illustrates the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system that contains multiple high-frequency return paths is difficult. The physical length of the individual return current wires will introduce parasitic resistance and inductance, making it difficult to obtain a low-impedance ground at high frequencies. In practice, the current returns must consist of large area ground planes to obtain low impedance to high-frequency currents. Without a low-impedance ground plane, it is almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available. They have spring-loaded gold contacts, which make good electrical and mechanical connection to the IC pins. However, multiple insertions may degrade their performance.

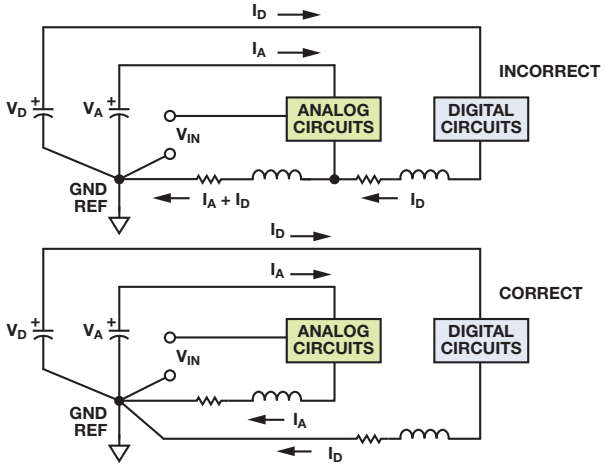

Figure 2. Digital currents flowing in analog return path create error voltages.

Power supply pins should be decoupled directly to the ground plane using low-inductance, ceramic surface-mount capacitors. If through-hole mounted ceramic capacitors must be used, their lead length should be less than 1 mm. The ceramic capacitors should be as close as possible to the IC power pins. Ferrite beads may also be required for noise filtering.

So, the more ground the better—right? Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, these can be enough to prevent proper circuit function. Figure 3 shows such a problem—and a possible solution.

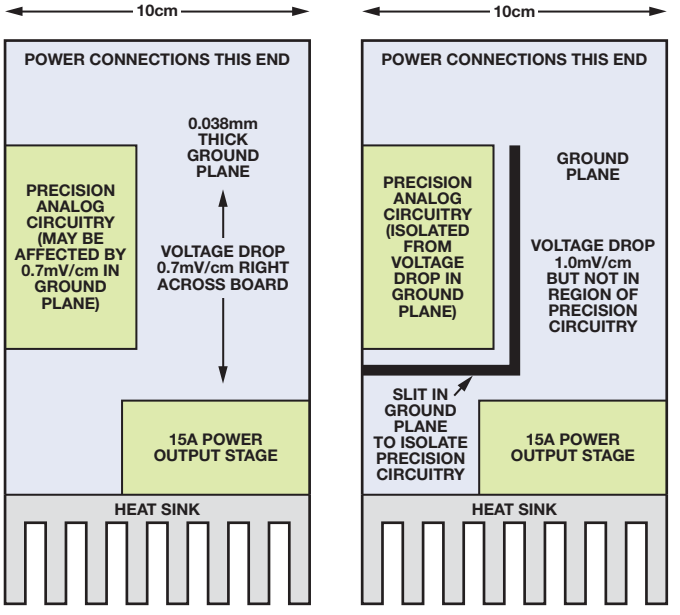

Figure 3. A slit in the ground plane can reconfigure current flow for better accuracy.

Due to the realities of the mechanical design, the power input connector is on one side of the board, and the power output section—which needs to be near the heat sink—is on the other side. The board has a 100-mm wide ground plane and a power amplifier that draws 15 A. If the ground plane is 0.038-mm thick and 15 A flows in it, there will be a voltage drop of 68 μV/mm. This voltage drop would cause serious problems for the ground-referenced precision analog circuitry sharing the PCB. The ground plane can be slit so that high current does not flow in the precision circuitry region; instead, it is forced to flow around the slit. This can prevent a grounding problem (which in this case it does), even though the voltage gradient increases in those parts of the ground plane where the current flows.

One thing to definitely avoid in multiple ground plane systems is overlapping the ground planes, especially analog and digital grounds. This will cause capacitive coupling of noise from one (probably digital ground) into the other. Remember that a capacitor is made up of two conductors (the two ground planes) separated by an insulator (the PC board material).

Grounding and Decoupling Mixed-Signal ICs with Low Digital Currents

Sensitive analog components, such as amplifiers and voltage references, are always referenced and decoupled to the *analog* ground plane. The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane. At first glance, this may seem somewhat contradictory since a converter has analog and digital interfaces and usually has pins designated *analog ground* (AGND) and *digital ground* (DGND). Figure 4 will help to explain this apparent dilemma.

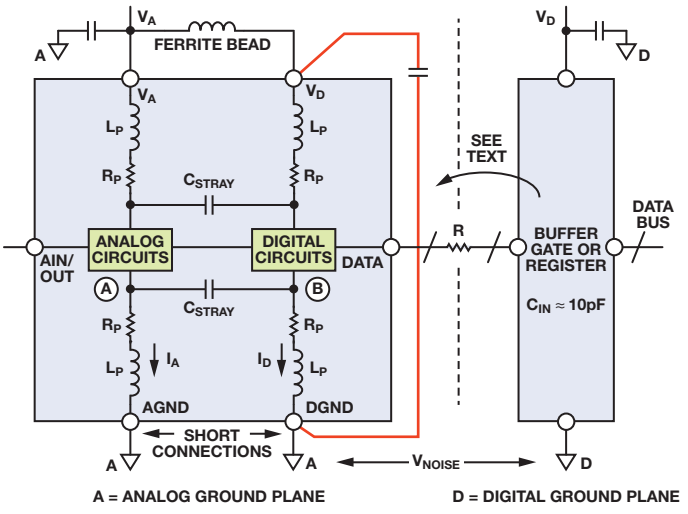

Figure 4. Proper grounding of mixed-signal ICs with low internal digital currents.

Inside an IC that has both analog and digital circuits (an ADC or a DAC, for example), the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 4 shows a simple model of a converter. There is nothing the IC designer can do about the wire bond inductance and resistance associated with connecting the bond pads on the chip to the package pins, except to realize it's there. The rapidly changing digital currents produce a voltage at Point B that will inevitably couple into Point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2 pF of unavoidable stray capacitance between every adjacent pin-pair of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent additional coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at Point B which will, in turn, couple more digital noise into the analog circuit through the stray capacitance. Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins, inviting disaster!

The name "DGND" tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system. It could be better described as the IC's internal "Digital Return."

It is true that the grounding arrangement described may inject a small amount of digital noise onto the analog ground plane, but these currents should be quite small and can be minimized by ensuring that the converter's output does not drive a large fanout (they normally can't, by design). Minimizing the fanout on the converter's digital port (which, in turn, means lower currents) also keeps the converter's logic transition waveforms relatively free of ringing, minimizes digital switching currents, and thereby reduces any coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead, as shown in Figure 4. The internal transient digital currents of the converter will flow in the small loop from V_D through the decoupling capacitor and to DGND (this path is shown in red on the diagram). The transient digital currents will, therefore, not appear on the external analog ground plane but are confined to the loop. The V_D pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. The decoupling capacitors should be low inductance ceramic types, typically between 0.01 μF (10 nF) and 0.1 μF (100 nF).

Again, no single grounding scheme is appropriate for all applications. However, by understanding the options and planning ahead, problems can be minimized.

Treat the ADC Digital Outputs with Care

It is always a good idea to place a data buffer adjacent to the converter to isolate the digital output from data bus noise (Figure 4). The data buffer also serves to minimize loading on the converter's digital outputs and acts as a Faraday shield between the digital outputs and the data bus (Figure 5). Even though many converters have three-state outputs/inputs, these registers are on the die; they allow data pin signals to couple into sensitive areas, so the isolation buffer still represents good design practice. In some cases, it may even be desirable to provide an additional data buffer on the analog ground plane next to the converter output to provide greater isolation.

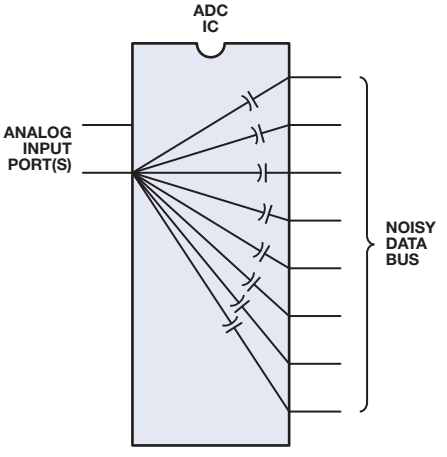

Figure 5. A high-speed ADC using a buffer/latch at the output shows enhanced immunity to digital data bus noise.

The series resistors (labeled "R" in Figure 4) between the ADC output and the buffer register input help to minimize the digital transient currents, which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register's input capacitance acts as a low-pass filter to slow down the fast edges.

A typical CMOS gate, combined with PCB trace and a through-hole, will create a load of approximately 10 pF. A logic output slew rate of 1 V/ns will produce 10 mA of dynamic current if there is no isolation resistor:

$$\Delta i = C \frac{\Delta v}{\Delta t} = 10\ pF \times \frac{1\ V}{ns} = 10\ mA \qquad (2)$$

A 500 Ω series resistor will minimize the transient output current and result in rise- and fall-times of approximately 11 ns when driving the 10 pF input capacitance of the register:

$$t_r = 2.2 \times t = 2.2 \times R \times C = 2.2 \times 500\ \Omega \times 10\ pF = 11\ ns \qquad (3)$$

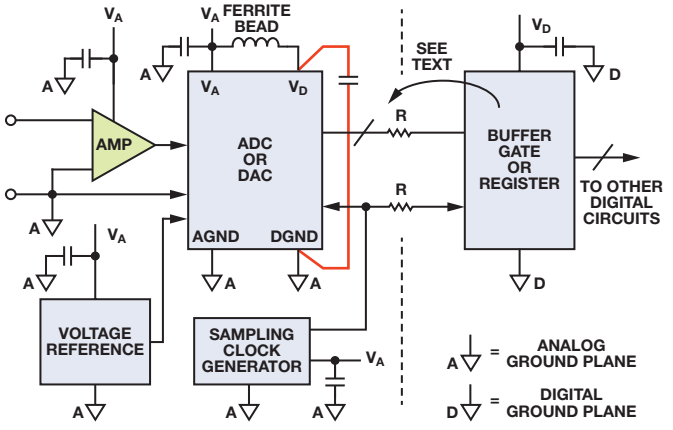

Figure 6. Grounding and decoupling points.

TTL registers should be avoided; they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground planes reduces the noise margin at the converter digital interface. Since digital noise immunity is of the order of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance to maintain the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300 mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply or filtered, as shown in Figure 6. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane, as shown in Figure 6. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but *be very cautious*.

In some cases, it may not be possible to connect V_D to the analog supply. Some high-speed ICs may have their analog circuits powered by +5 V, but the digital interface is powered by +3.3 V or less, to interface to external logic. In this case, the +3.3-V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3.3-V digital logic supply.

The sampling clock-generation circuitry should be treated like analog circuitry and also be grounded and heavily decoupled to the analog ground plane. Phase noise on the sampling clock degrades system signal-to-noise ratio (SNR); this will be discussed shortly.

Sampling Clock Considerations

In a high-performance sampled-data system, a low-phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock, because sampling clock jitter modulates the analog input/output signal and raises the noise-and-distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, along with the op amp and the ADC.

The effect of sampling clock jitter on ADC SNR is given approximately by Equation 4:

$$\mathrm{SNR} = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right] \quad (4)$$

where f is the analog input frequency, SNR is that of a perfect ADC of infinite resolution, and the only source of noise is rms sampling clock jitter, t_j. Working through a simple example, if t_j = 50 ps (rms), and f = 100 kHz, then SNR = 90 dB, equivalent to approximately 15-bit dynamic range.

It should be noted that t_j in the above example is actually the root-sum-square (rss) value of the external clock jitter *and* the internal ADC clock jitter (called *aperture jitter*). However, in most high-performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to render the sampling clock as noise-free as possible with the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low-jitter (less than 5 ps rms) CMOS-compatible outputs.

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, system constraints may not permit this. In many cases, the sampling clock must be derived from a higher frequency multipurpose system clock that is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and produce unwanted harmonics.

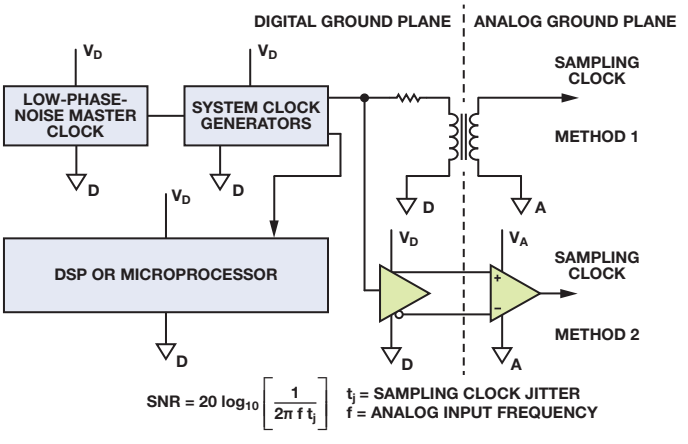

Figure 7. Sampling clock distribution from digital to analog ground planes.

This can be relieved somewhat by transmitting the sampling clock signal as a differential signal, using either a small RF transformer—as shown in Figure 7—or a high-speed differential driver and receiver. If the latter are used, they should be ECL to minimize phase jitter. In a single +5-V supply system, ECL logic can be connected between ground and +5 V (PECL), with the outputs ac-coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low-phase-noise crystal oscillator.

The Origins of the Confusion About Mixed-Signal Grounding

Most data sheets for ADCs, DACs, and other mixed-signal devices discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane, with the further recommendation that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point, as shown in Figure 8. This essentially creates the system "star" ground at the mixed-signal device. All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed-signal device.

While this approach will generally work in a simple system, with a single PCB and a single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or even on the same PCB), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multicard systems; the approach discussed earlier should be used for mixed-signal ICs with low digital currents.

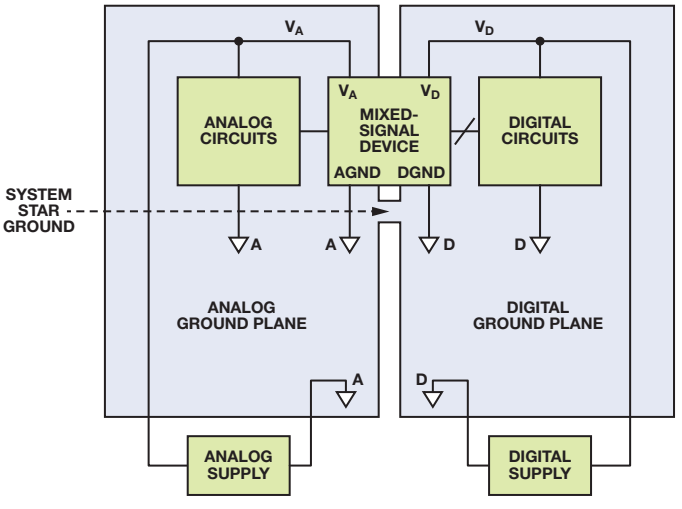

Figure 8. Grounding mixed-signal ICs: single PCB (typical evaluation/test board).

Grounding for High-Frequency Operation

The "ground plane" layer is often advocated as the best return for power and signal currents, while providing a reference node for converters, references, and other subcircuits. However, even extensive use of a ground plane does not ensure a high-quality ground reference for an ac circuit.

The simple circuit of Figure 9, built on a two-layer printed circuit board, has an ac + dc current source on the top layer connected to Via 1 at one end and to Via 2 by way of a single U-shaped copper trace. Both vias go through the circuit board and connect to the ground plane. Ideally, the impedance in the top connector and in the ground return between Via 1 and Via 2 would be zero, and the voltage appearing across the current source would also be zero.

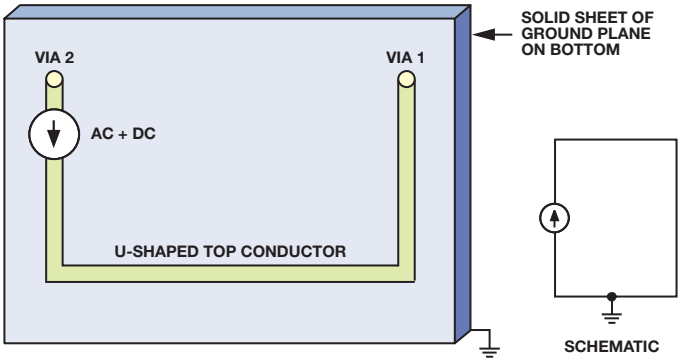

Figure 9. Schematic and layout of current source with U-shaped trace on PCB and return through ground plane.

This simple schematic hardly begins to show the underlying subtleties, but an understanding of how the current flows in the ground plane from Via 1 to Via 2 discloses the realities and shows how ground noise in high-frequency layouts can be avoided.

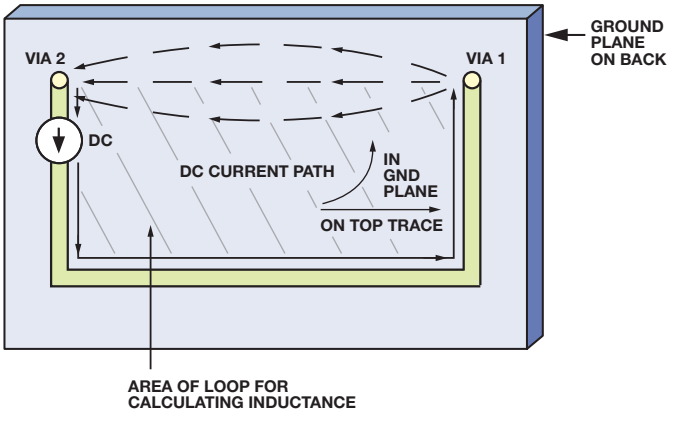

Figure 10. DC current flow for PCB shown in Figure 9.

The dc current flows in the manner shown in Figure 10, taking the path of least resistance from Via 1 to Via 2 in the ground plane. Some current spreading occurs, but little current flows at a substantial distance from this path. In contrast, the ac current takes the path of least *impedance*, which, in turn, depends on inductance.

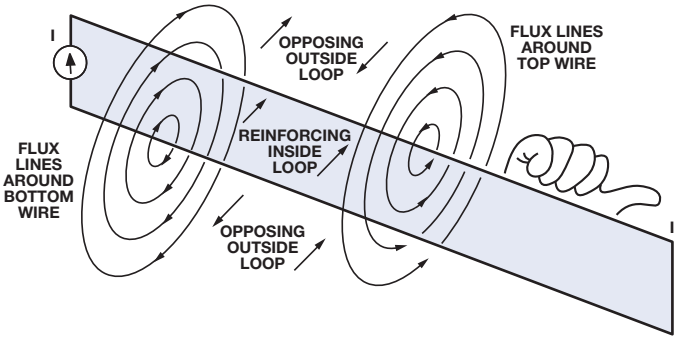

Figure 11. Magnetic field lines and inductive loop (right hand rule).

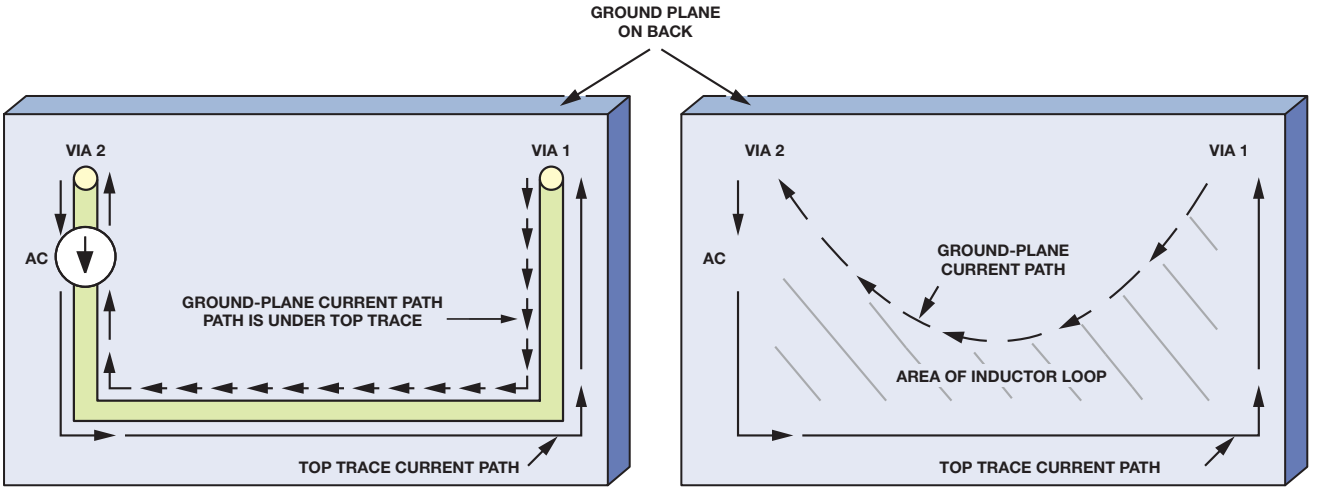

Figure 12. AC current path without resistance (left) and with resistance (right) in the ground plane.

Inductance is proportional to the area of the loop made by the current flow; the relationship can be illustrated by the right hand rule and the magnetic field shown in Figure 11. Inside the loop, current along all parts of the loop produces magnetic field lines that add constructively. Away from the loop, however, field lines from different parts add destructively, thus the field is confined principally within the loop. The larger the loop, the greater the inductance, which means that, for a given current level, a larger loop has more stored magnetic energy (Li^2) and greater impedance ($X_L = j\omega L$), and, hence, will develop more voltage at a given frequency.

Which path will the current choose in the ground plane? Naturally, the lowest-impedance path. Considering the loop formed by the U-shaped surface lead and the ground plane, and neglecting resistance, the high-frequency ac current will follow the path with the least inductance, hence the least area.

In the example shown, the loop with the least area is quite evidently formed by the U-shaped top trace and the portion of the ground plane directly underneath it. So while Figure 10 shows the dc current path, Figure 12 shows the path that most of the ac current takes in the ground plane, where it finds minimum area, directly under the U-shaped top trace. In practice, the resistance in the ground plane causes the low- and mid-frequency current to flow somewhere between straight back and directly under the top conductor. However, the return path is nearly under the top trace at frequencies as low as 1 MHz or 2 MHz.

Be Careful with Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must, by necessity, flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 13, where Conductors A and B must cross one another.

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first signal and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multilayer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multilayer boards are expensive and harder to troubleshoot than simpler double-sided boards, but they do offer even better shielding and signal routing. The principles involved remain unchanged, but the range of layout options is increased.

The use of double-sided or multilayer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high-performance mixed-signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

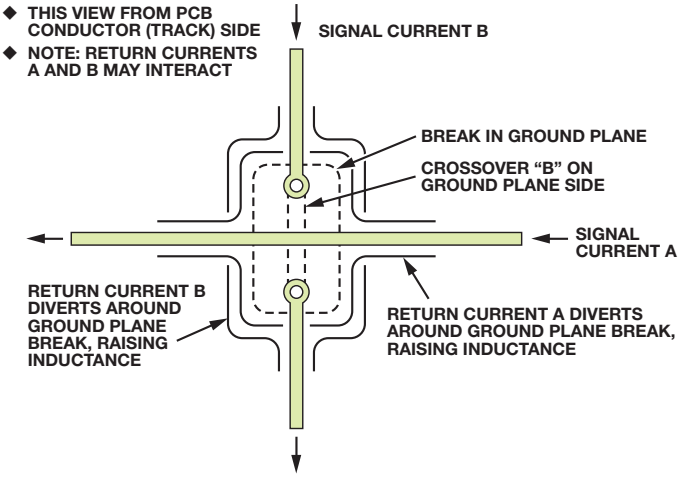

Figure 13. A ground-plane break raises circuit inductance and increases vulnerability to external fields.

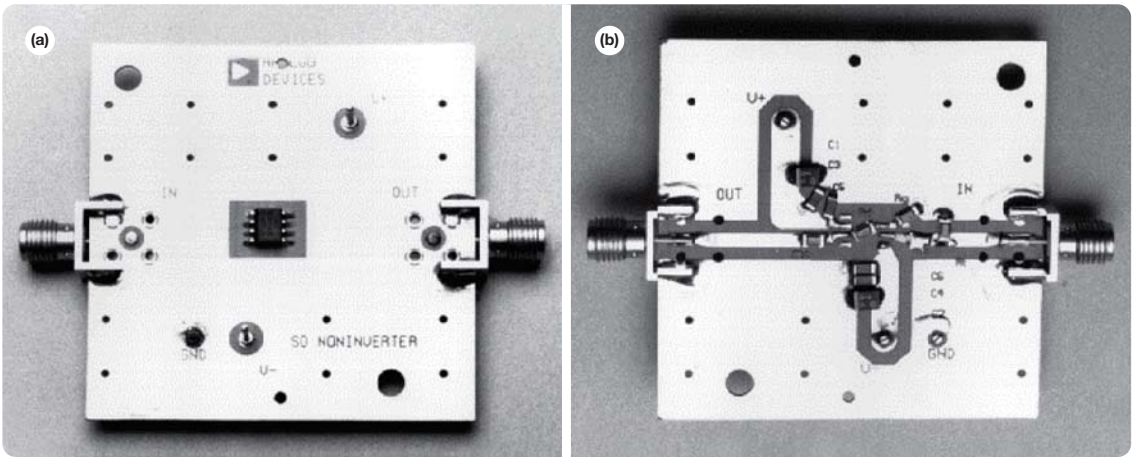

Figure 14. AD8001AR evaluation board—top view (a) and bottom view (b).

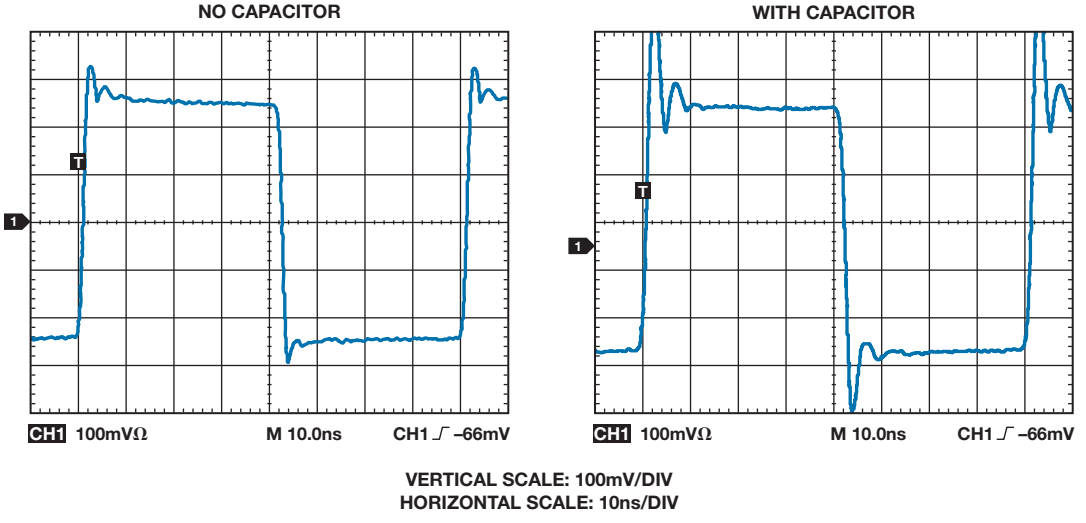

Figure 15. Effects of 10-pF stray capacitance on the inverting input on amplifier (AD8001) pulse response.

In one other instance, less is more. High-frequency, current-feedback amplifiers are very sensitive to capacitance around their inverting inputs. An input trace running next to a ground plane can have just the sort of capacitance that may cause problems. Remember that a capacitor consists of two conductors (the trace and the ground plane) separated by an insulator (the board and possible solder mask). To that end, ground planes should be cut back from the input pins, as shown in Figure 14, which is an evaluation board for the AD8001 high-speed current feedback amplifier. The effect of even small capacitance on the input of a current feedback amplifier is shown in Figure 15. Note the ringing on the output.

Grounding Summary

There is no single grounding method that will guarantee optimum performance 100% of the time. This article presents a number of possible options, depending upon the characteristics of the particular mixed-signal devices in question. When laying out the initial PC board, it is helpful to provide for as many options as possible.

It is *mandatory* that at least one layer of the PC board be dedicated to ground plane! The initial board layout should provide for nonoverlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required—and also so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should, in general, always be connected to the analog ground plane. An exception to this is DSPs with internal phase-locked loops (PLLs), such as the ADSP-21160 SHARC® processor. The ground pin for the PLL is labeled AGND but should be connected directly to the digital ground plane for the DSP.

Acknowledgment

The material presented in this article was compiled from many contributors, including James Bryant, Mike Byrne, Walt Jung, Walt Kester, Ray Stata, and the engineering staff at Analog Devices.

(references can be found on Page 27)

Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors

By Marcus O'Sullivan

Introduction

Current-sense resistors, which come in a variety of shapes and sizes, are used to measure current in many automotive, power control, and industrial systems. When using very low value resistors (a few milliohms or less), the resistance of the solder becomes a substantial portion of the sense element resistance and adds significantly to the measurement error. High-accuracy applications often use 4-terminal resistors and Kelvin sensing to reduce this error, but these special-purpose resistors can be expensive. In addition, the size and design of the resistor pads play a crucial role in determining the sense accuracy when measuring large currents. This article describes an alternative approach that enables high-accuracy Kelvin sensing using a standard, low-cost, 2-pad sense resistor with a 4-pad layout. Figure 1 shows the test board used to characterize the errors caused by five different layouts.

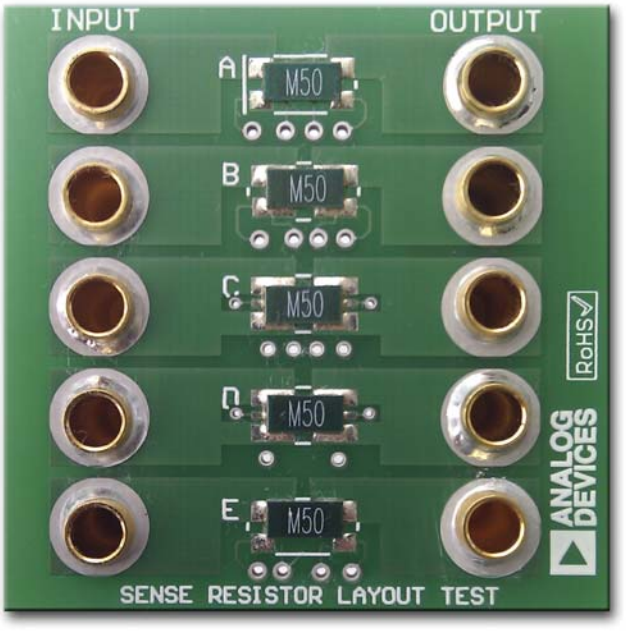

Figure 1. Sense resistor layout test PCB.

Current-Sense Resistor

Available in resistance values as low as 0.5 mΩ, commonly used current-sense resistors packaged in a 2512 case can dissipate up to 3 W. In order to highlight the worst-case errors, these experiments employ a 0.5-mΩ, 3-W resistor with 1% tolerance (part number ULRG3-2512-0M50-FLFSLT from Welwyn/TTelectronics). Its dimensions and the standard 4-wire footprint are shown in Figure 2.

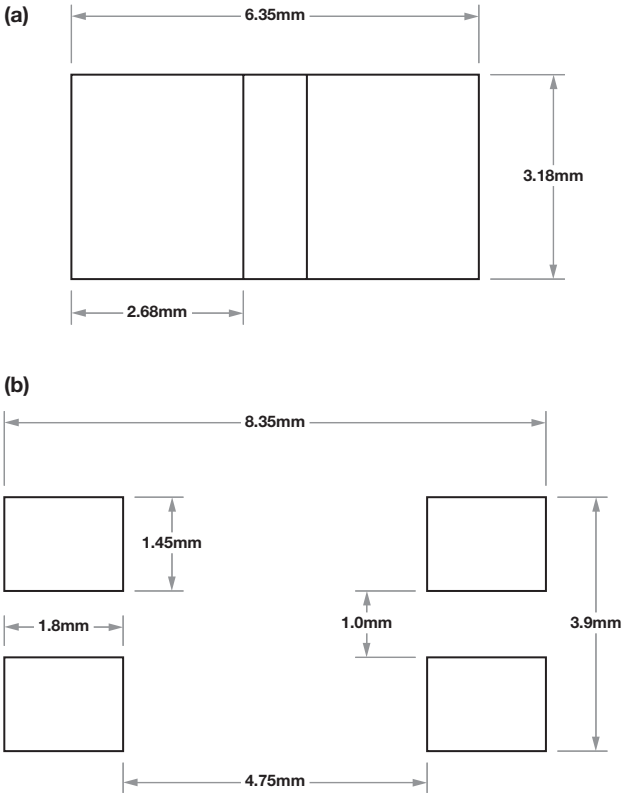

Figure 2. (a) ULRG3-2512-0M50-FLFSLT resistor dimensions; (b) Standard 4-pad footprint.

Traditional Footprint

For Kelvin sensing, pads in the standard 2-wire footprint must be divided to provide separate paths for the system currents and the sense currents. Figure 3 shows an example of such a layout. The system current takes the path shown by the red arrows. If a simple 2-pad layout was used, the total resistance would be:

$$R_{TOTAL} = R_{SENSE} + (2 \times R_{SOLDER})$$

To avoid the additional resistance, voltage sensing traces need to be routed right to the sense resistor pad. The system current will still cause a significant voltage drop across the upper solder joints, but the sense currents will cause a negligible voltage drop across the lower solder joints. This split pad approach thus removes the solder joint resistance from the measurement and improves the total system accuracy.

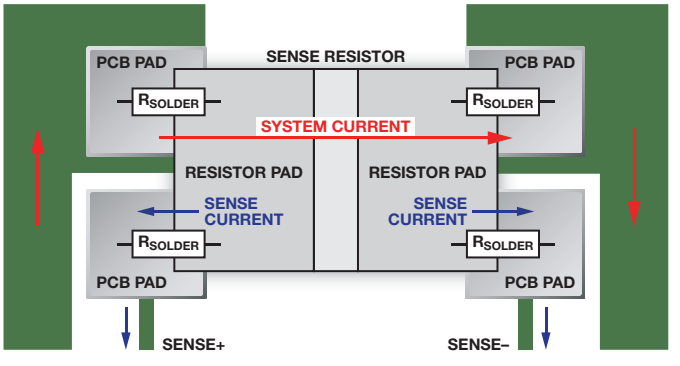

Figure 3. Kelvin sensing.

Optimizing the Kelvin Footprint

The layout shown in Figure 3 is a significant improvement on the standard 2-pad approach, but with very low value resistors (0.5 mΩ or less), the physical location of the sensing point on the pad and the symmetry of the current flow through the resistor become more significant. For example, the ULRG3-2512-0M50-FLFSLT is a solid metal-alloy resistor, so every millimeter of the resistor along the pad will influence the effective resistance. Using a calibrated current, an optimum sensing layout was determined by comparing the voltage drops across five custom footprints.

Test PCB

Figure 4 shows five layout patterns, labeled A though E, created on a test PCB. Where possible, traces were routed to test points at different locations along the sense pads, as indicated by the color coded dots. The individual resistor footprints are:

A. Standard 4-wire resistor based on 2512 recommended footprints (see Figure 2(b)). Sense point pairs (**X** and **Y**) at the outer and inner edges of the pads (x-axis).

B. Similar to A but with pads elongated closer inwards to allow better coverage of the pad area (see Figure 2(a)). Sense points at the center and end of the pads.

C. Provides more symmetrical system current flow by using both sides of the pad. Also moves sense point to a more central location. Sense points are at the center and end of the pads.

D. Similar to C but with system current pads joined at the innermost point. Only the outer sense points are used.

E. Hybrid of A and B. The system current flows through the wider pads and the sense current flows through the smaller pads. Sense points are at the outer and inner edges of the pads.

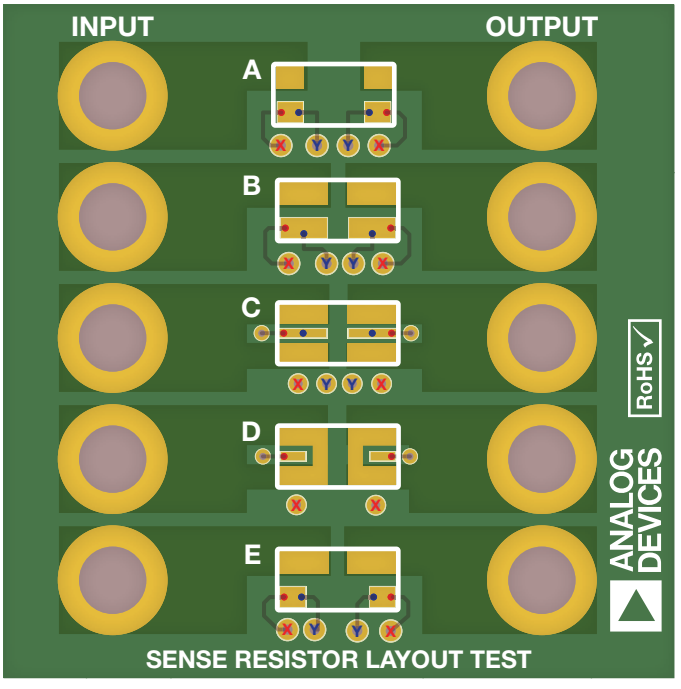

Figure 4. Test PCB layout.

Solder was applied using a stencil and reflowed in a reflow oven. The ULRG3-2512-0M50-FLFSLT resistor was used.

Test Procedure

The test setup is shown in Figure 5. A calibrated current of 20 A was passed through each resistor while the resistor was kept at 25°C. The resulting differential voltage was measured less than 1 second after the load current was enabled to prevent the resistor temperature from rising by more than 1°C. The temperature of each resistor was monitored to ensure the test results were recorded at 25°C. At 20 A, the ideal voltage drop across a 0.5-mΩ resistor is 10 mV.

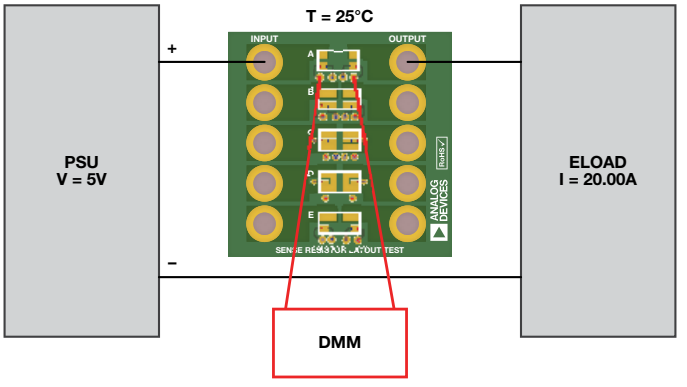

Figure 5. Test setup.

Test Results

Table 1 shows the measured data using the sense pad locations shown in Figure 4.

Table 1. Measured Voltages and Errors

Footprint	Sense Pad	Measured (mV)	Error (%)
A	Y	9.55	4.5
	X	9.68	3.2
B	Y	9.50	5
	X	9.55	4.5
C	Y	9.80	2
	X	9.90	1
D	X	10.06	0.6
E	Y	9.59	4.1
	X	9.60	4
	Top pad*	12.28	22.8

**Without Kelvin sensing. Voltage was measured across the main high-current pad to demonstrate the error associated with the solder resistance.*

Observations

1. Footprints C and D exhibit the lowest errors, with comparable results and variation within the individual resistor tolerance. Footprint C is preferred as it is less likely to cause problems related to component placement tolerances.
2. The sense points at the outer extremity of the resistors provide the most accurate results in each case. This indicates the resistors are sized by the manufacturer to the entire length.
3. Note the 22% error associated with the solder resistance without using Kelvin sensing. This is an equivalent solder resistance of about 0.144 mΩ.
4. Footprint E demonstrates the effects of asymmetrical pad layout. During reflow, the component is pulled to the pad with the most solder. This type of footprint should be avoided.

Conclusion

Based on the results shown, the optimum footprint is C, with an expected measurement error of less than 1%. Recommended dimensions of this footprint are shown in Figure 6.

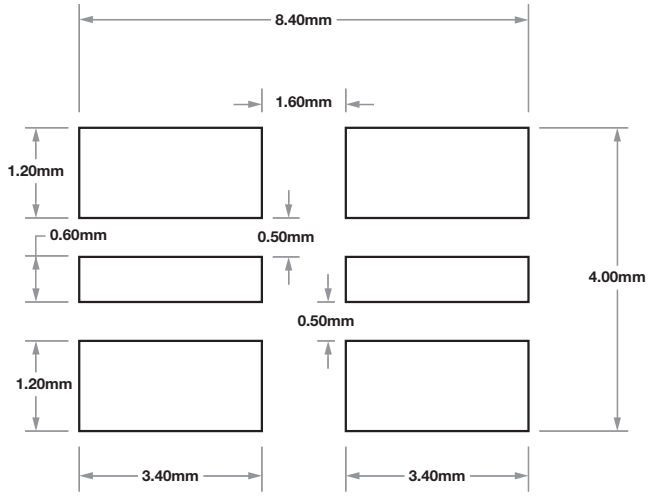

Figure 6. Optimum footprint dimensions.

The routing of the sense trace also had an impact on the measurement accuracy. To achieve the highest accuracy, the sense voltage should be measured at the edge of the resistor. Figure 7 shows a recommended layout using vias to route the outer edge of the pad to another layer, thus avoiding cutting the main power plane.

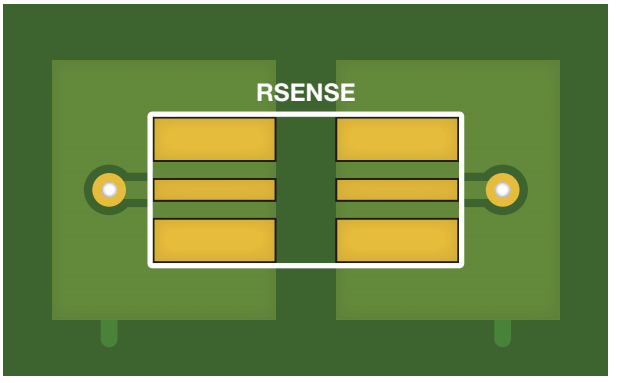

Figure 7. Recommended PCB trace routing.

The data in this article may not be applicable to all resistors, and results may vary, depending on resistor composition and size. Resistor manufacturers should be consulted. It is the responsibility of the user to ensure that the layout dimensions and structure of the footprint comply with individual SMT manufacturing requirements. Analog Devices, Inc., does not accept responsibility for any issues that may arise as a result of using this footprint.

Author

Marcus O'Sullivan [marcus.osullivan@analog.com] joined Analog Devices in 1999 and works as an applications engineer with the Power Management Group. He holds a BEng degree in electronic engineering from the University of Limerick.

(continued from Page 24)

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Author

Louis "Hank" Zumbahlen [hank.zumbahlen@analog.com] has worked at ADI since 1989, originally as a field applications engineer based in California. For the last several years, he has been involved with training and seminar development as a senior staff applications engineer. Previously, he held a similar position at Signetics (Philips)—and positions as a design engineer at several companies, primarily in the test and measurement areas. Hank has a BSEE from the University of Illinois. He is the author of *Linear Circuit Design Handbook* (Newnes-Elsevier 2008).

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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