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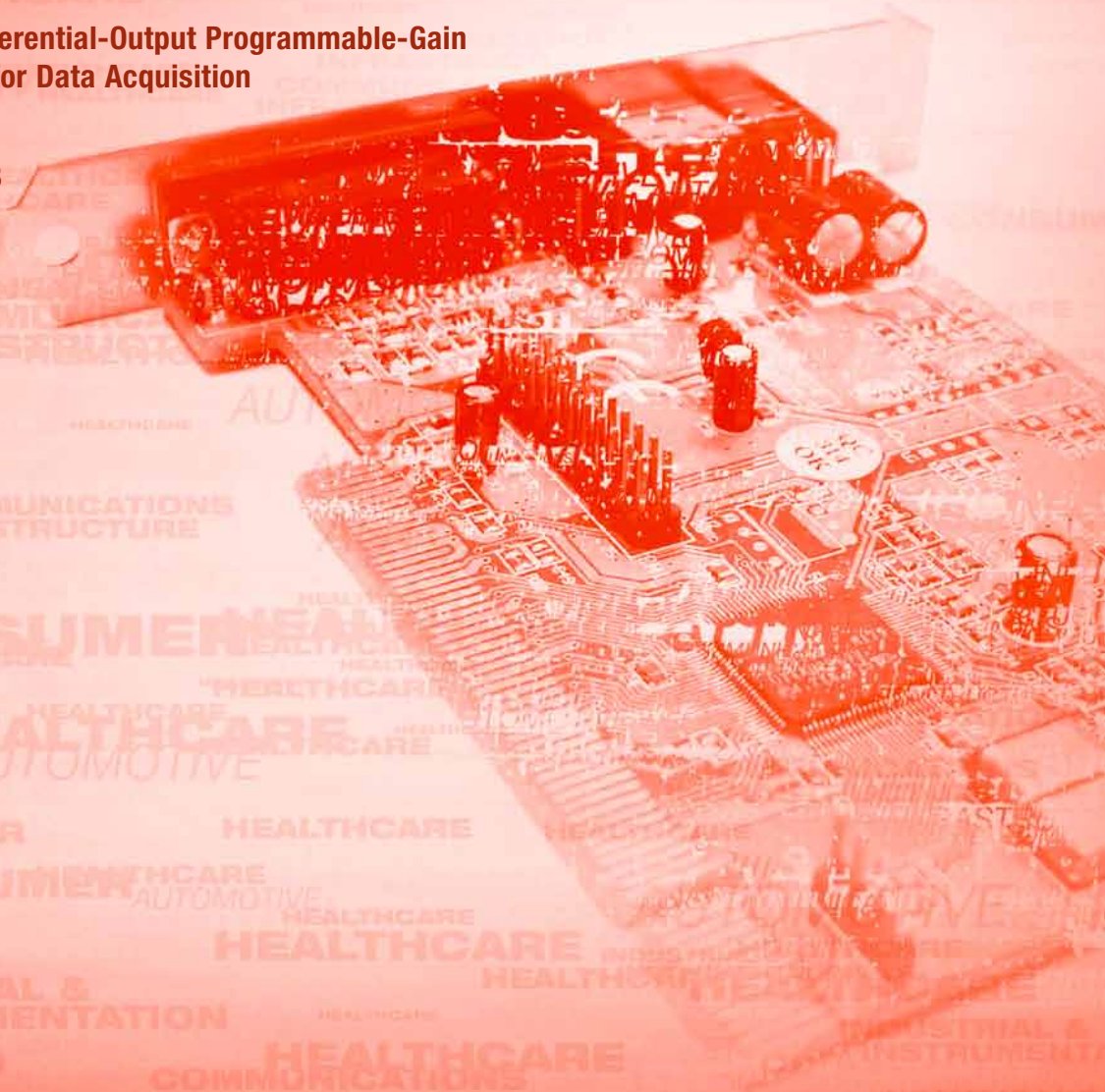
Analog Dialogue

In This Issue



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ANALOG DEVICES

Editors' Notes

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Various software packages enable PC sound cards to provide oscilloscope-like displays, but the low-sample-rate, high-resolution ADCs and ac-coupled front ends have limited bandwidths. For repetitive waveforms, a sampling front-end stretches the time axis, allowing the PC to be used as a high-speed sampling scope. This article describes a front end and probe that provide an appropriate adaptation. Page 3.

Monitoring and Sequencing in Multirail Power-Supply Systems
Today's electronic systems are likely to have many different power supply rails. For reliable, repeatable operation, the on-off timing, rise/fall rates, order of application, and magnitude of each voltage must be controlled. Typical system designs may include supply sequencing, tracking, and voltage/current monitoring/control. A variety of integrated power management ICs exists to perform these functions. Page 7.

S-Parameters Allow High-Frequency Verification of RF Switch Models
S- (scattering) parameters characterize electrical networks using matched impedances. Scattering refers to the way traveling currents or voltages are affected when they meet a discontinuity in a transmission line. *S-parameters* allow a device to be treated as a "black box" with inputs and outputs, enabling a system to be modeled without having to deal with the complex details of its actual structure. Page 11.

How to Apply DC-to-DC Step-Up/Step-Down Regulators Successfully
High efficiency dc-to-dc converters come in three basic topologies: step-down (buck), step-up (boost), and step-down/step-up (buck/boost). The buck converter generates a lower dc output voltage, the boost converter generates a higher dc output voltage, and the buck/boost converter generates an output voltage less than, greater than, or equal to the input voltage. Page 15.

Ultrahigh-Performance Differential-Output Programmable-Gain Instrumentation Amplifier for Data Acquisition
Data-acquisition systems and PLCs require versatile high-performance analog front ends that interface with a variety of sensors to measure signals accurately and reliably. Depending on the magnitude of the voltage or current being measured, the signal may need to be amplified or attenuated to match the full-scale input range of the ADC used for further digital processing and feedback control. Page 17.

Oversampled ADC and PGA Combine to Provide 127-dB Dynamic Range
The need to measure wide dynamic range signals is common, but current technology often has difficulty meeting system requirements. This article presents an alternative that uses a high-speed, successive-approximation ADC, combined with an autoranging programmable-gain amplifier front end with gain that changes automatically based on analog input value to provide a dynamic range of more than 126 dB. Page 19.

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Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 45, NUMBER 4

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

October
ADC, 12-bit, 250-MSPS/210-MSPS/170-MSPS **AD9634**
ADC, 14-bit, 250-MSPS/210-MSPS/170-MSPS **AD9642**
ADC, dual, 10-bit, 125-MSPS/105-MSPS **AD9608**
ADC, dual, 12-bit, 125-MSPS/105-MSPS **AD9628**
ADC, dual, 14-bit, 125-MSPS/105-MSPS **AD9648**
Processor, Blackfin®, 12-bit ADC, executable flash **ADSP-BF506F**
PMU, two 800-mA bucks, one 300-mA LDO **ADP5023**
PMU, two 800-mA bucks, two 300-mA LDOs **ADP5037**
PMU, two 1200-mA bucks, one 300-mA LDO **ADP5024**
Receiver, IF **AD6672**
Synthesizer, PLL, HV, fractional-N/integer-N **ADF4150HV**

November
Amplifier, differential, 6-GHz, ultrahigh DR **ADL5565**
Amplifier, operational, dual, low-power **ADA4084-2**
Controller, synchronous buck, dual, 600-kHz **ADP1876**
Controllers, digital power factor correction **ADP1047/ADP1048**
Converter, logarithmic, high-speed, 200-dB **ADL5304**
DAC, 16-channel, 24-bit, 192-kHz **ADAU1966**
Driver, white LED, four-string **ADD5205**
Generator, clock, multioutput **AD9577**
Gyroscope, yaw rate, vibration rejecting, ±250°/sec **ADXRS646**
Microphone, MEMS, ultralow-noise, analog output **ADMP504**
Modulator, quadrature, 400-MHz to 1250-MHz **ADRF6701**
Modulator, quadrature, 2050-MHz to 3000-MHz **ADRF6704**
Receiver, IF, quad **AD6657A**
Sensor, temperature, digital, 16-bit, automotive **ADT7311**
Switch, high-side load, logic-level control **ADP198**
Translators, clock, multiservice line card **AD9557/AD9558**
VGA, high-speed, digital-control, wide DR **ADL5202**

December
ADC, octal, 12-bit, 40-MSPS/80-MSPS, LVDS **AD9637**
ADC, octal, 14-bit, 40-MSPS/65-MSPS, LVDS **AD9257**
ADC, quad, 12-bit, 80-MSPS/105-MSPS/125-MSPS, LVDS **AD9633**
ADC, quad, 14-bit, 80-MSPS/105-MSPS/125-MSPS, LVDS **AD9253**
Amplifier, difference, input short-circuit protection **ADA4830-1**
Amplifier, differential, precision, low-power, G = 1 ..... **AD8476**
Amplifier, instrumentation, 1.5-nV/√Hz, G = 2000 ..... **AD8428**
Amplifier, operational, low-noise, low-power **ADA4897-2**
Amplifier, operational, precision, zero-drift **ADA4638-1**
Battery Manager, fast charge, USB-compatible **ADP5065**
Controller, hot-swap, –48-V, digital power monitor **ADM1075**
Drivers, ADC, ultralow-power, low-distortion **ADA4940-1/ADA4940-2**
Energy Meter, polyphase, harmonic monitoring **ADE7880**
Microphone, MEMS, omnidirectional, digital output **ADMP441**
Potentiometer, digital, 64-position, push-button **AD5116**
Potentiometers, digital, 128-/64-/32-position, I²C **AD5110/AD5112/AD5114**
Potentiometers, digital, 128-/64-/32-position, up/down **AD5111/AD5113/AD5115**
Regulators, low-dropout, low-noise, 300-mA/500-mA ... **ADP7102/ADP7104**
References, voltage, high-accuracy, micropower **ADR35xxW**
Sensor, angular rate, precision, ±450°/sec **ADIS16136**
Sensor, inertial, 10-DOF, tactical-grade **ADIS16488**
Switch, high-side load, logic-level control **ADP199**
Synthesizer, PLL, fractional-N/integer-N **ADF4151**
Synthesizer, PLL, 6-GHz, low-noise, fast-settling **ADF4196**
Transceiver, CAN, 24-V bus protection **ADM3051**
Transceiver, CAN, 24-V bus protection, 5-kV isolation **ADM3054**
VGA, high-speed, digital-control, wide DR **ADL5201**

Analog Dialogue

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Front End Turns PC Sound Card into High-Speed Sampling Oscilloscope

By Doug Mercer

Various software packages enable the stereo sound card found in a personal computer (PC) to provide oscilloscope-like displays, but the low-sample-rate, high-resolution analog-to-digital converters (ADCs) and ac-coupled front end are optimized for 20 kHz or less of usable bandwidth. This limited bandwidth can be extended—for repetitive waveforms—by using a sampling front end ahead of the sound card inputs. Subsampling the input waveform with a high-speed sample-and-hold amplifier (SHA)—followed by a low-pass filter to reconstruct and smooth the waveform—effectively stretches the time axis, allowing the PC to be used as a high-speed sampling oscilloscope. This article describes a front end and probe that provide an appropriate adaptation.

Figure 1 shows a schematic for a plug-in attachment that can be used for sampling with typical PC sound cards. It uses one AD783 high-speed sample-and-hold amplifier per oscilloscope channel. The sampling signal for the SHA is provided by the digital output of a clock-divider circuit; an example of one will be described. The AD783 input is buffered by a FET, so simple ac/dc input coupling can be used. In the two channels shown, 1-MΩ resistors (R1 and R3) provide dc bias when the dc-coupling jumper is open and the input is ac-coupled. The sampled output is low-pass filtered by the two-pole active RC networks shown. The filter need not be an active circuit, but the one shown usefully provides a buffered low impedance to drive the PC sound-card input.

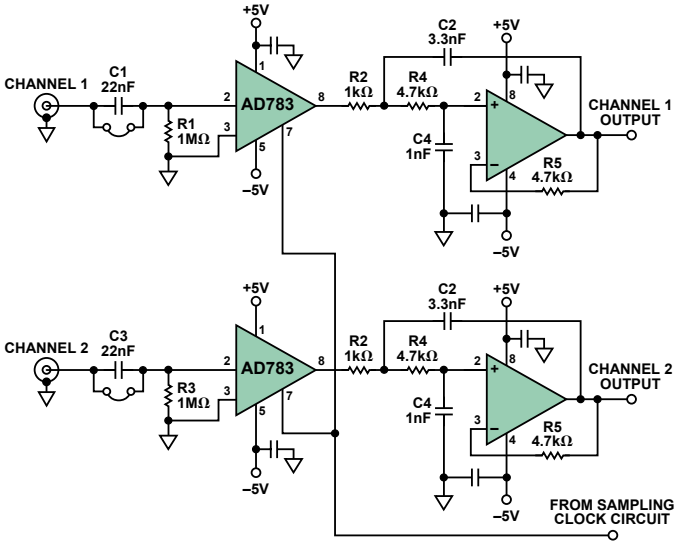


Figure 1. 2-channel analog sampling circuit.

The AD783 SHA provides a usable large-signal bandwidth up to a few megahertz. The effective slew rate at the input is above 100 V/µs. Input/output swing with a ±5-V supply is at least ±3 V. The small-signal 3-dB bandwidth for swings less than 500 mV p-p is close to 50 MHz.

With the front-end circuit of Figure 1, and a PC's sound card employing the Visual Analyser[1] software, the screen shot in Figure 2 illustrates a 2-MHz, single-cycle sine repeated at 1 MHz. The sampling clock provides 250-ns-wide sample pulses at an 80.321-kHz sample rate. The effective horizontal time base here is 333 ns/division. The PC sound card used in these examples uses an Analog Devices SoundMax® codec sampling at 96 kSPS. In this example, the effective sampling rate is about 40 MSPS.

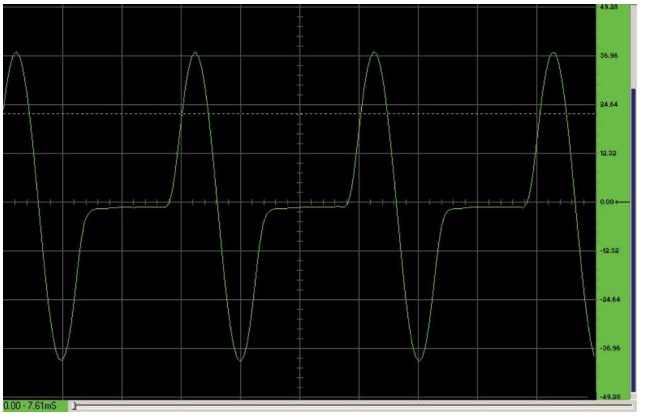


Figure 2. 2-MHz single-cycle sine pulse at 1-MHz repetition rate.

Another screen shot was taken of a Gaussian sine pulse with a 1-MHz repetition rate (Figure 3). The sampling clock rate was again 80.321 kHz, with 250-ns sample pulse width.

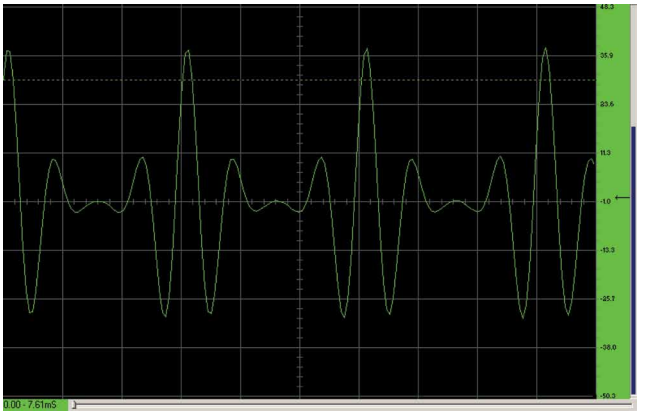


Figure 3. 4-MHz Gaussian sine pulse at 1-MHz repetition rate.

Example of a Sampling Clock Generator

The AD783 requires a narrow positive sampling pulse with a width between 150 ns and 250 ns. The sampling pulse must be very stable with low jitter in order for the displayed waveform to be stable without jumping back and forth. This requirement tends to limit possible clock choices to crystal-based oscillators. Another requirement is that the sampling rate be adjustable or tunable over a range from slightly less than 100 kHz to about 500 kHz. The tuning steps between sampling frequencies need to be relatively fine for downsampled signals to fall somewhere within the 20 Hz to 20 kHz audio bandwidth of the sound card. A divide-by-*N* circuit, such as that shown in Figure 4, and a crystal oscillator with a frequency between 10 MHz and 20 MHz (IC4), can provide up to 200 or more different sample rates from 80 kHz to 350 kHz, with step sizes from 300 Hz to 5 kHz. In this example, using two 74HC191 4-bit binary up/down counters, *N* can be any integer between 4 and 256. Alternatively, decade counters, such as the 74HC190, with identical pinouts to the 74HC191, could be used to provide a range of N from 4 to 100. The division ratio is set using the two hex switches, S1 and S2. Switch S3 sets the counters to count up or count down. Resistor R1 (250 Ω) and Capacitor C1 (68 pF) add a slight delay to the terminal count output before it asynchronously loads the start-count values. The four NAND gates of the 74HC00 are used to implement a one shot that makes a 200 ns sample pulse when R12 is 2.7 kΩ and C2 is 68 pF.

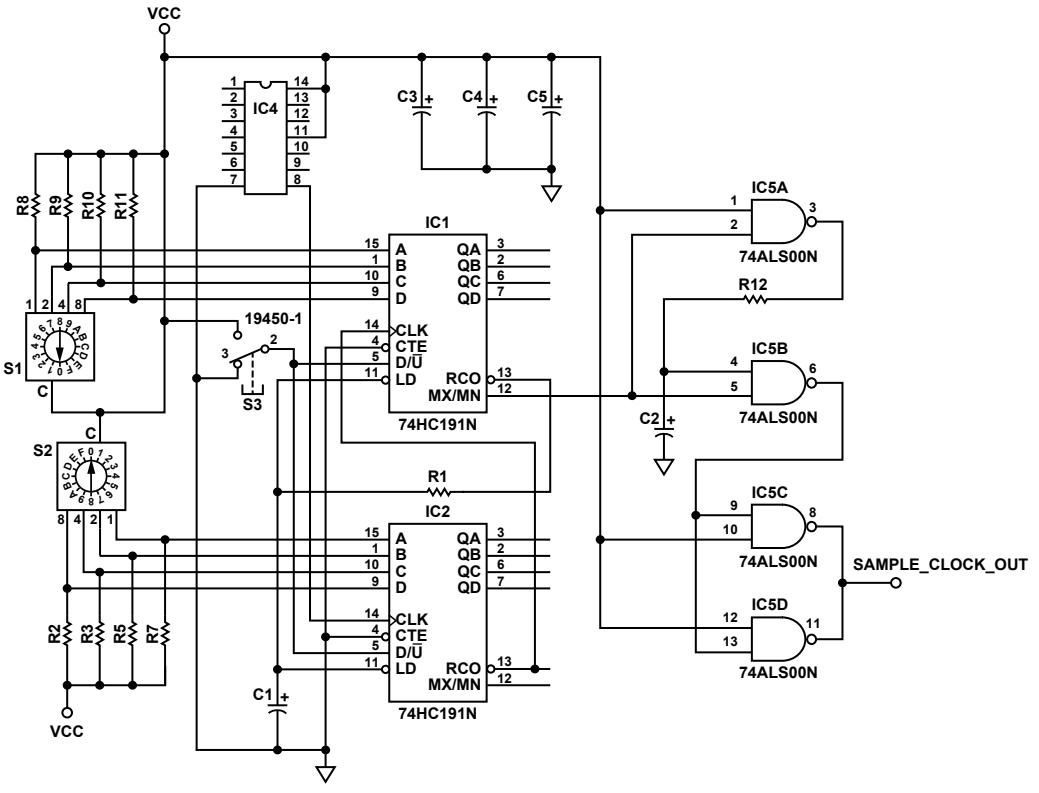


Figure 4. Sampling clock divider circuit.

IC4 is a fixed-frequency metal-can crystal oscillator. Another approach would be to use CMOS inverters (74HC04) and a discrete crystal, X1, to form an oscillator, as shown in Figure 5. This approach, while using more components than the all-in-one metal-can oscillator, permits a small amount of frequency tuning by adjusting Capacitor C1 to pull the crystal frequency.

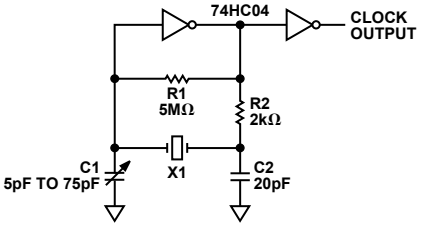


Figure 5. Discrete crystal oscillator with mechanical tuning.

To avoid the mechanically variable component, use a varactor diode—which has voltage-dependent capacitance—for D1, as shown in Figure 6.

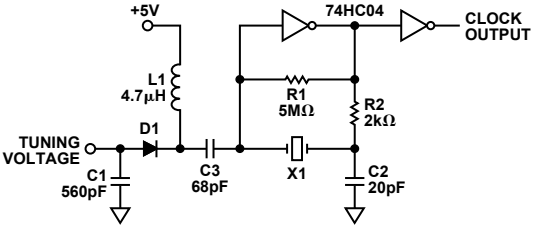


Figure 6. Discrete crystal oscillator with voltage tuning.

Examples of Active Reconstruction Filters

Figure 7 and Figure 8 show active filter designs that should work well in place of a simple passive RC filter. Figure 7 shows a second-order Sallen-Key filter, with a corner frequency of about 39 kHz, using standard resistance and capacitance values. The AD8042 and AD822 dual op amps, specified for low supply voltage and wide swing, are good choices. The filter has a gain of +1 in the pass band.

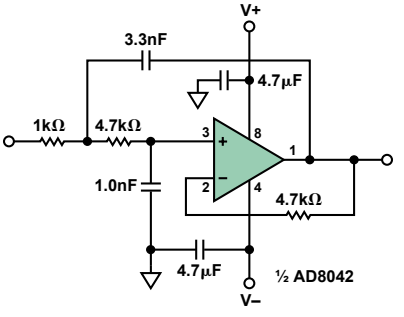


Figure 7. Sallen-Key 39-kHz low-pass filter.

Figure 8 shows another second-order multiple-feedback (MFB) filter with a corner frequency of about 33 kHz, using standard resistance and capacitance values. This filter has a pass-band gain of –1, so—if it is used—select the *invert* button on the scope software in order for the displayed waveform to be right-side up.

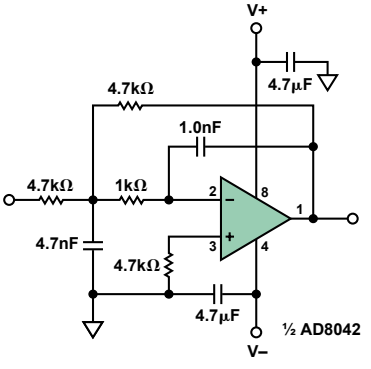


Figure 8. MFB 33-kHz low-pass filter.

Powering the Circuits

The AD783 and the amplifier used in the reconstruction filter require dual power supplies. These could be provided simply by six AA batteries, with three providing +4.5 V and the other three providing –4.5 V. Or, a single 9-V battery could be used, with a resistance divider providing a midsupply voltage as the ground—which would need to be buffered by an op amp to supply any ground currents required by the circuit; alternatively, an adjustable linear regulator could be used to produce a voltage of approximately 4.5 V with respect to the negative battery terminal for use as the ground reference.

Yet another option would be to use the +5 V provided by a spare PC or laptop USB port. The –5 V could be generated by a dc-to-dc voltage inverter, such as the Analog Devices ADM8829—in a surface-mount package—or the ICL7660 in a DIP from Intersil. Special care will be required to avoid interference from switching noise generated by the dc-to-dc voltage inverter.

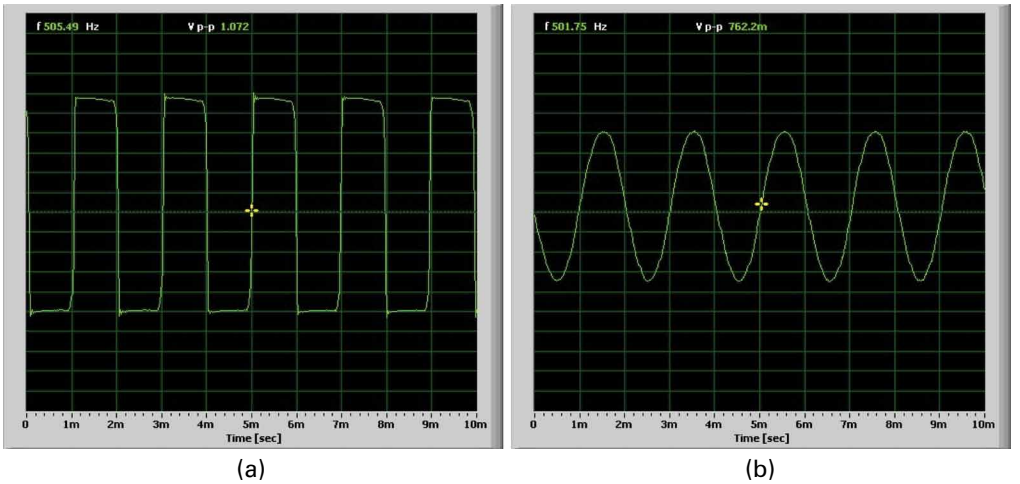
Input Attenuators

The small-signal gain of the AD783 is much higher than its full swing bandwidth. By inserting a 10:1 resistive attenuator ahead of the sampler to limit the maximum signal swing, usable bandwidth well beyond 20 MHz is possible. Relatively low cost scope probes are available from companies such as Syscomp Electronic Design, Ltd.[2] (Figure 9). At this writing:

- Oscilloscope probes (P6040) with 40-MHz bandwidth, 1×/10×switchable, cost $29.99 per pair from Syscomp Electronic Design.

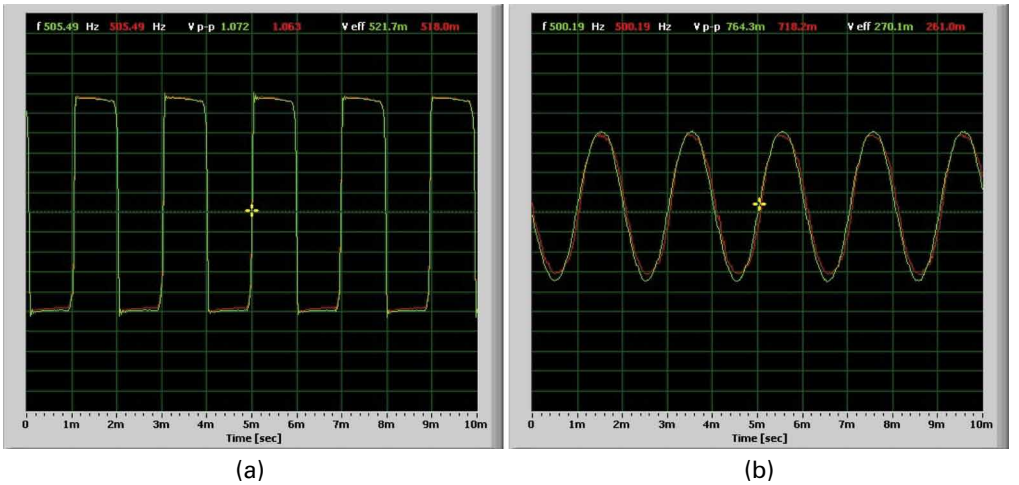
Figure 9. P6040 1×/10× scope probes.

- HobbyLab[3] sells the 20-MHz 10:1 version oscilloscope probes (GT-P6020) for $19.50 per pair.
- Gabotronics.com[4] sells both 100-MHz P2100 and 60-MHz P2060 generic probes for about $10.00 each.



(a) (b)

Figure 10. Single-channel, 10× probes, 1-MHz (a) and 50-MHz (b) 5-V p-p input square waves.



(a) (b)

Figure 11. Dual-trace 2-channel matching, 10× probes, 1-MHz (a) and 50-MHz (b) 5-V p-p input square waves.

Using the Probes

The P2100 100-MHz 10× probes, used to take the Soundcard[5] screen shots in Figure 10, Figure 11, and Figure 12, can compensate for input capacitance in the range from 10 pF to 35 pF. This seems to be a sufficient adjustment range for the proposed circuit if the PC board wire lengths are kept as short as possible. With the 10× probe, the input looks like 10 MΩ and 18 pF and can support input voltages up to ±30 V.

To demonstrate the AD783 sample-and-hold input stage, the probe compensation was first adjusted using a 1-kHz flat-top square wave. The screen shots show the response for various signals with frequencies of 1 MHz and 50 MHz. The two screen shots in Figure 10 show one channel with a 1-MHz, 5-V p-p square wave (a), and a 50-MHz, 5-V p-p square wave (b). In each case, the sample clock was adjusted for a downsampled signal frequency of about 500 Hz, so that any sound-card response differences were eliminated. Thus, the effective time scale is 500 ns/division for the screen shot on the left and 10 ns/division for the screen shot on the right. The sound card input gain was set for the scope software to report a 1.072-V p-p amplitude for the 1-MHz input and a 762.2-mV p-p amplitude for the 50-MHz input. The ratio of 0.7622/1.072 is close to –3 dB. This measurement shows that the combination of the 100-MHz 10× probe and the AD783 has a 50-MHz, 3-dB bandwidth.

In Figure 11, the same 1-MHz (a) and 50-MHz signals (b) are applied to both channels. From these two overlaid screen shots of both channels, one can see that there is good gain-, offset-, and delay-matching between the two channels.

The final screen shot (Figure 12) is of a 375-kHz, 5-V p-p square wave (red trace) and a 1.5-MHz 42 ns wide 5-V p-p pulse (green trace). The horizontal scale is 333 ns/division. The AD783 sampler maintains the full 5-V swing, even for these narrow 42-ns wide pulses.

References

[1]Visual Analyser is a complete professional real-time software package that transforms a PC into a complete set of measurement instruments. No new hardware is necessary as it uses the PC's sound card. http://www.sillanumsoft.org/.

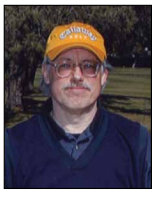
[2]Syscomp Electronic Design, Ltd. http://www.syscompdesign.com/Accessories.html.

[3]HobbyLab http://securedwithssl.com/HobbyLab-us/product/63258ffa-dcc8-4508-8152-d2461d943169.aspx.

[4]Gabotronics http://www.gabotronics.com/accesories-and-cables/view-all-products.htm.

[5]The PC-based Soundcard oscilloscope receives its data from the sound card with 44.1-kHz sampling rate and 16-bit resolution. Also available is WaveIO, a Soundcard Interface for LabView software. http://www.zeitnitz.de/Christian/scope_en.

Author



Doug Mercer [doug.mercer@analog.com] was a full-time Analog Devices employee from 1977 to 2009, the last 14 years as an ADI Fellow. The AD783 is one of the more than 30 standard products he contributed to the ADI high speed converter product lineup. Since 2009 he has transitioned to the role of Consulting Fellow at ADI working part time, most recently in the area of undergraduate EE education outreach and development, principally as ADI's point of contact with Rensselaer Polytechnic Institute.

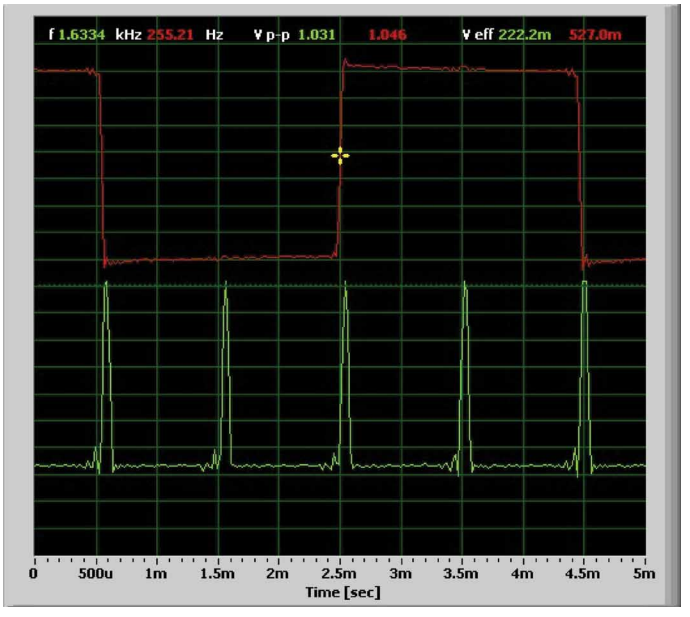


Figure 12. Dual-trace 2-channel, 10× probes, 375-kHz, 5-V p-p square wave and 1.5-MHz, 42-ns 5-V p-p pulse.

Monitoring and Sequencing in Multirail Power-Supply Systems

By Rich Ghiorse

Introduction

Today's electronic systems are likely to have many different power supply rails. This is especially true in systems employing analog circuitry along with microprocessors, DSPs, ASICs, and FPGAs. For reliable, repeatable operation, the on-off timing, rise and fall rate, order of application, and magnitude of each of the supply voltages needs to be controlled. A given power system design may include supply sequencing, supply tracking, and supply voltage/current monitoring and control. A variety of power management ICs exists to perform the functions of sequencing, tracking, and monitoring for both power-up and power-down.

Sequencing and tracking devices can monitor and control multiple rails; their functions may include setting turn-on time and voltage ramp-up rate, undervoltage and overvoltage fault detection, *margining* (supply adjustment within a range around a nominal voltage value), and orderly shutdown. ICs for these applications may range from simple purely analog devices, with resistors, capacitors, and comparators, to highly integrated state machines and programmable devices digitally controlled via an I^2C bus. In some cases, the system's voltage regulators and controllers may include key control functions.

Another consideration for systems employing multiple switching controllers and regulators is how to minimize the system noise generated as they operate at various switching frequencies. It is often desirable to synchronize the regulators' clocks. In fact, many of today's high-performance switching controllers and regulators can be synchronized to an external clock.

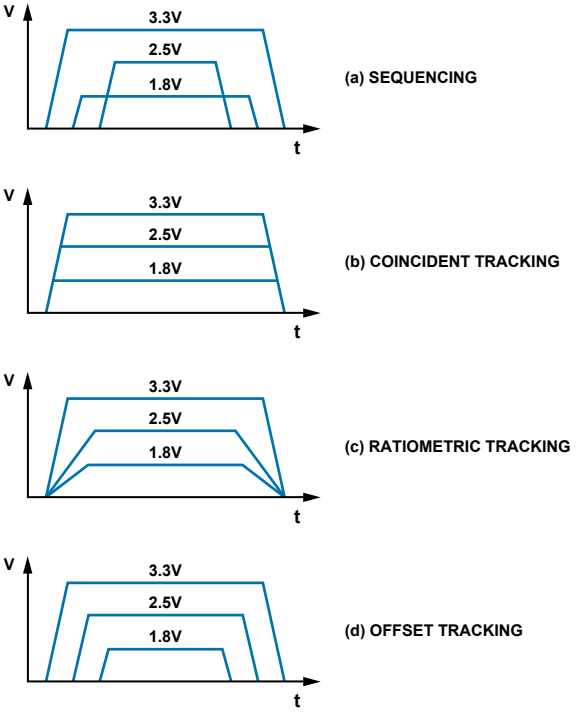


Figure 1. Types of power rail control.

Power Supply Sequencing and Tracking

Power supply *sequencing* entails turning supplies on or off in a specific order. Control of the supply sequence can be simply based on an established time order, or the turn-on time of a supply may depend on another supply reaching a programmed threshold. Power supply *tracking* is based on the fact that power supplies cannot (and generally should not) provide instantaneous changes in their voltage; this can be used advantageously by power system designers in controlling the *slew rate* of each of the various supplies in relation to other supplies in the system. Supply tracking falls into three categories: *coincident*, *ratiometric*, and *offset*. Figure 1 shows four graphs comparing sequencing, coincident tracking, ratiometric tracking, and offset tracking.

In Figure 1a, the sequence of turning the three supplies on and off is timed. Here the 3.3-V supply comes up first, and the delay-times for subsequent supplies to turn on and off depend on the needs of the application. This simple sequencing technique can ensure that the maximum ratings of active components are not exceeded if those ratings require that supplies be activated in a specific order. An example of this would be the need to guarantee that an ADC's power supply is present before the amplifier that drives it is powered up—where failure to make this provision could result in damage to the ADC's front end.

In Figure 1b, *coincident* tracking, all three supplies are turned on at the same time and brought up tracking one another at the same rate, so that the lowest supply voltages are established before higher ones are applied. Power-down is done in the reverse manner. This is a good example of how supplies might be brought up in older FPGA or microprocessor applications, where lower core voltages should be active before auxiliary or I/O supplies are brought up. An example of coincident tracking for a Xilinx Virtex-5 FPGA is shown later in this article.

In Figure 1c, the supplies are brought up at different slew rates. As noted earlier, the ability to control the slew rate, dV/dt, of supplies is very useful to prevent damage from large, decoupling-capacitor inrush currents (charging currents) in the circuit. Inrush currents can greatly exceed normal operating currents if not contained. Slew-rate limiting can prevent latch-up of active devices, shorting of capacitors, potential damage to PCB tracks, and blowing of in-line fuses.

In Figure 1d, the supplies all have the same slew rate, but their times of application are determined by predetermined offset voltages. This type of tracking is appropriate for devices that require the difference between the supply voltages to be limited; often appearing in the maximum rating sections of mixed-signal components such as DACs and ADCs. This approach can prevent permanent damage to the parts.

FPGA-Based Design Example

The powering of a system that uses an FPGA provides an excellent object lesson on the subject of handling multiple supply systems. Proper control of FPGA supplies can make the difference between a reliable, repeatable design, and a possibly catastrophic failure in the lab or, worse, in the field. Most FPGAs have multiple rails, commonly labeled V_{CCO}, V_{CCAUX}, and V_{CCINT}. These supplies are respectively used to power the FPGA core, *auxiliary circuits* (such as clocks and PLLs), and *interface logic*.

The considerations for these power supply rails can be categorized as:

- Sequencing of the rails
- Tolerance requirements for the rail voltages
- The possible need for soft start, or slew-rate control, of the supplies.

As an illustrative example, consider the power supply requirements for the Xilinx Virtex-5 family of FPGAs, a family that offers a wide range of features—including logic programmability, signal processing, and clock management. According to the data sheet, the Virtex-5 requires a power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. The ramp times for these supplies relative to ground are 200 µs min to 50 ms max. The recommended operating conditions are shown in Table 1.

The Virtex-5, as noted earlier, requires coincident voltage tracking. In addition, the supplies must fall within specific recommended operating tolerances—and also must ramp up and down within specified ranges of *dV*/*dt*.

But the FPGA is only part of a larger system. To elaborate on this example, assume that there is a high-current, 5-V, main system rail. The 1-V supply that powers the FPGA core has a tolerance of ±5% (±50 mV) and is required to deliver currents up to 4 A. The 3-V supply is a general logic supply with a ±5% tolerance and, in this example, is required to supply 4 A to power the FPGA I/O and other logic devices in the design. The 2.5-V supply is an analog supply that must deliver 100 mA with low noise.

A good solution for this application employs the ADP1850 dual buck controller for the 1-V and 3-V high-current supplies. Among the ADP1850's features are soft-start control, coincident tracking, and the ability to sequence a slave supply from a master supply. Power-on ramp-up rates are controlled by capacitors on the SS1 and SS2 pins. In this example, the 3-V digital supply is the master supply. For the 2.5-V analog supply, an ADP150 ultralow noise low-dropout regulator (LDO) is an excellent choice; it can be sequenced from the ADP1850's PGOOD2 signal. A simplified diagram of the system, showing the general flow of sequencing, appears in Figure 2 (for full details, see the ADP1850 data sheet).

The above example illustrates a common use of sequencing and tracking; it can be extended to many of today's multiple-supply systems, including microprocessor-based systems and those that involve mixed-signal technologies—with ADCs and DACs.

Analog Voltage and Current Monitoring (ADM1191)

For high-reliability applications that require precise *monitoring* of multiple system power-supply currents and voltages, easy-to-deploy analog monitoring circuits are available. For example, the ADM1191 digital power monitor, with 1% measurement accuracy, includes a 12-bit ADC for current and voltage readback, a precision current-sense amplifier, and an ALERTB output that provides an overcurrent interrupt. Figure 3 shows the ADM1191 in an application with a host controller, such as a microprocessor or microcontroller.

Table 1. Xilinx Virtex-5 Power Rail Requirements

	Voltage Range	Voltage Min/Max	Current	Start-Up Time (Min)	Start-Up Time (Max)	
V_{CCINT}	1 V ± 5%	−0.5 V to +1.1 V	4 A	200 µs	50 ms	On before V_{CCAUX}/V_{CCO}
V_{CCAUX}	2.5 V ± 5%	−0.5 V to +3.0 V	~50 mA	200 µs	50 ms	On before V_{CCO}
V_{CCO}	3 V ± 5%	−0.5 V to +3.75 V	<50 mA	200 µs	50 ms	

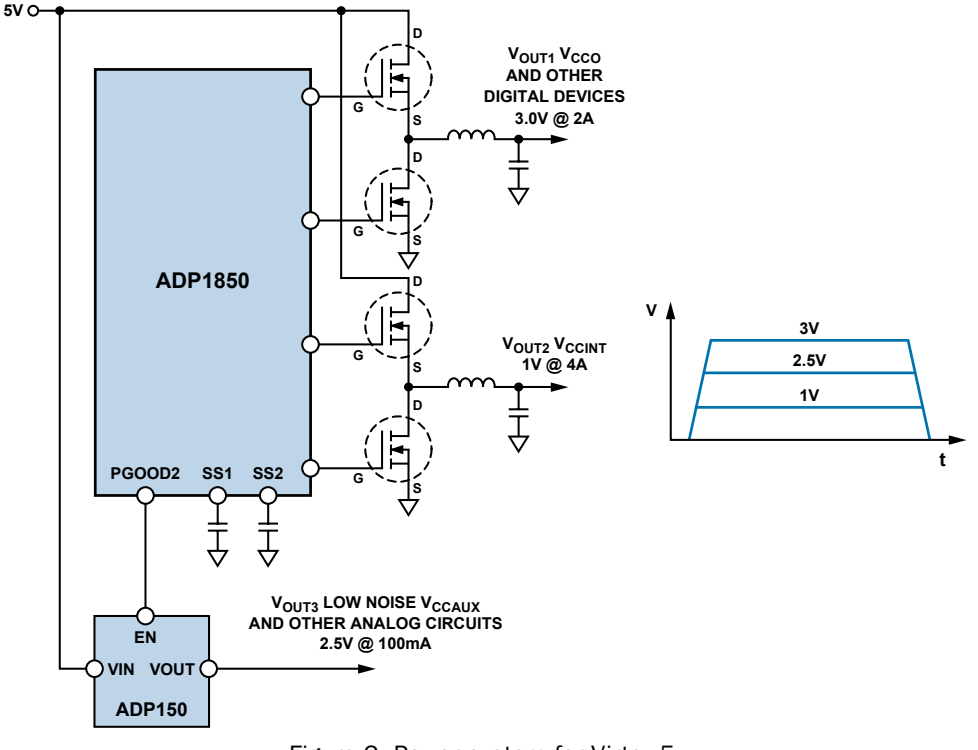


Figure 2. Power system for Virtex-5.

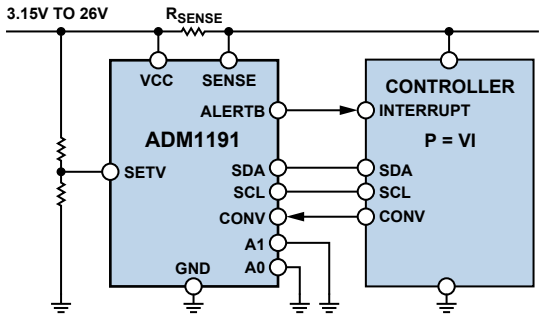


Figure 3. A simple power-supply voltage and current monitor.

The ADM1191 communicates over the I²C bus to the host controller. A total of 16 devices can be addressed in the same system by configuring the logic input levels of their A0 and A1 pins. The local controller can compute the power consumption on the rail by multiplying together the measured voltage and current. The ALERTB signal gives quick notification of an overcurrent condition via an interrupt to the controller—a rapid warning of a fault condition to help protect the system from damage.

Combining Sequencing and Monitoring

Large fixed systems, and even some high-performance plug-in cards, have many power rails that need to be controlled and monitored. Figure 4 deals with a complex power system that has eight supply rails. The heart of the system is an ADM1066, a flexible highly integrated Super Sequencer® that provides complete power control. Features include sequencing, monitoring, margining, and programmability. Other devices in the ADM106x family add temperature monitoring and a watchdog function.

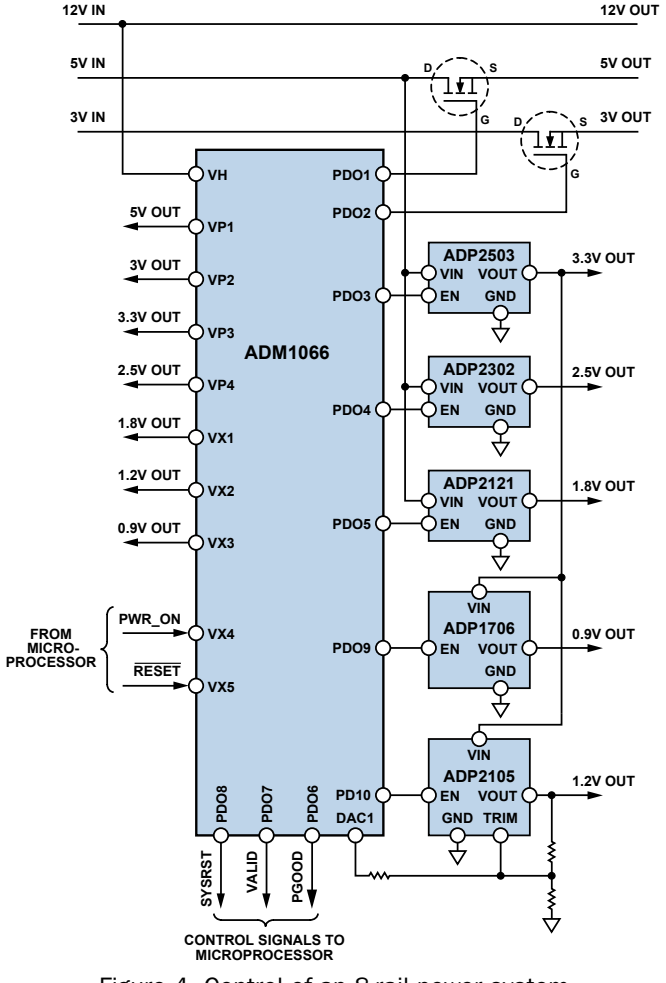


Figure 4. Control of an 8-rail power system.

The 8-rail system has three main power rails: 12 V, 5 V, and 3 V. The other rails are derived from these using switching regulators and LDOs. Each of the regulators has an enable input that is driven by one of the 10 *programmable driver* (PD) outputs of the ADM1066, thus allowing the user to bring all the power rails up in a controlled sequence. The ADM1066 has an on-board charge pump to step up six of the PD output voltages to provide a high-voltage drive for external N-MOSFETS that act as power-rail switches in cases where it is necessary to control higher-voltage supplies.

The ADM1066 has on-board EEPROM to store power system control parameters. Device configuration is facilitated with a utility program available from Analog Devices, Inc. This makes the task of getting up and running much easier, eliminating time-consuming code development. As a system evolves and new parts are added to the design, adjustments to supply sequences are easily handled. Timing parameters and voltage trip points are easily reprogrammed. This valuable feature saves development time and reduces the risk of possible board spins.

The digital output signals—PWRGD (power good), VALID, and SYSRST (system restore)—are generated by the ADM1066 to inform the system microcontroller of the status of the power system, either when polled or via interrupts or digital inputs, so that action can be taken if fault conditions exist. Such quick notification can prevent catastrophic damage from shorted capacitors and other dangerous conditions. PWR_ON and $\overline{\text{RESET}}$ are digital inputs to the ADM1066 from the system controller, completing the overall system control loop.

Supply Margining with the ADM1066

The on-chip DACs of the ADM1066 are useful for performing supply margining during system development, when it is necessary for the designer to adjust supply voltages, either to optimize their levels or move them away from nominal values. This margining feature allows a system to be fully characterized over supply limits without the use of external instrumentation. The function is typically performed during an in-circuit test (ICT), for example, when a manufacturer wants to guarantee that a product under test functions correctly at nominal supply voltages within limits of ±5%. Starting with the circuit in Figure 4, the user can implement margining on many of the supply rails.

Open-Loop Supply Margining

The simplest method of margining a supply, such as a dc-to-dc converter or an LDO, is to switch extra resistors into the feedback node of the power module to alter the voltage at the feedback or trim node, forcing the output voltage to margin up or down by the desired amount using a DAC. With such an attenuator in place (Figure 5), the ADM1066 can be remotely commanded to margin a supply, using the SMBus, by updating the values on the relevant DAC output. The process can be implemented using an open-loop technique, independently of the system control loop.

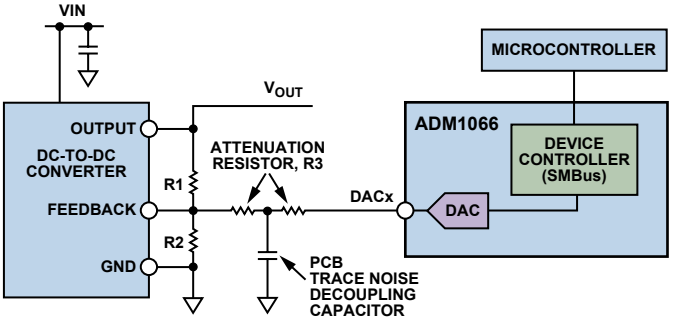


Figure 5. Open-loop margining.

The ADM1066 can perform open-loop margining for up to six supplies, using the six on-board voltage-output DACs (DAC1 to DAC6) to drive into the feedback pins of the power modules being margined. The simplest circuit to implement this function is an attenuation resistor (R3) that connects the DACx pin to the feedback node of a dc-to-dc converter. When the DACx output voltage is set equal to the feedback voltage, no current flows into the attenuation resistor, and the dc-to-dc converter output voltage does not change. Taking DACx above the feedback voltage forces current into the feedback node, and the output of the dc-to-dc converter must fall to compensate for this. To raise the dc-to-dc converter output, the DACx output voltage is set lower than the feedback node voltage. For noise reduction, as shown here, the series resistor can be split into two resistors, and the node between them can be decoupled with a capacitor to ground at the dc-to-dc converter.

Closed-Loop Supply Margining

A more accurate and comprehensive method of margining uses a similar circuit in a closed-loop system. An example is shown in Figure 4 for the 1.2-V output. The voltage on the rail to be margined can be read back via VX2 to accurately margin the rail to the target voltage. The ADM1066 incorporates all the circuits required to do this, with the 12-bit successive-approximation ADC reading the level of the supervised voltages, and the six voltage-output DACs adjusting supply levels as described above. These circuits can be used along with other intelligence, such as a microcontroller, to implement a closed-loop margining system that allows any dc-to-dc converter or LDO supply to be set to any voltage, accurate to within ±0.5% of the target.

To implement closed-loop margining on the rail to be tested, use the following steps:

1. Disable the six DACx outputs.
2. Set the DACx output voltage equal to the voltage on the feedback node.
3. Enable the DAC.
4. Read the voltage at the dc-to-dc converter output that is connected to one of the VPx, VH, or VXx pins.
5. If necessary, modify the DACx output voltage up or down to adjust the dc-to-dc converter output voltage. Otherwise stop; the target voltage has been reached.
6. Set the DAC output voltage to a value that alters the supply output by the required amount (for example, ±5%).
7. Repeat the process until the required voltage for that rail is reached.

Steps 1 to 3 ensure that when each DACx output buffer is turned on, it has little immediate effect on the dc-to-dc converter output. The DAC output buffer is designed to power up without transient "glitches" by first powering up the buffer to follow the pin voltage. It does not drive the pin at this time. Once the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer is turned on, all but eliminating output glitching.

Synchronization of Switching Regulators

In systems with multiple rails that use more than one switching regulator or controller, the possibility exists for these devices to interact due to differences in their internal switching frequencies. This can cause beat harmonics that can greatly increase supply noise and wreak havoc with EMI testing. Fortunately, many switching controllers and regulators are designed to allow their internal clocks to be synchronized. LDOs do not share this problem, but it is not always desirable to use them due to their limited current output and, in most cases, poor efficiency.

The ADP2116 dual switching regulator is a good example of a synchronizable device. Its SYNC/CLKOUT pin can be configured as an input SYNC pin or an output CLKOUT pin via the SCFG pin. As an input SYNC pin, it synchronizes the ADP2116 to an external clock; the two channels switch at half the external clock frequency and are 180° out of phase with one another.

As a CLKOUT pin, it provides an output clock that is twice the switching frequency of the channels and 90° out of phase. Thus a single ADP2116 configured for the CLKOUT option can act as the master converter and provide an external clock for all other dc-to-dc converters—including other ADP2116 devices (Figure 6). Configured as slaves, they accept the master's external clock and synchronize to it. By synchronizing all dc-to-dc converters in the system, this approach prevents beat harmonics that can lead to EMI issues.

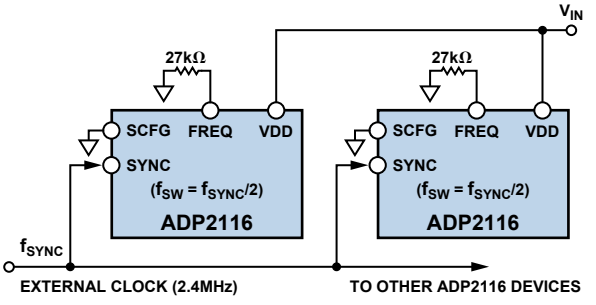


Figure 6. Synchronizing ADP2116s from an external clock.

Conclusion

This article discusses ways of handling multiple power supply systems. The high level of functional integration provided by sequencers, monitors, regulators, and controllers enables designers to address potential power problems without employing a board full of discrete ICs—a capability that provides designers with good value and increases the odds of successful designs with minimal redesigns and board spins.

References

Moloney, Alan. "Power Supply Management—Principles, Problems, and Parts." *Analog Dialogue*. 40-2. May 2006.

Author

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S-Parameters Allow High-Frequency Verification of RF Switch Models

By Joseph Creech

Introduction to S-Parameters

S (scattering) parameters are used to characterize electrical networks using matched impedances. Here, scattering refers to the way traveling currents or voltages are affected when they meet a discontinuity in a transmission line. *S-parameters* allow a device to be treated as a "black box" with inputs and resulting outputs, making it possible to model a system without having to deal with the complex details of its actual structure.

As the bandwidth of today's integrated circuits increases, it is important to characterize their performance over wide frequency ranges. Traditional low-frequency parameters—such as resistance, capacitance, and gain—can be frequency dependent, and thus may not fully describe the performance of the IC at the desired frequency. In addition, it may not be possible to characterize every parameter of a complex IC over frequency, so system-level characterization using S-parameters may provide better data.

A simple RF relay can be used to demonstrate the techniques of high-frequency model verification. As shown in Figure 1, an RF relay can be thought of as a three-port device, with an input, an output, and a control to switch the circuit on and off. If the device performance is independent of the control terminal, once set, the relay can be simplified to a two-port device. As such, the device can be completely characterized by observing the behavior at its input and output terminals.

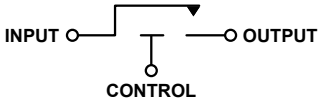


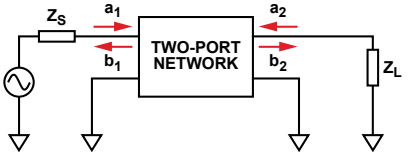
Figure 1. RF relay model.

In order to understand the concept of S-parameters, it is important to know some transmission line theory. Similar to the familiar dc relationship, the maximum power transfer at high frequencies is related to the impedance of the power source and the impedance of the load. Voltages, currents, and power from a source, of impedance Z_S, travel in waves to the load, of impedance Z_L, along a transmission line of impedance Z_0. If $Z_L = Z_0$, total power is transferred from the source to the load. If $Z_L \neq Z_0$, some power is reflected from the load back to the source, and maximum power transfer does not occur. The relationship between the incident and reflected wave is known as the reflection coefficient, Γ, a complex number that contains both magnitude and phase information about the signal.

If the match between Z_0 and Z_L is perfect, no reflections occur, and $\Gamma = 0$. If Z_L is open- or short-circuited, $\Gamma = 1$, indicating perfect mismatch, with all power reflected back to Z_S. In most passive systems, Z_L is not exactly equal to Z_0, so $0 < \Gamma < 1$. For Γ to be greater than unity, the system must contain a gain element—which will not be considered in the case of the RF relay. Reflection coefficients can be expressed as a function of the impedances under consideration, so Γ can be calculated as:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (1) \qquad \rightarrow \qquad \Gamma = \frac{\frac{Z_L}{Z_0} - 1}{\frac{Z_L}{Z_0} + 1} \quad (2)$$

Assume that the transmission line is a two-port network, as shown in Figure 2. In this representation, it can be seen that every traveling wave is made up of two components. The total traveling wave component flowing from the output of the two-port device to the load, b_2, is actually made up of the portion of a_2 that is reflected from the output of the two-port device plus the portion of a_1 that is transmitted through the device. Conversely, the total traveling wave flowing from the input of the device back toward the source, b_1, is made up of the portion of a_1 that is reflected from the input plus that fraction of a_2 that is transmitted back through the device.



a1 = TRAVELING WAVE INCIDENT ON PORT 1
b1 = TRAVELING WAVE REFLECTED FROM PORT 1
a2 = TRAVELING WAVE INCIDENT ON PORT 2 (REFLECTED FROM THE LOAD)
b2 = TRAVELING WAVE REFLECTED FROM PORT 2

Figure 2. S-parameter model.

Using the above interpretations, equations can be written to determine the values of the reflected waves, employing S-parameters. Equation 3 and Equation 4 show the reflection and transmission wave equations.

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (3)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (4)$$

If $Z_S = Z_0$ (impedance of two-port input), no reflections occur, and $a_1 = 0$. If $Z_L = Z_0$ (impedance of two-port output), no reflections occur and $a_2 = 0$. Therefore, we can define the S-parameters, based on the matched condition, as:

$$S_{11} = \frac{b_1}{a_1} \quad (5) \qquad S_{22} = \frac{b_2}{a_2} \quad (6)$$

$$S_{21} = \frac{b_2}{a_1} \quad (7) \qquad S_{12} = \frac{b_1}{a_2} \quad (8)$$

where:

S_{11} = the input reflection coefficient.

S_{12} = the reverse transmission coefficient.

S_{21} = the forward transmission coefficient.

S_{22} = the reverse reflection coefficient.

Any two-port system can be fully described by these equations, with forward- and reverse gain characterized by S_{21} and S_{12}, and forward- and reverse-reflected power characterized by S_{11} and S_{22}.

To realize the above parameters in a physical system, Z_S, Z_0, and Z_L must be matched. For most systems this is easily implemented over a wide frequency range.

Designing and Measuring Transmission Line Impedance

To ensure that a two-port system has matched impedances, it is necessary to measure Z_S, Z_0, and Z_L. Most RF systems work in a 50-Ω environment. Z_S and Z_L are normally restricted by the type of *vector network analyzer* (VNA) used, but Z_0 can be designed to match the VNA impedance.

Transmission Line Design

The impedance of a transmission line is set by the ratio of inductance and capacitance on the line. A simple model for a transmission line is shown in Figure 3.

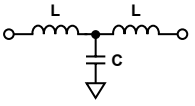


Figure 3. Lumped-element model of a transmission line.

Equations for calculating the complex impedance at a desired frequency determine the values of L and C required to obtain a particular impedance. The manner of adjusting L and C depends on the type of transmission line model, with the most common models being *microstrip* and *co-planar waveguide*. Using physical parameters, such as distance from trace to ground plane, trace width, and the dielectric constant of the PCB substrate, the inductance and capacitance can be balanced to provide the desired impedance. The easiest way to design transmission line impedance is to use one of the many available impedance design programs.

Measuring Impedance

Once the transmission line has been designed and produced, the impedance must be measured to verify that the design and execution were correct. One method for measuring impedance is to use *time-domain reflectometry* (TDR). TDR measurements provide a representation of the signal integrity of a PCB trace. TDR sends a fast pulse down the signal line and records the reflections, which are then used to calculate the impedance of the path at a particular distance from the source. This information can then be used to find open- or short circuits in the signal path or to analyze the impedance of a transmission line at a particular point.

TDR is based on the principle that, in an unmatched system, reflections that occur will add or subtract from the signal source at various points along the signal path (*constructive* and *destructive interference*). If a system (in this case a transmission line) is matched to 50 Ω, no reflections occur across the signal path, and the signal remains unaltered. However, if the signal encounters an open circuit, the reflections add to the signal, doubling it; if the signal encounters a short circuit, reflections null it through subtraction.

If the signal meets a terminating resistor with a value somewhat higher than the correct matching resistance, a bump will be seen in the TDR response; a slightly lower terminating resistance will cause a dip in the TDR response. Comparable responses will be seen for terminations that are capacitive or inductive, because a capacitor is a short at high frequencies and an inductor is an open circuit at high frequencies.

Among the factors that influence the accuracy of the TDR response, one of the most important is the rise time of the TDR pulse sent down the signal path. The faster the rise time of the pulse, the smaller the features that TDR can resolve.

Based on the TDR equipment's set rise time, the minimum spatial distance that the system can detect between two discontinuities is:

$$l_{\min} = \frac{c_0 t_{rise}}{2\sqrt{\varepsilon_{eff}}} \tag{9}$$

where:

l_{min} = minimum spatial distance of the discontinuity from the source.
c_0 = speed of light in a vacuum.
t_{rise} = rise time of the system.
ε_{eff} = effective permittivity of the medium where the wave is traveling.

To examine relatively long lengths of transmission lines, rise times of the order of 20 ps to 30 ps are sufficient; however, a much faster rise time is necessary to examine the impedance of integrated-circuit devices.

TDR impedance measurements can be recorded to help resolve various issues of transmission line design, such as incorrect impedance, discontinuities due to connector junctions, and soldering-related problems.

Recording S-Parameters Accurately

Once the PCB and system have been designed and manufactured, the S-parameters must be recorded at a set power over a range of frequencies using a VNA that has been calibrated to ensure accurate recordings. The choice of calibration technique will depend on such factors as frequency range of interest and the necessary reference plane for the *device under test* (DUT).

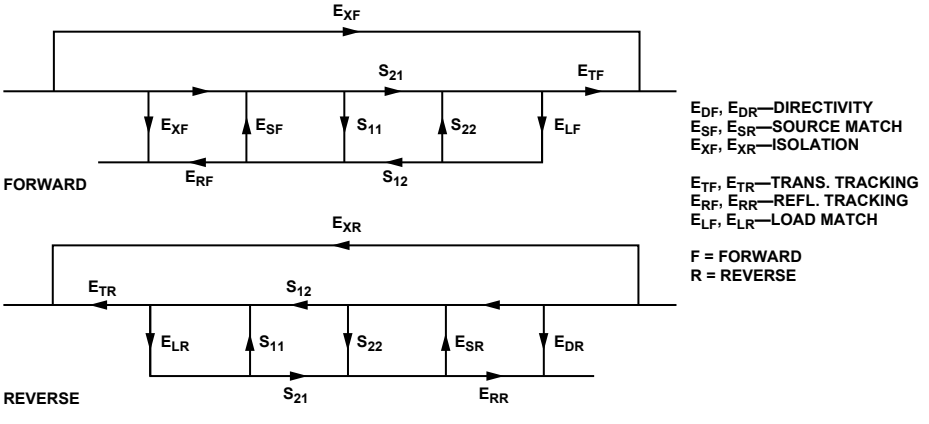


Figure 4. Full two-port, 12-term error model.

Calibration Techniques

Figure 4 shows the full 12-term error model with systematic effects and error sources for a two-port system. The measurement frequency range affects the calibration choice: the higher the frequency, the greater the calibration error. As more terms become significant, the calibration technique must change to accommodate the high-frequency effects.

One widely used VNA calibration technique is SOLT (short, open, load, thru) calibration, also known as TOSM (thru, open, short, match). Simple to implement, it only requires a set of known standards, which are measured in both the forward and reverse directions. These can be bought with the VNA or from other manufacturers. Once these standards are measured, the systematic errors can be calculated by determining the difference between the measured responses and the known responses of the standards.

SOLT calibration locates the reference plane of the VNA measurement at the ends of the coaxial cables used during the calibration procedure. A disadvantage of SOLT calibration is that any interconnect introduced between the reference planes, including, for example, SMA (subminiature version A) connectors and PCB traces, will affect the measurement; as the measurement frequency increases these will become greater sources of error. SOLT calibration removes only six of the error terms shown in Figure 4, but it can provide accurate results for low-frequency measurements and has the advantage of being easily implemented.

Another useful VNA calibration technique is TRL (thru, reflect, line) calibration. This technique is based only on the characteristic impedance of a short transmission line. Using two sets of two-port measurements that differ by this short length of transmission line and two reflection measurements, the full 12-term error model can be determined. The TRL calibration kit can be designed on the DUT's PCB, allowing the calibration technique to remove errors due to transmission line design and interconnects, and moving the reference plane of the measurement from the coaxial cable up to the DUT pin.

Both calibration techniques have their advantages, but TRL removes more error sources, so it can provide greater accuracy for high-frequency measurements. It can be more difficult to implement, however, as it requires accurate transmission line design and accurate TRL standards at the frequencies of interest. SOLT is easier to implement, as most VNAs come with SOLT standard kits that are usable over a wide frequency range.

PCB Design and Implementation

For proper calibration of the VNA, correct PCB design is essential. Techniques such as TRL can compensate for errors in the PCB design, but cannot fully negate them. When designing a PCB with TRL calibration, for example, accurate S-parameter measurements, where low values of S_{21} (such as the insertion loss of the RF relay) are necessary, requires consideration of the return loss (S_{11}, S_{22}) of the thru standard. Return loss is input power reflected back to the source because of impedance mismatch. And no matter how well designed a PCB trace is, there will always be some degree of mismatch. Most PCB manufacturers can only guarantee impedance match to ±5% of the desired impedance, and even that with difficulty. This return loss causes the VNA to indicate a greater insertion loss than is actually present, as the VNA "thinks" it has sent more power through the DUT than it has.

As the required level of insertion loss decreases, it becomes necessary to reduce the amount of return loss the thru standard contributes to the calibration. This becomes increasingly difficult as the measurement frequency increases.

Improving the return loss of the calibration standards for TRL designs involves a number of key considerations. First, the transmission line design is critical and requires close coordination with the PCB manufacturer to ensure that correct design, materials, and processes are used to achieve the required impedance vs. frequency profile. The choice of connector components that can operate satisfactorily over the range is critical. Once the components are chosen, it is also necessary to make sure that the junction between the connector and the PCB is well designed; if not, it can disrupt the desired 50 Ω impedance between the coaxial cable and the PCB transmission line, thus degrading the system return loss. Many connector manufacturers provide drawings for the correct layout of high-frequency connectors, along with a predesigned transmission line design and PCB stack-up. Finding a PCB manufacturer that can produce to this design greatly simplifies the PCB design work.

Second, consider the *assembly* of the PCB. As the junction between the connector and the PCB transmission line is critical, soldering of the connection has a large effect on the transition. Poorly connected or misaligned connectors disrupt the delicate balance of inductance and capacitance that defines the impedance of the junctions. Figure 5 shows an example of a poorly soldered connector junction.

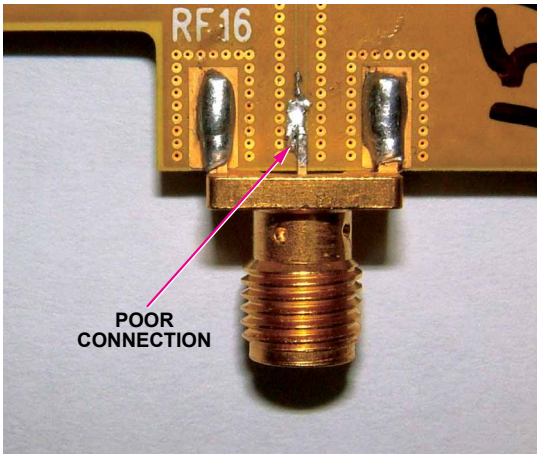


Figure 5. Poorly connected SMA.

A solder mask coating can also have an undesired effect on the impedance of the transmission line if its dielectric constant is not taken into account by the design program. While not a major consideration in lower frequency PCBs, as frequency increases, the solder mask can become troublesome.

To ensure that the return loss of the thru trace is acceptable, it is necessary to measure it using a VNA. As the reference plane of the system goes from connector to connector, a SOLT calibration should be sufficient to measure the thru trace. Once the return loss performance of the thru has been established, deficiencies can be monitored by performing a TDR on the trace. The TDR will show the areas where the system deviates most from the desired impedance.

On the TDR plot, it should be possible to mark out the specific components of the system that contribute to most of the deviation. Figure 6 shows a transmission line trace and its corresponding TDR plot. It is possible to locate the impedance of certain components on the TDR plot to see which ones contribute most of the return loss. From this plot, it can be seen that the junction between the SMA and the transmission line deviates from 50 Ω, and that the impedance of the transmission line itself is not satisfactorily close to 50 Ω. To improve the performance of this PCB, it will be necessary to work to implement some of these considerations.

Using S-Parameters

S-parameters can provide many benefits in characterizing a DUT over a frequency range. As well as showing gain, loss, or impedance match at a certain frequency, physical parameters such as capacitance can also be calculated by replacing S-parameters with other forms such as Y-parameters (admittance parameters). Y-parameters differ only in that they are derived (Equations 5–8) in terms of a short circuit (0 Ω) at the terminal of interest instead of a matched 50-Ω termination as for S-parameters. Y-parameters can be physically measured, but they are harder to record than S-parameters, as creating a true short over a wide frequency range is difficult. Since it is easier to make a broadband 50-Ω match, it is better to record S-parameters and convert them to Y-parameters. Most modern RF software packages can do this.

Calculating Physical Parameters

For an example of using S-parameters to calculate capacitance over a desired frequency range, consider the RF relay example shown in Figure 1. To calculate the capacitance of the relay to ground when the relay is open (that is, *off*), it is first necessary to change the S-parameter recordings to Y-parameters, which transforms the data from a 50-Ω environment to being terminated in a short circuit. From the physical structure of the relay, it is evident that when the output port is terminated to ground and the switch is off, the capacitance to ground can be seen by examining the Y_{11} parameter, a measure of the amount of power sent back to the source. When the switch is open, all the power is expected to be reflected. However, some of the power will get through to the output port, which is connected to ground (by definition of the Y-parameter). The power is transferred through the capacitance to ground. Therefore, dividing the imaginary part of the Y_{11} parameter by $2\pi f$ will give the capacitance of the RF relay to ground at the desired frequency.

To calculate the inductance of the RF relay, a similar method is used, but Z- (impedance) parameters are used in place of Y-parameters. Z-parameters are similar to S- and Y-parameters, but instead of a resistive match or a short, an open circuit is used to define the termination. With a little thought this approach can be taken to all devices to calculate various physical parameters.

Matching Networks

Another use of S-parameters is in the design of matching networks. Many applications require impedance matching to ensure the best possible power transfer at a certain frequency. Using S-parameters, the input- and output impedance of a device can be measured. The S-parameters can then be displayed on a Smith chart and the appropriate matching network can be designed.

Providing Customers with Models

As discussed earlier, because of their universal nature, S-parameter files are useful to provide input-output information for linear circuits to customers, as parts can be fully described over large frequency ranges without the need to disclose complex (or possibly proprietary) designs. Customers can use the S-parameters in similar ways as described previously to model the part in their system.

Conclusion

S-parameters are useful tools for creating and verifying high-frequency models over a large bandwidth. Once recorded they can be used to calculate many other circuit characteristics and to create matching networks. However, a number of necessary precautions must be taken into account when designing the measurement system. Of paramount importance is the choice of calibration method and the PCB design. By following the measures outlined here, some of the potential pitfalls can be avoided.

References

Rako, Paul. "TDR: taking the pulse of signal integrity." *EDN*. September 3, 2007.

Bowick, Chris, John Blyler, and Cheryl Ajluni. *RF Circuit Design*. Newnes. 2007.

Author

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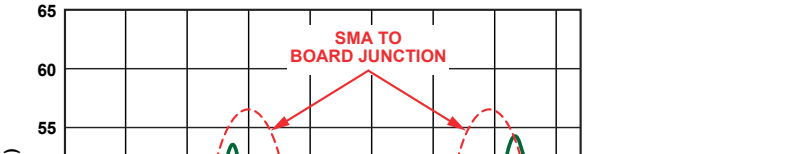

Figure 6. PCB to TDR plot.

How to Apply DC-to-DC Step-Up/Step-Down Regulators Successfully

By Ken Marasco

DC-to-dc *switching converters* are used to change one dc voltage to another efficiently. High efficiency dc-to-dc converters come in three basic topologies: *step-down* (buck), *step-up* (boost), and *step-down/step-up* (buck/boost). The *buck* converter is used to generate a lower dc output voltage, the *boost* converter is used to generate a higher dc output voltage, and the *buck/boost* converter is used to generate an output voltage less than, greater than, or equal to the input voltage. This article focuses on how to successfully apply buck/boost dc-to-dc converters. Buck and boost converters have been covered individually in the June 2011 and September 2011 issues of *Analog Dialogue* and will not be reviewed in this article.

Figure 1 shows a typical low-power system powered from a single-cell *lithium-ion* (Li-Ion) battery. The battery's usable output varies from about 3.0 V when discharged to 4.2 V when fully charged. The system ICs require 1.8 V, 3.3 V, and 3.6 V for optimum operation. While the lithium-ion battery starts at 4.2 V and ends at 3.0 V, a buck/boost regulator can supply a constant 3.3 V, and a buck regulator or *low-dropout regulator* (LDO) could supply the 1.8 V, as the battery discharges. Conceivably a buck regulator or LDO could be used for the 3.3 V while the battery voltage is above 3.5 V, but the system would cease to operate when the battery voltage dropped below 3.5 V. Allowing the system to be turned off prematurely reduces the system's operating time before the battery needs to be recharged.

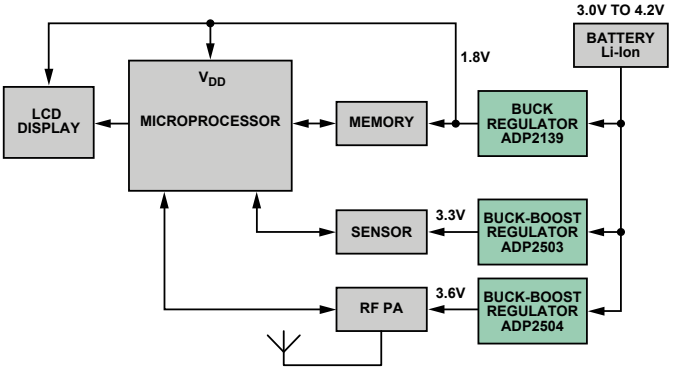

Figure 1. Typical low-power portable system.

Buck/boost regulators contain four switches, two capacitors, and an inductor, as shown in Figure 2. Today's low-power, high-efficiency buck/boost regulators reduce losses and improve efficiency by actively operating only two of the four switches when operating in buck- or boost mode.

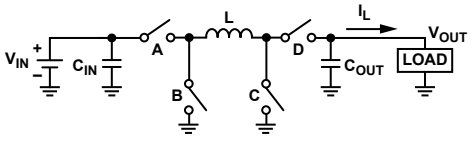

Figure 2. Buck/boost converter topology.

When V_{IN} is greater than V_{OUT}, Switch C is open and Switch D is closed. Switches A and B operate as in a standard buck regulator—as shown in Figure 3.

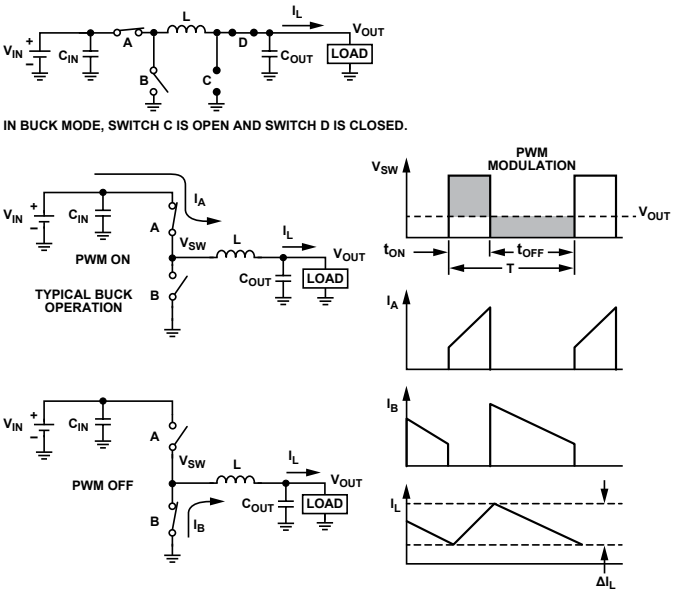

Figure 3. *Buck* mode when $V_{IN} > V_{OUT}$.

When V_{IN} is less than V_{OUT}, Switch B is open and Switch A is closed. Switches C and D operate as in a boost regulator—as shown in Figure 4. The most difficult operating mode is when V_{IN} is in the range of $V_{OUT} \pm 10\%$, and the regulator enters the *buck-boost* mode. In buck-boost mode, the two operations (buck and boost) take place during a switching cycle. Care must be taken to reduce losses, optimize efficiency, and eliminate instability due to mode switching. The objective is to maintain voltage regulation with minimal current ripple in the inductor to guarantee good transient performance.

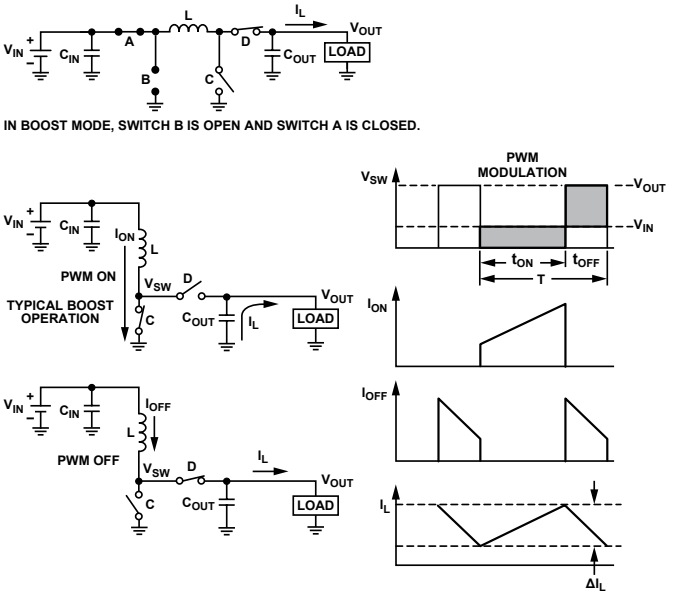

Figure 4. *Boost* mode when $V_{IN} < V_{OUT}$.

At high load currents, the buck-boost uses voltage or current-mode, fixed-frequency *pulse-width-modulation* (PWM) control for optimal stability and transient response. To ensure the longest battery life in portable applications, a *power-save* mode reduces the switching frequency under light load conditions. For wireless and other low-noise applications, where variable-frequency power-save mode may cause interference, the addition of a logic control input to force fixed-frequency PWM operation under all load conditions is included.

Buck/Boost Regulators Improve System Efficiency

A large number of the portable systems in use today are powered by a single-cell rechargeable Li-Ion battery. As mentioned above, the battery will start from a fully charged 4.2 V and slowly discharge down to 3.0 V. When the battery's output drops below 3.0 V, the system is turned off to protect the battery from damage due to extreme discharging. When a low-dropout regulator is used to generate a 3.3-V rail, the system will shut down at

$$V_{IN\,MIN} = V_{OUT} + V_{DROPOUT} = 3.3\text{ V} + 0.2\text{ V} = 3.5\text{ V}$$

employing only 70% of the battery's stored energy. However, using a buck/boost regulator, such as the ADP2503 or ADP2504, enables the system to continue operating down to minimum practical battery voltage. The ADP2503 and ADP2504 (see Appendix) are high-efficiency, low-quiescent-current 600-mA and 1000-mA, step-up/step-down (buck/boost) dc-to-dc converters that operate with input voltages greater than, less than, or equal to the regulated output voltage. The power switches are internal, minimizing the number of external components and printed-circuit-board (PCB) area. This approach allows the system to operate all the way down to 3.0 V, using most of the battery's stored energy, increasing the system's operating time before a battery recharge is required.

To save energy in portable systems, various subsystems—such as the microprocessor, display backlighting, and power amplifiers—when not in use, are frequently switched between full *on* and *sleep* mode, which can induce large voltage transients on the battery supply line. These transients can cause the battery's output voltage to briefly drop below 3.0 V and trigger the *battery low* warning, causing the system to turn off before the battery is completely discharged. The buck/boost solution will tolerate voltage swings as low as 2.3 V, helping to maintain the system's potential operating time.

Buck/Boost Regulator Key Specifications and Definitions

Output voltage range options: Buck/boost regulators are available with specified fixed output voltages or in an option that allows the output voltage to be programmed via an external resistance divider.

Ground or *quiescent* current: DC bias current not available for the load (I_q). The lower the I_q, the better the efficiency, but I_q can be specified under many conditions, including switched *off*, zero load, pulse-frequency mode (PFM), or pulse-width mode (PWM) operation, so it is best to look at operating efficiency at specific operating voltages and load currents when determining the best boost regulator for the application.

Shutdown current: The input current consumed when the enable pin has been set to *off*. Low I_q is important for long standby times when a battery-powered device is in *sleep* mode. During logic-controlled shutdown, the input is disconnected from the output and draws less than 1 μA from the input source.

Soft start: It is important to have a *soft-start* function that ramps the output voltage in a controlled manner to prevent excessive output voltage overshoot at startup.

Switching frequency: Low-power buck/boost converters generally operate between 500 kHz and 3 MHz. Higher switching frequencies allow the use of smaller inductors and reduce the required PCB area, but efficiency is decreased by approximately 2% for every doubling of the switching frequency.

Thermal shutdown (TSD): If the junction temperature rises above the specified limit, the thermal shutdown circuit turns the regulator off. Consistently high junction temperatures can be the result of high-current operation, poor circuit-board cooling, and/or high ambient temperature. The protection circuit includes hysteresis so that, after thermal shutdown, the device will not return to normal operation until the on-chip temperature drops below the preset limit.

Conclusion

Low-power buck-boost regulators with proven performance and in-depth support take the worry out of designs using switching dc-to-dc converters. In addition to a comprehensive data sheet, with design calculations available in its applications section, the ADIsimPower design tool simplifies the task for the end user. Regulator selection guides, data sheets, and application notes can be found at http://www.analog.com/en/power-management/products/index.html.

For help, visit the Engineering Zone at http://ez.analog.com/index.jspa; or phone or email an applications engineer at Analog Devices.

References

Marasco, K. "How to Apply DC-to-DC Step-Up (Boost) Regulators Successfully." *Analog Dialogue*. Volume 45. September 2011.

Marasco, K. "How to Apply DC-to-DC Step-Down (Buck) Regulators Successfully." *Analog Dialogue*. Volume 45. June 2011.

Marasco, K. "How to Apply Low-Dropout Regulators Successfully." *Analog Dialogue*. Volume 43. August 2009.

http://www.analog.com/en/power-management/products/index.html.

http://www.analog.com/en/power-management/switching-regulators-integrated-fet-switches/products/index.html.

http://www.analog.com/en/power-management/switching-controllers-external-switches/products/index.html.

http://designtools.analog.com/dtPowerWeb/dtPowerMain.aspx.

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APPENDIX

Buck-Boost DC-to-DC Switching Converters Operate at 2.5 MHz

The ADP2503 and ADP2504 are high-efficiency, low-quiescent-current step-up/step-down dc-to-dc converters that can operate at input voltages greater than, less than, or equal to the regulated output voltage. The power switches and synchronous rectifiers are internal to minimize external part count. At high load currents, they use a current-mode, fixed-frequency pulse-width modulation (PWM) control scheme for optimal stability and transient response. To ensure the longest battery life in portable applications, the devices have an optional power-save mode that reduces the switching frequency under light load conditions. For wireless and other low-noise applications where variable frequency power-save mode may cause interference, the logic control input sync forces fixed-frequency PWM operation under all load conditions.

The ADP2503 and ADP2504 can run from input voltages between 2.3 V and 5.5 V, allowing a single lithium or lithium polymer cell, multiple alkaline or NiMH cells, PCMCIA, USB, and other standard power sources. Various fixed-output options are available, or using the adjustable model, the output voltage can be programmed through an external resistor divider. Compensation is internal to minimize the number of external components.

Ultrahigh-Performance Differential-Output Programmable-Gain Instrumentation Amplifier for Data Acquisition

By Reem Malik and Sandro Herrera

Data-acquisition systems and programmable-logic controllers (PLCs) require versatile high-performance analog front ends that interface with a variety of sensors to measure signals accurately and reliably. Depending on the particular type of sensor and the magnitude of the voltage or current being measured, the signal may need to be amplified or attenuated to match the full-scale input range of the analog-to-digital converter (ADC) used for further digital processing and feedback control.

Typical voltage measurement spans in data-acquisition systems range from ±0.1 V to ±10 V. By choosing the correct voltage range, the user implicitly changes the system gain to maximize the amplitude of the sampled voltage at the input of the analog-to-digital converter (ADC), which, in turn, maximizes the signal-to-noise ratio (SNR) and measurement accuracy. In typical data-acquisition systems, signals that require attenuation and signals that require amplification are processed by different signal paths. This usually results in a more complex system design, requires extra components, and uses more board space. Solutions that offer attenuation and amplification in the same signal path generally use programmable-gain amplifiers and variable-gain amplifiers, but these amplifiers do not usually offer the high dc precision and temperature stability required by many industrial and instrumentation applications.

One way to build a powerful analog front end that provides both attenuation and amplification in a single signal path—and differential outputs to drive high-performance analog-to-digital converters—is to cascade a programmable-gain instrumentation amplifier (PGIA), such as the AD8250 (gain of 1, 2, 5, or 10), AD8251 (gain of 1, 2, 4, or 8), or AD8253 (gain of 1, 10, 100, or 1000), with a fully differential funnel (attenuating) amplifier, such as the AD8475, in a circuit similar to that shown in Figure 1. This solution offers simplicity, flexibility, and high speed—along with excellent precision and temperature stability.

The aforementioned programmable-gain instrumentation amplifiers, featuring 5.3-GΩ differential input impedance and –110-dB total-harmonic distortion (THD), are ideal for interfacing with a wide variety of sensors. At a gain of 10, guaranteed specifications for the AD8250 include: 3-MHz bandwidth, 18-nV/√Hz voltage noise, 685-ns settling time to 0.001%, 1.7-µV/°C offset drift, 10-ppm/°C gain drift, and 90-dB common-mode rejection from dc to 50 kHz. This combination of precision dc performance coupled with high speed makes the amplifiers well-suited for data-acquisition applications with multiplexed inputs.

The AD8475 high-speed, fully differential funnel amplifier with integrated precision resistors provides precision attenuation of 0.4 or 0.8, common-mode level-shifting, single-ended-to-differential conversion, and input overvoltage protection. This easy-to-use, fully integrated precision gain block is designed to process signal levels up to ±10 V using a single +5 V supply. As a result, it can match industrial-level signals with the differential input voltage range of low-voltage, high-performance, 16-bit and 18-bit successive-approximation (SAR) ADCs with sampling rates of up to 4 MSPS.

The AD825x and AD8475, working together as shown in Figure 1, provide a flexible high-performance analog front end. Table 1 shows the gain combinations that can be achieved, depending on the input and output voltage range requirements.

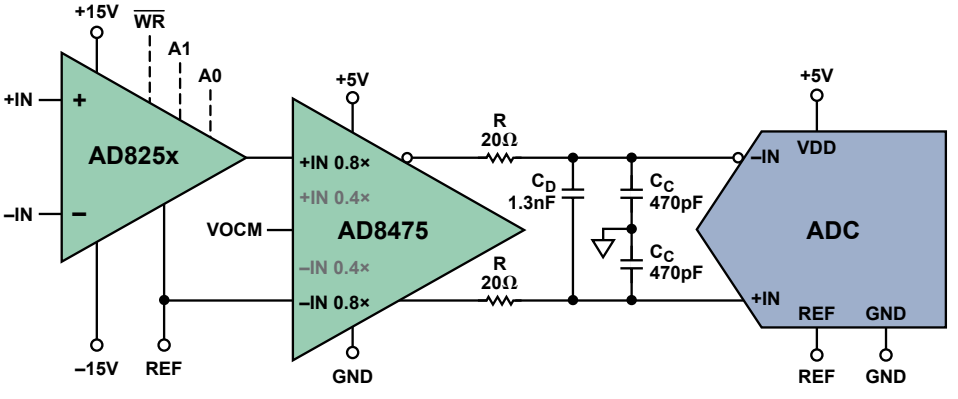

Figure 1. Data-acquisition analog front end that uses the AD825x PGIA and AD8475 differential-output funnel amplifier.

Table 1. Input Voltage Ranges and Gains Possible with the AD8475 in Combination with the AD8250, AD8251, and AD8253

DAQ Instrument Measurement Range (V)	Peak-to-Peak Voltage (V)	ADC Max Voltage per Input (V)	Overall System Gain	AD825x Gain	AD8475 Gain	Peak-to-Peak Voltage at ADC Input	AD825x Input Voltage Limit Needed (to Protect ADC)	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8250 Gain
±5	10	4.096	0.8	2	0.4	8	5.12	
±2	4	4.096	2	5	0.4	8	2.048	
±1	2	4.096	4	10	0.4	8	1.024	
±5	10	4.096	0.8	1	0.8	8	5.12	
±2.5	5	4.096	1.6	2	0.8	8	2.56	
±1	2	4.096	4	5	0.8	8	1.024	
±0.5	1	4.096	8	10	0.8	8	0.512	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8251 Gain
±5	10	4.096	0.8	2	0.4	8	5.12	
±2.5	5	4.096	1.6	4	0.4	8	2.56	
±1	2	4.096	3.2	8	0.4	6.4	1.28	
±5	10	4.096	0.8	1	0.8	8	5.12	
±2.5	5	4.096	1.6	2	0.8	8	2.56	
±1	2	4.096	3.2	4	0.8	6.4	1.28	
±0.5	1	4.096	6.4	8	0.8	6.4	0.64	
±10	20	4.096	0.4	1	0.4	8	10.24	AD8253 Gain
±1	2	4.096	4	10	0.4	8	1.024	
±0.1	0.2	4.096	40	100	0.4	8	0.1024	
±0.01	0.02	4.096	400	1000	0.4	8	0.01024	
±5	10	4.096	0.8	1	0.8	8	5.12	
±0.5	1	4.096	8	10	0.8	8	0.512	
±0.05	0.1	4.096	80	100	0.8	8	0.0512	
±0.005	0.01	4.096	800	1000	0.8	8	0.00512	

Capabilities: Input Voltage Range and Bandwidth

The maximum input voltage range for the AD825x family of PGIAs is about ±13.5 V when operating on ±15-V power supplies (the AD8250 and AD8251 provide additional overvoltage protection of up to 13 V beyond the power-supply rails). In this application, the effective limit on the PGIA input voltage range is set by the full-scale voltage range of the ADC inputs and the signal path gain from the sensor to the ADC. For example, the AD7986 18-bit, 2-MSPS PulSAR ADC operates on a single +2.5-V supply, with a typical 4.096-V reference voltage. Its differential inputs accept up to ±4.096 V (0 V to 4.096 V and 4.096 V to 0 V on the inputs). If the overall gain of the analog front end is set to 0.4, with the AD825x configured for a gain of 1 and the AD8475 configured for a gain of 0.4, the system can process an input signal with a maximum magnitude of ±10.24 V.

To determine the combination of gain settings required in any system, consider the full-scale input voltage of the ADC (VFS) and the minimum/maximum current or voltage levels expected from the sensors.

$$GAIN_{SYSTEM} = GAIN_{AD825x} \times GAIN_{AD8475}$$

$$V_{INmax} = \frac{V_{FS(ADC)}}{GAIN_{SYSTEM}}$$

The speed and bandwidth of this analog front end is exceptional given its level of precision and functionality. The speed and bandwidth capabilities of this circuit are determined by the following combination of factors:

- AD825x settling time: For a 10-V output voltage step, the AD8250 settles to 0.001% (16 bits) in 615 ns.
- AD825x slew rate: The AD825x slews at a rate between 20 V/µs and 30 V/µs depending on the gain setting. The AD8475 slews at a rate of 50 V/µs, so the system is limited by the AD825x slew rate.
- Antialiasing filter (AAF) cutoff frequency: This user-determined filter band-limits the signal presented at the ADC inputs to prevent aliasing and improve the SNR of the signal chain (see amplifier and ADC data sheets for details).
- ADC sample rate: The AD8475 can drive up to 4-MSPS converters with 18-bit resolution.

Many data-acquisition and process-control systems measure pressure, temperature, and other low-frequency input signals, so the dc precision and temperature stability of the front-end amplifiers are critical to the system performance. Many of these applications include multiple sensors that are multiplexed to the amplifier inputs in a polling fashion. Typically, the polling frequency is much greater than the bandwidth of the signal of interest. When the multiplexer switches from one sensor to the next, the voltage change seen by the amplifier inputs is unknown, so the design must accommodate the worst-case scenario: a full-scale voltage step. The amplifier must be able to settle from this full-scale step within the time allotted to switching. This settling time also needs to be lower than the settling time required by the ADC to sample and acquire the signal.

(continued on Page 23)

Oversampled ADC and PGA Combine to Provide 127-dB Dynamic Range

By Colm Slattery and Mick McCarthy

Introduction

The need to measure signals with a wide dynamic range is quite common in the electronics industry, but current technology often has difficulty meeting actual system requirements. Weigh-scale systems typically use load-cell bridge sensors with maximum full-scale outputs of 1 mV to 2 mV. Such systems may require resolutions on the order of 1,000,000 to 1, which, when referred to a 2-mV input, call for a high-performance, low-noise, high-gain amplifier and a Σ-Δ modulator. Similarly, chemical and blood analysis for medical applications often use photodiode sensors, producing very small currents that need to be accurately measured (see Figure 1). A low-noise transimpedance amplifier is typically used, with multiple stages of gain and post processing.

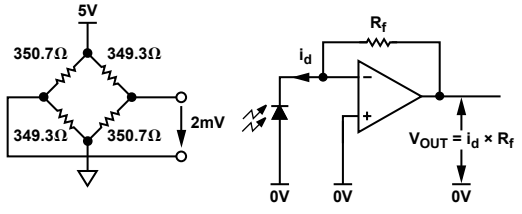

Figure 1. Inputs for load-cell and photodiode applications.

While the actual sensor data typically takes up only a small portion of the input signal range, the system must often be designed to handle fault conditions. Thus, a wide dynamic range, high performance with small inputs, and quick response to fast-changing signals, are key requirements. Some applications, such as vibration-monitoring systems, contain both ac and dc information, so the ability to accurately monitor both small and large signals is growing in importance.

These requirements call for a flexible signal-conditioning block, with low-noise inputs, relatively high gains, and the ability to dynamically change the gain in response to input level changes without affecting performance, while still maintaining a wide dynamic range. Existing Σ-Δ technology can provide the dynamic range needed for many applications, but only at the expense of update rate. This article presents an alternative approach that uses a high-speed, *successive-approximation,* sampling ADC, combined with an autoranging *programmable-gain amplifier* (PGA) front end. With gain that changes automatically based on analog input value, it uses oversampling to increase the dynamic range of the system to more than 126 dB.

Technology

In ADC applications, dynamic range is the ratio of the rms value of the full scale to the rms noise, which is generally measured with the analog inputs shorted together. Commonly expressed in decibels ($dB_V = 20 \times \log_{10}$ of the voltage ratio), it indicates the range of signal amplitudes that the ADC can resolve; an ADC with a dynamic range of 60 dB can resolve signal amplitudes with a range of 1000:1. For an *N*-bit ADC, the dynamic range (DR) can be calculated as:

$$DR = 6.021N + 1.763 \text{ dB}$$

The Σ-Δ ADCs, such as the AD7767, achieve excellent dynamic range by combining a Σ-Δ modulator with a digital postprocessor. The digital filtering that follows the converter acts to remove the out-of-band quantization noise, but it also reduces the data rate from f_{MCLK}, at the input of the filter, to $f_{MCLK}/8$, $f_{MCLK}/16$, or $f_{MCLK}/32$, at the digital output—depending on which model of the device is being used. For increased dynamic range, a low-noise PGA can be added to condition the input signal to attain full scale. The noise floor of the system will be dominated by the input noise of the front-end PGA—depending on the gain setting. If the signal is too large, it overranges the ADC input. If the signal is too small, it gets lost in the converter's quantization noise. The Σ-Δ ADCs often tend to be used for applications that require lower system update rates.

Oversampling Successive-Approximation ADC to Improve Dynamic Range

One method for increasing the dynamic range of a successive-approximation ADC is to implement *oversampling*: the process of sampling the input signal at a much higher rate than the Nyquist frequency. As a general rule, every doubling of the sampling frequency yields approximately a 3-dB improvement in noise performance (see Figure 2). Oversampling can be implemented digitally using post-processing techniques. Some ADCs, such as the AD7606, have programmable oversampling rates, enabling the end user to choose the appropriate oversampling ratio.

Combining PGA Functionality with Oversampling

To achieve maximum dynamic range, a front-end PGA stage can be added to increase the effective signal-to-noise ratio (SNR) for very small signal inputs. Consider a system dynamic range requirement of >126 dB. First, calculate the minimum rms noise to achieve this dynamic range. For example, a 3-V input range (6 V p-p) has a 2.12-V full-scale rms value ($6/2\sqrt{2}$). The maximum allowable system noise is calculated as

$$126 \text{ dB} = 20 \log (2.12 \text{ V}/\textit{rms noise})$$

Thus, the *rms noise* ≈ 1 μV rms.

Now, consider the system update rate, which will determine the oversampling ratio and the maximum amount of noise, referred to the input (RTI), that can be tolerated in the system. For example, with the AD7985 16-bit, 2.5-MSPS PulSAR® ADC running at

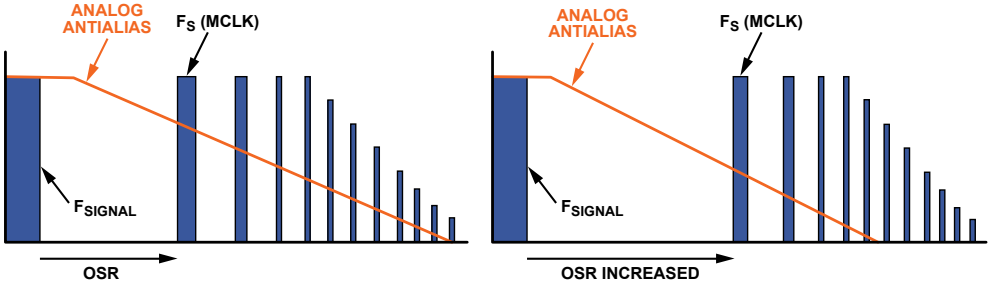

Figure 2. Oversampling reduces noise.

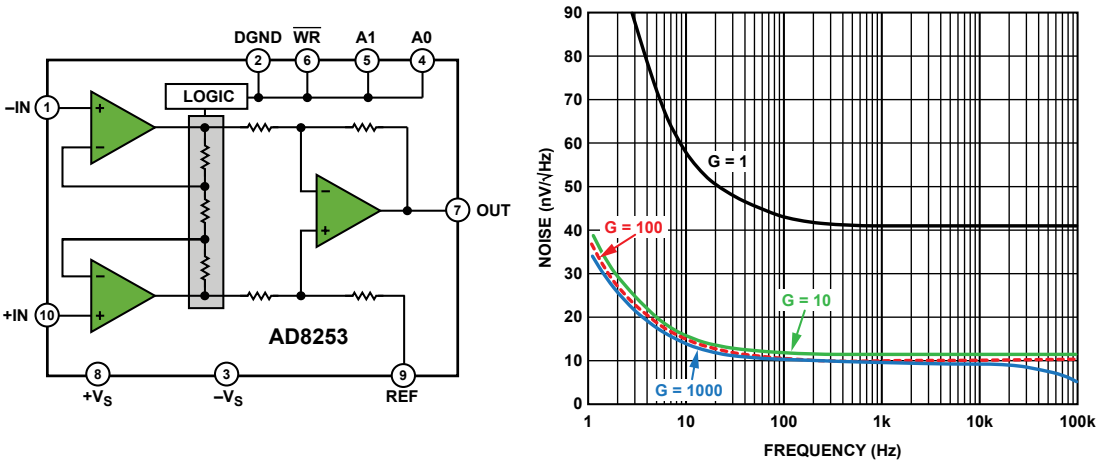

Figure 3. AD8253 instrumentation amplifier: block diagram and noise spectral density.

600 kSPS (11 mW dissipation) and an oversampling ratio of 72, the input signal is limited to a bandwidth of approximately 4 kHz. The total rms noise is simply the noise density (ND) times $\sqrt{f}$, so the maximum allowable input spectral noise density (*ND*) can be calculated as

$$1\ \mu V\ rms = ND \times \sqrt{4\ kHz}$$

Or, ND = 15.5 nV/√Hz

From this figure of merit for RTI system input noise, a suitable instrumentation amplifier can be chosen that will provide sufficient analog front-end gain (when summed with the SNR of the ADC, with associated oversampling) to achieve the required 126 dB. For the AD7985, the typical SNR figure is 89 dB, and oversampling by 72 yields another ~18-dB improvement (72 is approximately 2^6, and each doubling adds 3 dB). Achieving 126 dB DR still requires more than 20-dB improvement, which can come from the gain provided by the analog PGA stage. The instrumentation amplifier must provide a gain ≥20 (or whatever will not exceed a noise density specification of 15.5 nV/√Hz). A good candidate is the AD8253 10-MHz, 20-V/µs, G = 1, 10, 100, 1000 *i*CMOS® *programmable-gain instrumentation amplifier*; it has a low-noise, 10-nV/√Hz input stage at a gain of 100 for the required bandwidth, as shown in Figure 3.

A system-level solution to implement front-end PGA gain and ADC oversampling is shown in Figure 4. The AD8021 is a 2.1-nV/√Hz low-noise, high-speed amplifier capable of driving the AD7985. It also offsets and attenuates the AD8253 output. Both the AD8253 and AD8021 are operated with external common-mode bias voltages, which combine to maintain the same common-mode voltage on the input to the ADC.

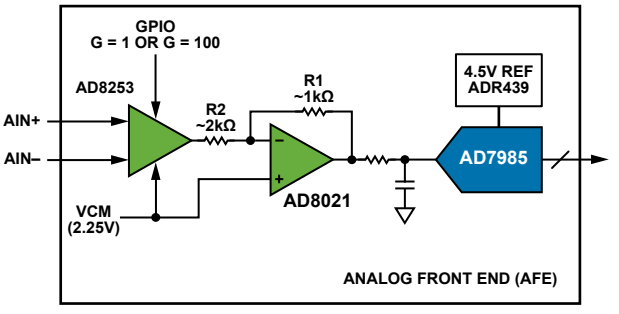

Figure 4. Low-noise wideband analog front end.

Since the complete system's noise budget is 15 nV/√Hz max, *referred to the input* (RTI), it is useful to calculate the dominant noise sources of each block to ensure that the 15-nV/√Hz hard limit is not exceeded. The AD8021 has an input-referred noise spec of <3 nV/√Hz, which is negligible when referred back to the input of the gain-of-100 AD8253 stage. The AD7985 has a specified SNR of 89 dB, using an external 4.5-V reference, for a noise resolution of <45 µV rms. Considering the Nyquist bandwidth of 300 kHz for the ADC, it will contribute ~83 nV/√Hz across this bandwidth. When referred back to the input of the AD7985, its <1 nV/√Hz will be negligible in the system, where the RTI noise sources are summed using a root-sum-of-squares calculation.

A further benefit of using the AD8253 is that it has digital gain control, which allows the system gain to be dynamically changed in response to changes in the input. This is achieved intelligently using the system's digital signal processing capability.

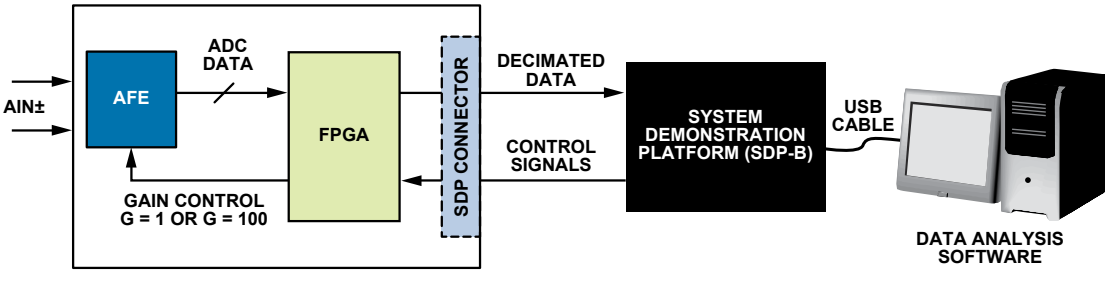

Figure 5. Using the analog front end (AFE) in a system with an FPGA, SDP, and PC.

The main function of digital processing in this application is to produce a higher-resolution output, using the AD7985 16-bit conversion results. This is achieved by decimating the data and switching the analog input gain automatically, depending on the input amplitude. This oversampling results in a lower output data rate than ADC sample rate, but with a greatly increased dynamic range.

To prototype the digital side of this application, a *field-programmable gate array* (FPGA) was used as the digital core. To rapidly debug the system, the analog circuitry and the FPGA were consolidated into a single board, shown in Figure 5, using the *system demonstration platform* (SDP) connector standard to allow easy USB connectivity to the PC. The SDP is a combination of reusable hardware and software that allows easy control of and capture from hardware over the most commonly used component interfaces.

The basic control flow is as follows:

- After power-up, a zero calibration operation is performed. The differential analog inputs of the AD8253 are shorted to ground and an AD7985 conversion is performed at each gain setting. The ADC values are stored for later use.
- After calibration, the AD7985 is given a periodic conversion start signal at a preset rate by the FPGA, in this case, approximately 600 kSPS. Each ADC result is read into the FPGA and passed to both the decimation and gain blocks.
- The gain block looks at the current ADC result, the previous ADC result, and the current gain setting—and determines what the most appropriate gain setting would be for the next ADC conversion. This process is detailed below.
- The decimation block takes in each ADC sample, the current PGA gain setting for that sample, and the calibration values that were stored earlier in the process. After 72 ADC samples have been received, the 23-bit output result is the average value of the 72 samples, with offset and gain taken into account.
- This 23-bit result is then converted into a twos-complement code and received from the FPGA in a format compatible with the Blackfin *serial port* (SPORT) and captured by the SDP-B hardware. The process is then repeated with a new word after every 72 ADC samples.

The two key modules implemented in the FPGA are the *decimator* and *gain calculator*. Detailed descriptions of each block follow.

Decimator

This block has an internal state machine that manages some sequential data-processing steps:

Each individual AD7985 sample is normalized to the same scale. For example: 4 mV input to the AD7985, with a 4.5-V reference, gives a code (4 mV/4.5 V × 65535) = 58 with G = 1. With G = 100, the ADC sees 400 mV at the input and gives an output code of 5825. For an ADC sample taken with an analog front-end (AFE) gain of 1, the sample must be multiplied by 100 to counteract the scaling effect when the AFE has a gain of 100. This ensures that these samples can be averaged and decimated correctly, regardless of the AFE gain setting.

With the decimator function in place, an initial test can be performed on the analog inputs.

With the inputs shorted, the system can be tested in a high-gain dc mode (see Figure 6).

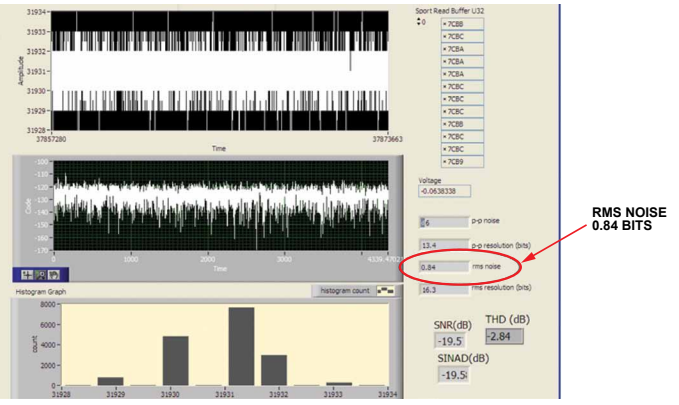

Figure 6. System high-gain dc mode noise test with inputs shorted.

Results show a p-p noise of 6 bits and an excellent rms noise of 0.84 LSB @ 16 bits = 0.654 µV rms. With a 2.12 V rms full-scale range, the dynamic range can be calculated as

$$DR = 20 \log_{10}(FS/rms\ noise) = \sim 130\ \text{dB}$$

Thus, the system easily meets the dynamic range target regarding noise. When tested with a 50 mV p-p ac analog input, significant distortion was noticed in the frequency domain (see Figure 7). This particular input amplitude highlights the worst case for the system—when the ac input amplitude is slightly larger than the range that is handled by the *Gain* = 100 mode and the system is regularly switching between the two modes. This range switching effect can also be exacerbated by the choice of gain thresholds, as discussed below. Mismatch between the offsets in each gain mode will show up as gross harmonic distortion, as the calculated output code jumps by the differential between the offsets in each range.

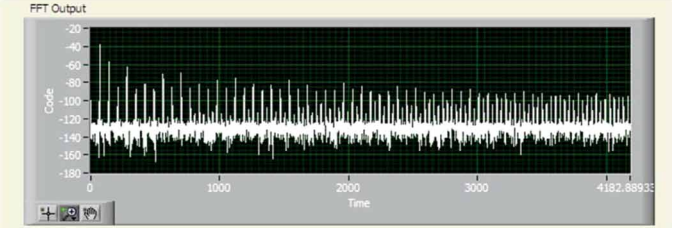

Figure 7. Worst-case input amplitude without calibration.

Simply calibrating out the zero offsets at each of the gain ranges can produce a dramatic reduction of signal distortion. In fact, calibration alone can reduce the harmonics by approximately 50 dB, as shown in Figure 8. With even a worst-case input tone, the harmonics have been reduced to the –110 dBFS level.

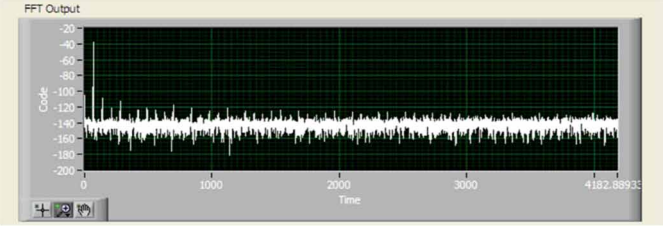

Figure 8. Worst-case input amplitude with calibration.

The calibrated offset is removed from the normalized sample. Since calibration is performed at both gain settings, the offset removed depends on the gain at the time the ADC sample was taken.

The normalized and offset-corrected sample is added into an accumulator register, which is reset at power-up and each time 72 samples have been received. When 72 samples have been received and added to the accumulator, the sum is passed to the divider, which divides the value in the accumulator by 72 to produce a 23-bit averaged result. An output flag is set to indicate that the division is complete and a new result is ready.

Gain Setting

This module outputs a new gain setting based on the current gain setting, two raw ADC samples, and some hard-coded threshold figures. Four thresholds are used in the system; selection of these thresholds is critical to maximizing the analog input range of the system, ensuring the G = 100 mode is used for as much of the signal range as possible, while also preventing the ADC input from being overranged. Note that this gain block operates on every raw ADC result, not on data that has been normalized. Bearing this in mind, an illustrative example of some thresholds that could be used in a system such as this (assuming a bipolar system with a midscale of zero) is as follows:

T1 (positive lower threshold): +162
(162 codes above midscale)

T2 (negative lower threshold): –162
(162 codes below midscale)

T3 (positive upper threshold): +32,507
(260 codes below positive full-scale)

T4 (negative upper threshold): –32,508
(260 codes above negative full-scale)

When in G = 1 mode, the inner limits, T1 and T2, are used. When an actual ADC result is between T1 and T2, gain is switched to G = 100 mode. This ensures that the analog input voltage that the ADC receives is maximized as quickly as possible.

When in G = 100 mode, the outer limits, T3 and T4, are used. If an ADC result is predicted to be above T3 or below T4, the gain is switched to the G = 1 mode to prevent the input of the ADC from being overranged (see Figure 9).

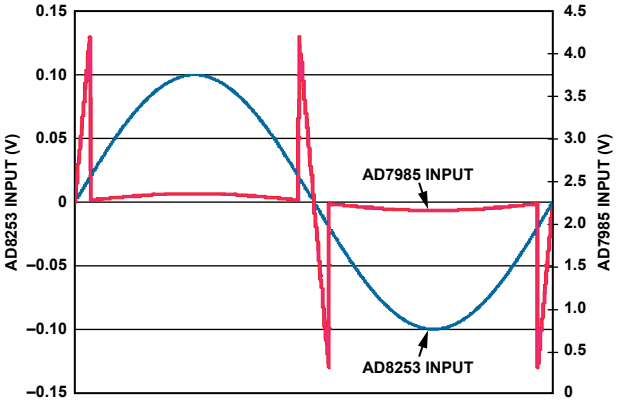

Figure 9. The gain from the amplifier input to the converter input is reduced by 100 when the ADC input is predicted to be outside the threshold limits. (Blue line: amplifier input; red line: converter input.)

When in G = 100 mode, if the algorithm predicts that the next ADC sample would be just outside the outer threshold (using a very rudimentary linear prediction), giving an ADC result of +32,510, the gain is switched to G = 1, and instead of +32,510 the next ADC result is +325.

In a system like this, to prevent *chatter* (rapidly repeated gain-switching around the threshold value), *hysteresis* (separation of the 100 to 1 and 1 to 100 switching levels) is important in determining the correct threshold limits. In the calculations of the actual limits used in this example, significant hysteresis is built in. If the system switches from the high-gain (G = 100) mode to the low-gain (G = 1) mode, the system's analog input voltage would have to be reduced by almost 50% in order to revert to the high-gain mode.

Performance of Full System

With fully optimized gain and decimation algorithms, the full system is ready to be tested. Figure 10 shows the system response to a large-signal input tone of –0.5 dBFS running at 1 kHz. When the PGA gain of 100 is factored in, the dynamic range achieved is 127 dB.

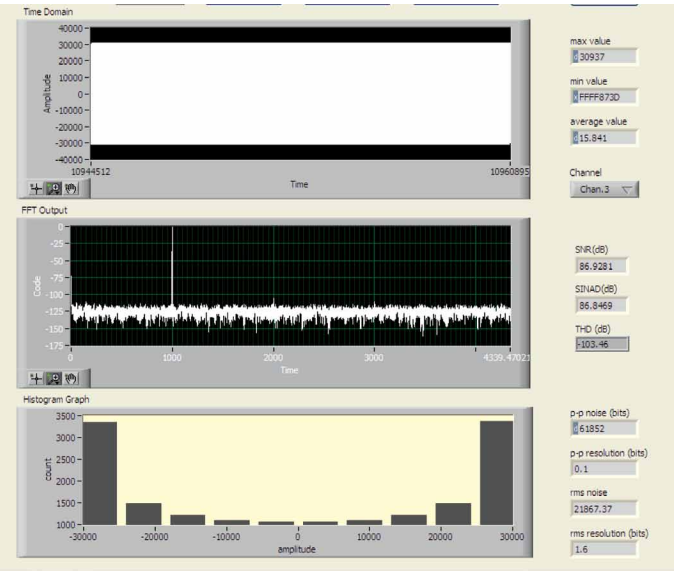

Figure 10. Response to large-scale 1-kHz signal.

Similarly, when tested for small-signal inputs in Figure 11, with an input tone of 70 Hz at –46.5 dBFS, up to 129 dB of dynamic range is achieved. The improvement in performance at the smaller input tone is expected, as no active switching of gain ranges occurs during this measurement.

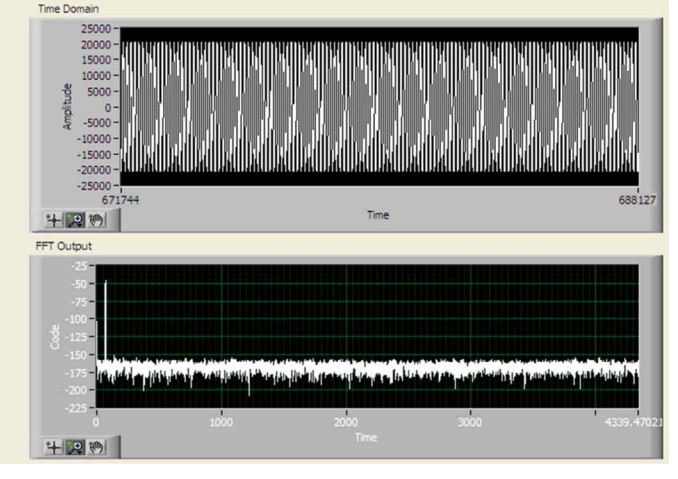

Figure 11. Response to small-scale input signal at 70 Hz.

Conclusion

The system's performance relies on the ability to switch the gain dynamically to handle both small- and large-signal inputs. While Σ-Δ technology provides excellent dynamic range, the SAR-based solution offers a way to dynamically change the front-end gain based on the input signal, without compromising system performance. This allows both small-signal and large-signal ac and dc inputs to be measured in real-time without waiting for system settling time or incurring large glitches due to delayed gain changing.

The key to the system is the ADC oversampling technique combined with the predictive gain-setting algorithm. Critical to the gain algorithm is how the input signal's slew rate is handled. For higher input slew rates, it could be necessary to customize the gain setting to respond more quickly to a signal that is approaching a level where the ADC input could be overranged. This could be achieved by tightening the thresholds used or with a more complex predictive analysis of the input signal using multiple samples instead of just two as described in this example. Conversely, in a system with a very low input slew rate, the thresholds could be widened to make greater use of the high gain mode without over-ranging the ADC input.

Although this article features the AD7985 ADC, the techniques used are applicable to other high-speed converters from Analog Devices. Using a faster ADC sampling rate, the end user could trade increased input bandwidth and faster output data rate for an increased oversampling ratio, achieving even greater dynamic range.

By utilizing additional gain ranges of the AD8253 VGA, instead of just G = 1 and G = 100, the impact of the gain change could be further minimized. In the current example, a small amount of distortion is introduced when the gain is switched. However, if the G = 10 range were to be used, for a three-step gain with an additional calibration point, a better system THD specification could be achieved.

Authors

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(continued from Page 18)

An antialiasing filter (AAF) is recommended between the AD8475 and the ADC's inputs. The AAF band-limits the signal and the noise presented to the ADC inputs to prevent undesirable aliasing effects and to improve the system SNR. Additionally, the AAF absorbs some of the ADC input transient currents, so the filter also provides some isolation between the amplifier and the ADC's switched-capacitor inputs. Typically, the AAF is implemented using a simple RC network as shown in Figure 1. The following equations describe the filter bandwidth:

$$FilterBW_{DIFF} = \frac{1}{2\pi \times 2RC_D}$$

$$FilterBW_{CM} = \frac{1}{2\pi \times RC_C}$$

In many cases, the filter's R and C values are optimized empirically to provide the necessary bandwidth, settling time, and drive capability for the ADC. Refer to the ADC data sheet for specific recommendations.

Conclusion

Together, the AD8475 and AD825x family of PGIAs implement a simple analog front end that provides high performance, functionality, and flexibility. A variety of programmable gain combinations are possible for both amplification and attenuation, allowing different measurement voltage ranges to be optimized. The AD825x's performance and programmability are well-suited for multiplexed measurement systems, and the AD8475 provides an excellent interface to precision analog-to-digital converters. The two amplifiers work well together to retain the integrity of the sensor signal, as a high-performance analog front end for industrial measurement systems.

See Circuit Note CN-0180, *Precision, Low Power, Single-Supply, Fully Integrated Differential ADC Driver for Industrial-Level Signals* for additional information on the AD8475 as a driver for a precision successive-approximation ADC.

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