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Analog Dialogue

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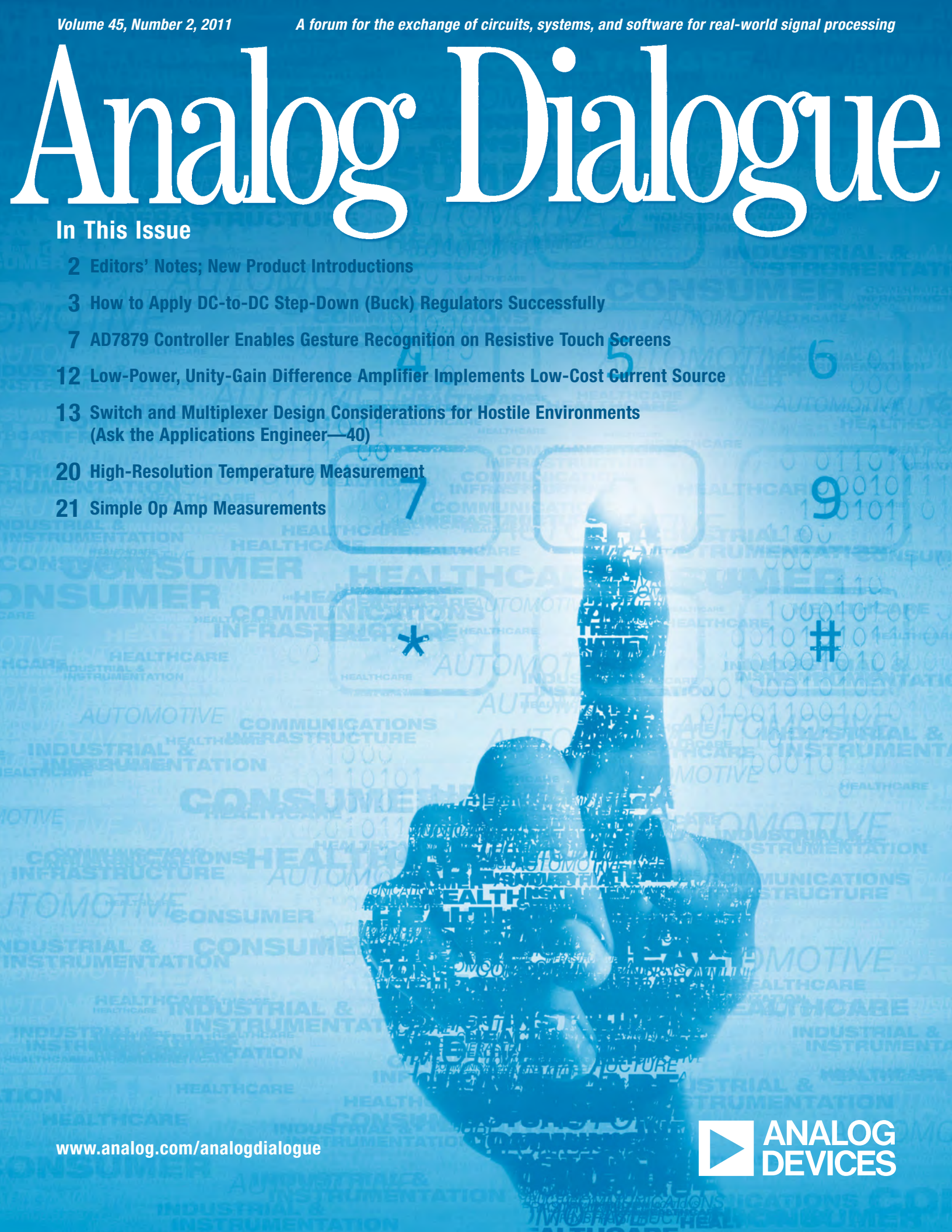

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Low-Power, Unity-Gain Difference Amplifier Implements Low-Cost Current Source

The article, "Difference Amplifier Forms Heart of Precision Current Source," published in *Analog Dialogue* in September 2009, showed how to use the AD8276 unity-gain difference amplifier and AD8603 micropower op amp to implement a precision current source. This article shows how the circuit can be simplified for use in low-cost, low-current applications—achieving ±1.5% accuracy from –40°C to +85°C. Page 12.

Switch and Multiplexer Design Considerations for Hostile Environments (Ask the Applications Engineer—40)

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Simple Op Amp Measurements

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PRODUCT INTRODUCTIONS: VOLUME 45, NUMBER 2

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

April

Amplifier, instrumentation, low-noise, 210°C **AD8229**
DAC, current-output, 14-bit, 2.5-GSPS **AD9739A**
Energy Meter, single-phase, multifunction **ADE7953**
Gyroscope, yaw-rate, vibration-rejecting, ±20,000°/sec **ADXRS649**
I/O Expander/Keypad Controller **ADP5589**
Mixer, balanced, dual, 2.2-GHz to 2.7-GHz **ADL5354**
Transceiver, low-power, zero-IF, 2.4-GHz **ADF7241**

May

ADC, pipelined, 8-bit, 500-MSPS **AD9484**
ADC, pipelined, 12-bit, 370-MSPS/500-MSPS **AD9434**
Controllers, synchronous buck, fast, low-noise **ADP1874/ADP1875**
Modulator, quadrature, 1200-MHz to 2400-MHz ... **ADRF6702**
Receiver, predistortion observation, 250-MHz **AD6641**
Sequencer, super, 8-supply, fault recording **ADM1168**
Switch, power, high-side, logic-level control **ADP197**

June

ADC, 8-channel, 18-bit, simultaneous-sampling **AD7608**
Amplifier, audio, 2.5-W, monophonic, Class-D **SSM2377**
Amplifier, instrumentation, 1-nV/√Hz input noise **AD8429**
Battery Monitor, lithium-ion **AD7280**
Controller, hot-swap, digital power/energy monitor **ADM1276**
DAC, dual, 16-bit, 1230-MSPS, TxDAC+ **AD9146**
DAC, quad, 16-bit, current output, HART **AD5757**
DAC, quad, 16-bit voltage/current outputs, HART .. **AD5755-1**
DDS, low-power, complete, up to 8 MHz output **AD9838**
Driver, LED, 9-channel, charge pump, lighting effects **ADP8866**
Generator, waveform, low-power, programmable **AD9837**
Gyro, yaw-rate, vibration-rejecting, ±250°/sec **ADXRS642**
Inclinometer/Accelerometer, precision, 3-axis .. **ADIS16210**
Micro-PMU, 800-mA buck regulator, 300-mA LDO **ADP5043**
Pin Electronics, 600-MHz, dual DCL with PPMU **ADATE318**
Processors, SHARC® **ADSP-21478/ADSP-21479**
Processor, Blackfin® **ADSP-BF592**
Regulator, low-dropout, dual, 300-mA **ADP223**
Sensor, inertial, 10-degrees-of-freedom **ADIS16407**
Sequencer, super, margining control, fault recording **ADM1169**
Switches, high-voltage, latch-up proof, quad SPST **ADG5212/ADG5213**
Transceiver, FSK, low-power, ISM band **ADF7023-J**

Analog Dialogue

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How to Apply DC-to-DC Step-Down (Buck) Regulators Successfully

By Ken Marasco

Smartphones, tablets, digital cameras, navigation systems, medical equipment, and other low-power portable devices often contain multiple integrated circuits manufactured on different semiconductor processes. These devices typically require several independent supply voltages, each usually different than the voltage supplied by the battery or external ac-to-dc power supply.

Figure 1 shows a typical low-power system operating with a Li-Ion battery. The battery's usable output varies from 3 V to 4.2 V, while the ICs require 0.8 V, 1.8 V, 2.5 V, and 2.8 V. A simple way to reduce the battery voltage to a lower dc voltage is to use a *low-dropout regulator*[1] (LDO). Unfortunately, power not delivered to the load is lost as heat, making LDOs inefficient when V_{IN} is much greater than V_{OUT}. A popular alternative, the *switching converter*, alternately stores energy in an inductor's magnetic field, and releases the energy to the load at a different voltage. Its reduced losses make it a better choice for high efficiency. *Buck*, or *step-down* converters—covered here—provide lower voltage. *Boost*, or *step-up* converters—to be covered in a future article—provide higher output voltage. Switching converters that include internal FETs as switches are called *switching regulators*,[2] while devices requiring external FETs are called *switching controllers*.[3] Most low-power systems use both LDOs and switching converters to achieve cost and performance objectives.

Buck regulators consist of two switches, two capacitors, and an inductor, as shown in Figure 2. Nonoverlapping switch drives ensure that only one switch is on at a time to avoid unwanted current "shoot through." In Phase 1, Switch B is open, and Switch A is closed. The inductor is connected to V_{IN}, so current flows from V_{IN} to the load. The current increases due to the positive voltage across the inductor. In Phase 2, Switch A is open and Switch B is closed. The inductor is connected to ground, so current flows from ground to the load. The current decreases due to the negative voltage across the inductor, and energy stored in the inductor is discharged into the load.

Note that the switching regulator operation can be continuous or discontinuous. When operating in *continuous conduction mode* (CCM), the inductor current never drops to zero; when operating in *discontinuous conduction mode* (DCM), the inductor current can drop to zero. Low-power buck converters rarely operate in DCM. The *current ripple*, shown as ΔI_L in Figure 2, is typically designed to be 20% to 50% of the nominal load current.

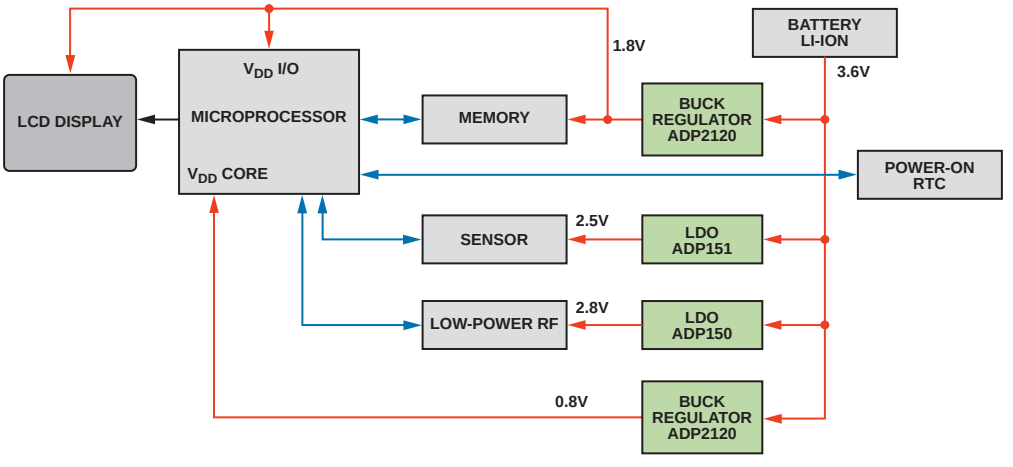

Figure 1. Typical low-power portable system.

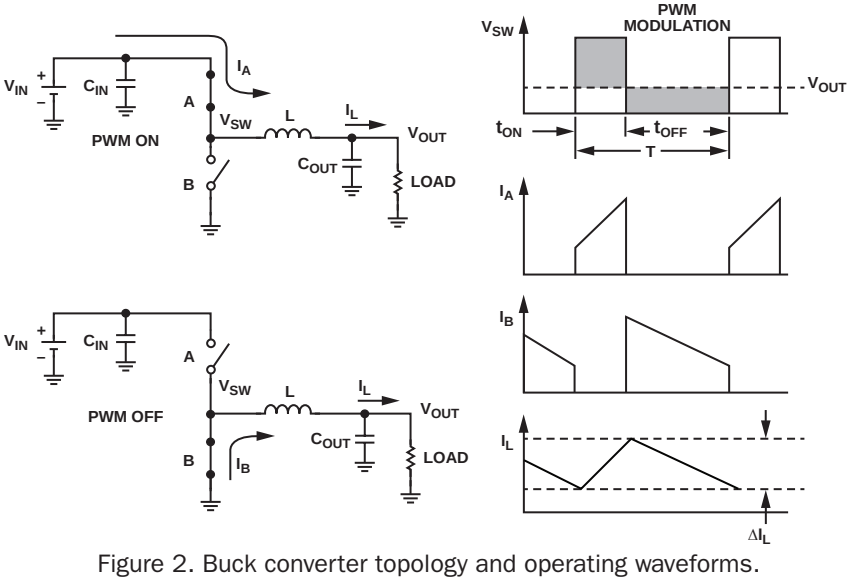

Figure 2. Buck converter topology and operating waveforms.

In Figure 3, Switch A and Switch B have been implemented with PFET and NFET switches, respectively, to create a synchronous buck regulator. The term *synchronous* indicates that a FET is used as the lower switch. Buck regulators that use a Schottky diode in place of the lower switch are defined as asynchronous (or nonsynchronous). For handling low power, synchronous buck regulators are more efficient because the FET has a lower voltage drop than a Schottky diode. However, the synchronous converter's efficiency at light load will be compromised if the bottom FET is not released when the inductor current reaches zero, and additional control circuitry increases the complexity and cost of the IC.

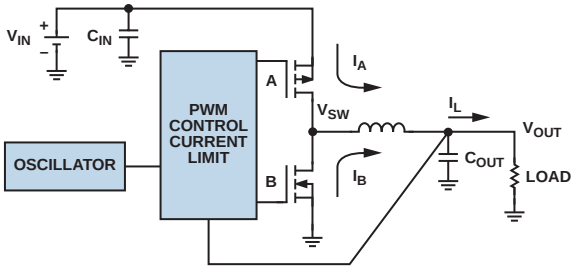

Figure 3. Buck regulator integrates oscillator, PWM control loop, and switching FETs.

Today's low-power synchronous buck regulators use pulse-width modulation (PWM) as the primary operating mode. PWM holds the frequency constant and varies the pulse width (t_{ON}) to adjust the output voltage. The average power delivered is proportional to the duty cycle, D, making this an efficient way to provide power to a load.

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} \approx \frac{V_{OUT}}{V_{IN}}$$

The FET switches are controlled by a pulse-width controller, which uses either voltage- or current feedback in a control loop to regulate the output voltage in response to load changes. Low-power buck converters generally operate between 1 MHz and 6 MHz. Higher switching frequencies allow the use of smaller inductors, but efficiency is decreased by approximately 2% for every doubling of the switching frequency.

PWM operation does not always improve system efficiency at light loads. Consider, for example, the power circuitry for a graphics card. As the video content changes, so does the load current on the buck converter driving the graphics processor. Continuous PWM operation can handle a wide range of load currents, but the efficiency rapidly degrades at light loads because the power required by the regulator consumes a larger percentage of the total power delivered to the load. For portable applications, buck regulators incorporate additional power-saving techniques—such as pulse-frequency modulation (PFM), pulse skipping, or a combination of both.

Analog Devices defines efficient light-load operation as *power-save mode* (PSM). When the power-save mode is entered, an offset induced in the PWM regulation level causes the output voltage to rise, until it reaches approximately 1.5% above the PWM regulation level, at which point PWM operation turns off: both power switches are off, and *idle* mode is entered. C_{OUT} is allowed to discharge until V_{OUT} falls to the PWM regulation voltage. The device then drives the inductor, causing V_{OUT} to again rise to the upper threshold. This process is repeated as long as the load current is below the power-save current threshold.

The ADP2138 is a compact 800-mA, 3-MHz, step-down dc-to-dc converter. Figure 4 shows a typical applications circuit. Figure 5 shows the improvement in efficiency between forced PWM and automatic PWM/PSM operation. Due to the variable frequency, PSM interference can be hard to filter, so many buck regulators include a MODE pin (shown in Figure 4) that allows the user to force continuous PWM operation or allow automatic PWM/PSM operation. The MODE pin can be hardwired for either operating mode or dynamically switched when needed to save power.

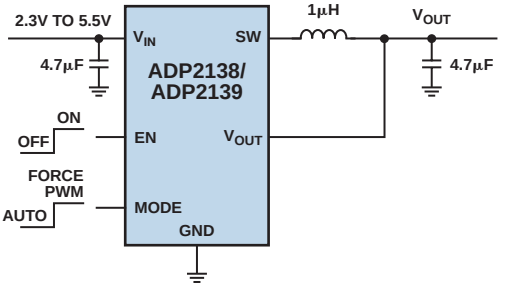

Figure 4. ADP2138/ADP2139 typical applications circuit.

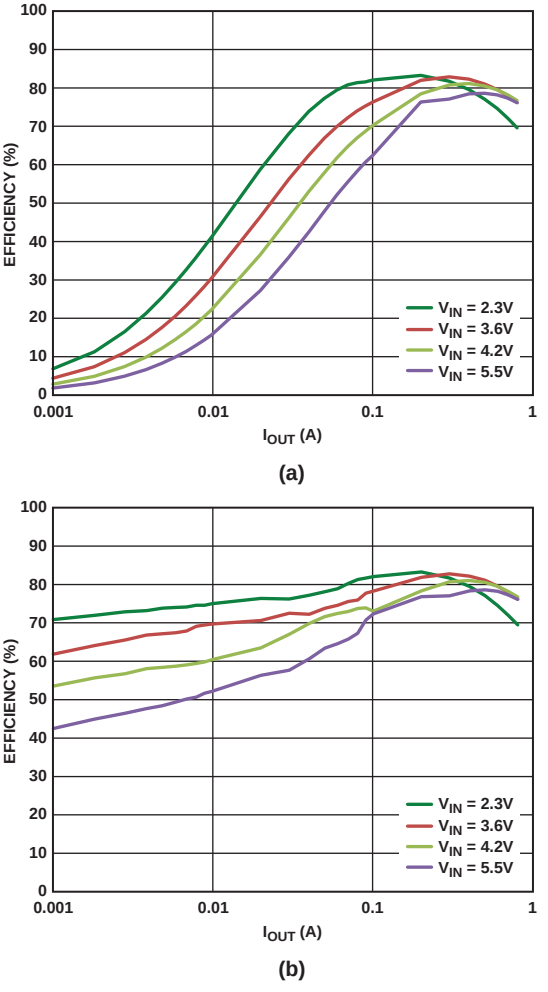

Figure 5. ADP2138 efficiency in (a) continuous PWM mode and (b) PSM mode.

Buck Regulators Improve Efficiency

Increased efficiency allows longer battery operating times before replacement or recharging, a highly desirable feature in new portable device designs. For example, a rechargeable Li-Ion battery can drive a 500-mA load at 0.8 V using the ADP125 LDO, as shown in Figure 6. The LDO's efficiency, $V_{OUT}/V_{IN} \times 100\%$, or 0.8/4.2, is only 19%. LDOs cannot store the unused energy, so the 81% (1.7 W) of power not delivered to the load is dissipated as heat

within the LDO, which could cause a handheld device to heat up quickly. Using the ADP2138 switching regulator, which offers 82% operating efficiency with a 4.2-V input and 0.8-V output, delivers more than four times the efficiency and reduces the temperature rise of the portable device. Such substantial improvements in system efficiency have resulted in large numbers of switching regulators being designed into portable devices.

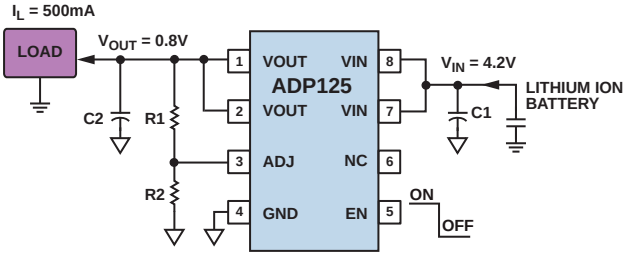

Figure 6. ADP125 low-dropout regulator can drive 500-mA loads.

Key Buck Converter Specifications and Definitions

Input Voltage Range: A buck converter's input voltage range determines the lowest usable input supply voltage. The specifications may show a wide input voltage range, but V_{IN} must be greater than V_{OUT} for efficient operation. For example, a regulated 3.3 V output voltage requires an input voltage above 3.8 V.

Ground or Quiescent Current: I_Q is the dc bias current not delivered to the load. Devices with lower I_Q provide higher efficiency. I_Q can be specified for many conditions, however, including switching *off*, zero load, PFM operation, or PWM operation, so it is best to look at actual operating efficiency data at specific operating voltages and load currents to determine the best buck regulator for an application.

Shutdown Current: The input current consumed when the enable pin has been set to *off*. This current, usually well below 1 μA for low-power buck regulators, is important during long standby times on the battery while the portable device is in sleep mode.

Output Voltage Accuracy: Analog Devices buck converters are designed for high output voltage accuracy. Fixed-output devices are factory trimmed to better than ±2% at 25°C. Output voltage accuracy is specified over the operating temperature, input voltage, and load current ranges, with worst-case inaccuracies specified as ±*x*%.

Line Regulation: Line regulation is the change in output voltage caused by a change in the input voltage, at the rated load.

Load Regulation: Load regulation is the change of the output voltage for a change in the output current. Most buck regulators can hold the output voltage essentially constant for slowly changing load current.

Load Transients: Transient errors can occur when the load current quickly changes from low to high, causing mode switching between PFM and PWM or from PWM to PFM operation. Load transients are not always specified, but most data sheets have plots of load transient responses at different operating conditions.

Current Limit: Buck regulators such as the ADP2138 incorporate protection circuitry to limit the amount of positive current flowing through the PFET switch and the synchronous rectifier. The positive current control limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

Soft Start: It is important for buck regulators to have an internal soft-start function that ramps the output voltage in a controlled manner upon startup to limit the inrush current. This prevents input voltage from a battery or high-impedance power source from dropping when it is connected to the input of the converter. After the device is *enabled*, the internal circuit begins the power-up cycle.

Start-Up Time: Start-up time is the time between the rising edge of the enable signal and when V_{OUT} reaches 90% of its nominal value. This test is usually performed with V_{IN} applied and the enable pin toggled from *off* to *on*. In cases where the enable is connected to V_{IN}, when V_{IN} is toggled from *off* to *on*, the start-up time can substantially increase because the control loop takes time to stabilize. Start-up time of a buck regulator is important for applications where the regulator is frequently turned on and off to save power in portable systems.

Thermal Shutdown (TSD): If the junction temperature rises above the specified limit, the thermal shutdown circuit turns the regulator off. Extreme junction temperatures can be the result of high current operation, poor circuit board cooling, or high ambient temperature. Hysteresis is included in the protection circuit to prevent return to normal operation until the on-chip temperature drops below the preset limit.

100% Duty Cycle Operation: With a drop in V_{IN} or an increase in I_{LOAD}, the buck regulator reaches a limit where the PFET switch is on 100% of the time and V_{OUT} drops below the desired output voltage. At this limit, the ADP2138 smoothly transitions to a mode where the PFET switch stays on 100% of the time. When the input conditions change, the device immediately restarts PWM regulation with no overshoot of V_{OUT}.

Discharge Switch: In some systems, if the load is very light, a buck regulator's output can stay high for some time after the system enters *sleep* mode. Then, if the system starts the power-on sequence before the output voltage has discharged, the system may latch up, or devices can be damaged. The ADP2139 buck regulator uses an integrated switched resistor (typically 100 Ω) to discharge the output when the enable pin goes low or when the device enters undervoltage lockout or thermal shutdown.

Undervoltage Lockout: Undervoltage lockout (UVLO) ensures that voltage is supplied to the load only when the system input voltage is above the specified threshold. UVLO is important because it allows the device to power on only when the input voltage is at or above the value required for stable operation.

Conclusion

Low-power buck regulators demystify switching dc-to-dc converter design. Analog Devices offers a family of highly integrated buck regulators that are rugged, easy to use, and cost effective—and require minimal external components to achieve high operating efficiency. System designers can use the design calculations presented in the applications section of the data sheet or use the ADIsimPower™[4] design tool. Selection guides, data sheets, and application notes for Analog Devices buck regulators can be found at www.analog.com/en/power-management/products/index.html. For further information, consult "Design Support" at www.analog.com.

References

(*Information on all ADI components can be found at www.analog.com.*)

[1] www.analog.com/en/power-management/linear-regulators/products/index.html.

[2] www.analog.com/en/power-management/switching-regulators-integrated-fet-switches/products/index.html.

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Author

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APPENDIX

3-MHz Synchronous Step-Down DC-to-DC Converters Drive 800-mA Loads

The ADP2138 and ADP2139 step-down dc-to-dc converters are optimized for use in wireless handsets, personal media players, digital cameras, and other portable devices. They can operate in forced pulse-width modulation (PWM) mode for lowest ripple, or can automatically switch between PWM mode and power-save mode to maximize efficiency at light loads. The 2.3-V to 5.5-V input range allows the use of standard power sources, including lithium, alkaline, and NiMH cells and batteries. Multiple fixed-output-voltage options from 0.8 V to 3.3 V are available, with 800-mA load capability and 2% accuracy. An internal power switch and synchronous rectifier improve efficiency and minimize the number of external components. The ADP2139, shown in Figure A, adds an internal discharge switch. Available in compact 1-mm × 1.5-mm, 6-ball WLCSP packages, the ADP2138 and ADP2139 are specified from −40°C to +125°C and priced at $0.90 in 1000s.

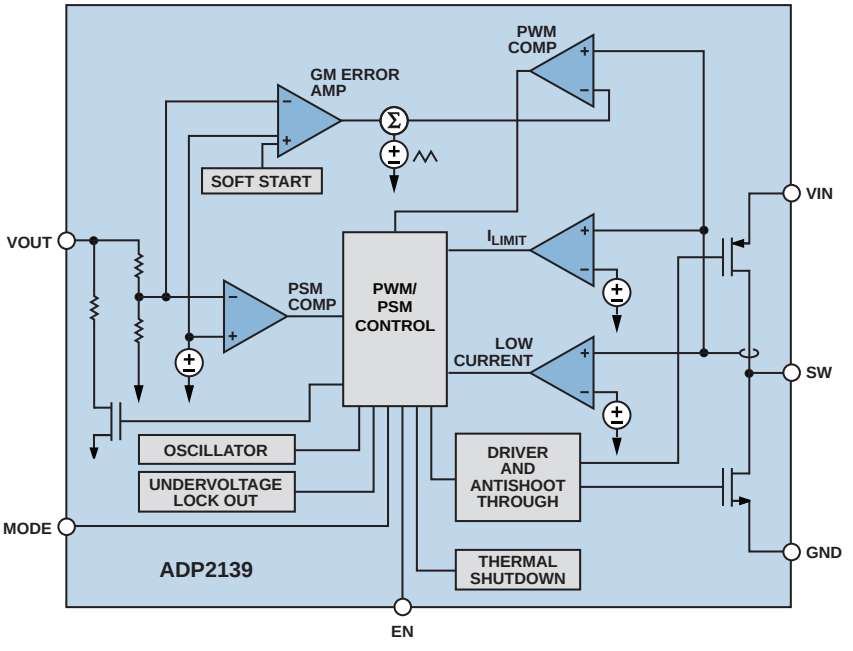

Figure A. ADP2139 functional block diagram.

AD7879 Controller Enables Gesture Recognition on Resistive Touch Screens

By Javier Calpe, Italo Medina, Alberto Carbajo, María José Martínez

An enhanced, low-cost user interface using touch is a valuable feature for a variety of consumer, medical, automotive, and industrial devices. In many consumer applications, designers prefer expensive capacitive touch screens to resistive technologies because they can track a large number of fingers and seem to offer a friendlier interaction with the user. At present, low-cost resistive technologies fill a market niche where only a single touch is required, extremely accurate spatial resolution is paramount, a stylus facilitates specific functionality—such as Asian-language character recognition, or in environments where users must wear gloves.

Although resistive technologies have conventionally been used to detect the position of a *single touch* on the screen, this article offers a new *dual-touch* concept that uses the AD7879 resistive touch-screen controller to detect the most common two-finger gestures (zoom, pinch, and rotation) using inexpensive resistive touch screens.

The Classical Approach to Resistive Touch Screens

Typical resistive screens have two parallel *indium tin-oxide* (ITO) conducting layers separated by a gap (Figure 1). The edge electrodes of the upper layer (Y) are rotated 90° with respect to those of the lower layer (X). A "touch" occurs when the two layers are brought into electrical contact by pressure applied to a small area of the screen. If a dc voltage is applied between the two electrodes of the top layer, while the lower layer floats, the touch brings the lower layer to the same voltage as the touch point. The touch coordinate in the direction of the top layer is identified by measuring the voltage on the bottom layer to determine the ratio of the resistance at the touch point to the total resistance. Then, electrical connections for the layers are swapped, and the coordinate of the touch point on the other axis is obtained.

The layer supplied with the dc voltage, which carries a current inversely proportional to its impedance, is called the *'active' layer*. The layer the voltage is measured from is called the *'passive' layer*, since no relevant current flows through it. When a single touch occurs, a voltage divider is formed in the active layer, and the passive-layer voltage measurement allows an analog-to-digital converter to read the voltage proportional to the distance of the touch point from the negative electrode [1].

The classical 4-wire resistive touch screen is popular for single-touch applications because of its low cost. Resistive approaches for *multitouch* have employed various techniques that always include a matrix layout screen—but at a daunting increase in screen manufacturing cost. Furthermore, the controller requires many inputs and outputs to measure and drive the various screen strips, increasing controller cost and measurement time.

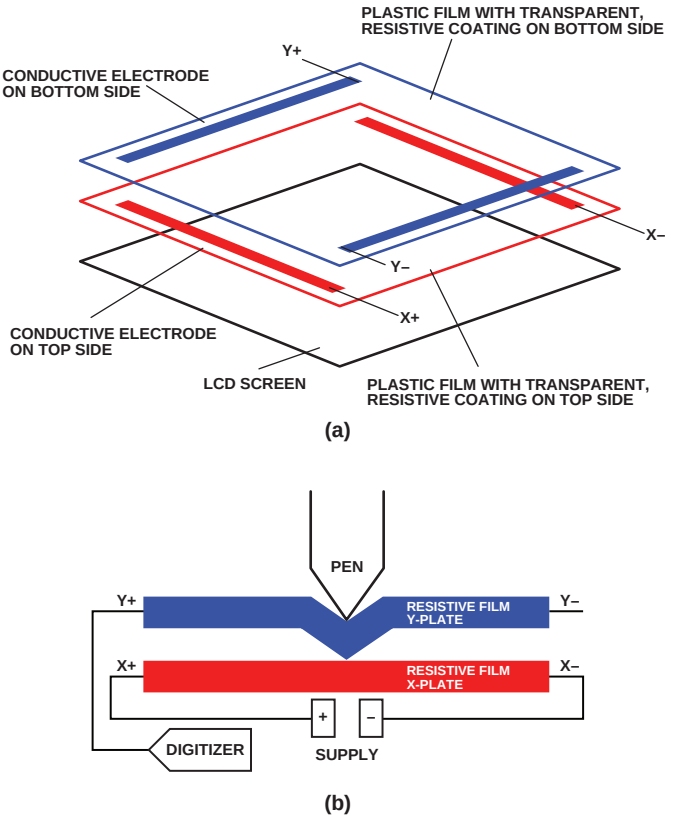

Figure 1. (a) Construction of a resistive touch screen, (b) electrical contact when user touches the screen.

Beyond Single Touch

Nevertheless, more information can be extracted from resistive touch screens by understanding and modeling the physics behind the process. When two touches occur, a segment of resistance from the passive screen, plus the resistance of the touch contacts, is paralleled with the conducting segment of the active screen, so the impedance seen by the supply is reduced and current increases. The classical approach to resistive controllers assumes that the *current through the active layer is constant, and the passive layer is equipotential*. With two touches, these assumptions no longer hold, so additional measurements are required to extract the desired information.

A model of dual touch sensing in a resistive screen is shown in Figure 2. R_{touch} is the contact resistance between layers; in most of the screens currently available, it is typically of the same order as the resistance of both layers. If a constant current, I, flows through the terminals of the active layer, the voltage across the active layer is as follows:

$$V_+ - V_- = I\left(R_u + R_d + R_a \| (2R_{touch} + R_p)\right)$$

$$= I\left(R_u + R_d + \frac{R_a(2R_{touch} + R_p)}{R_a + 2R_{touch} + R_p}\right)$$

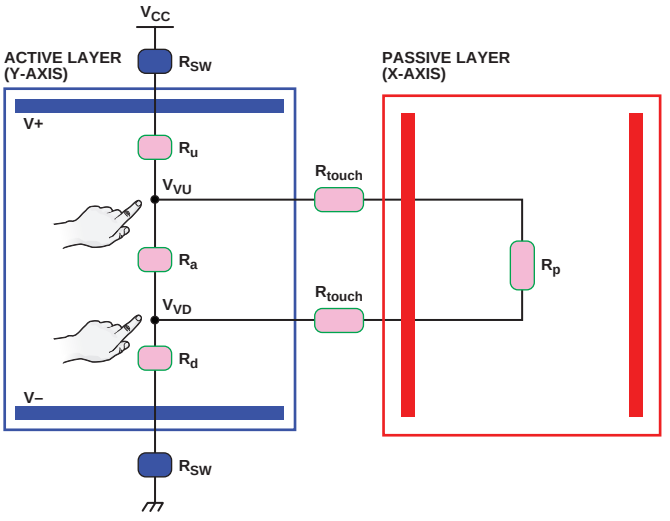

Figure 2. Basic model of dual touch in resistive screens.

Gesture Recognition

The idea behind gesture recognition can be better described using a *pinch* as an example. A pinch gesture starts with touches by two well-separated fingers. This produces a double contact, which reduces the impedance of the screen—and, thus, the voltage difference between the plates of the active layer. As the fingers are brought closer together, the paralleled area decreases, so the impedance of the screen increases, as does the voltage difference between the plates of the active layer.

When tightly pinched, the parallel resistance approaches zero and $R_u + R_d$ increases to the total resistance, so the voltage increases to

$$V_+ - V_- = I\left(R_u + R_d\right) = I \times R_{layer}$$

Figure 3 shows an example where the pinch is executed along the vertical (Y) axis. The voltage between the electrodes of one of the layers is constant while the other layer shows a step decrease when the gesture starts, followed by an increase as the fingers come closer together.

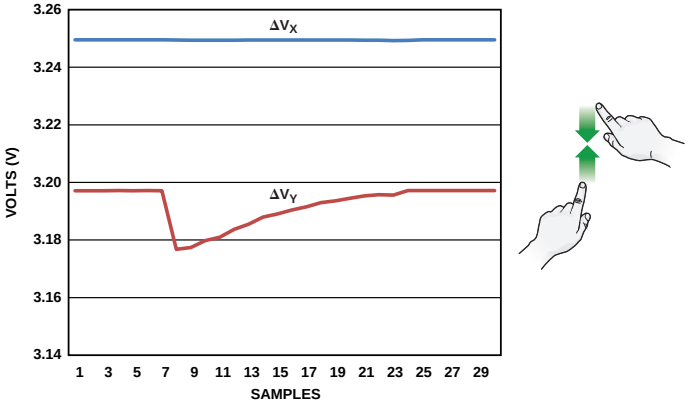

Figure 3. Voltage measurements when a vertical pinch is performed.

Figure 4 shows the voltage measurements when a pinch is executed at a slant. In this case, both voltages show the step decrease and slow recovery. The ratio between the two recovery rates, normalized by the resistances of each layer, can be used to detect the angle of the gesture.

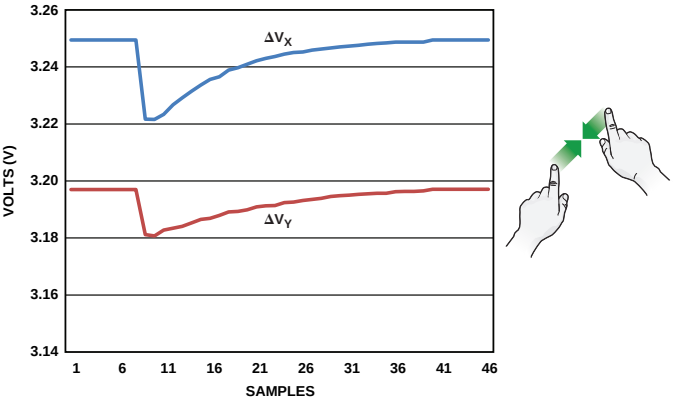

Figure 4. Voltage measurements when a diagonal pinch is executed.

If the gesture is a *zoom* (fingers moved apart), the behavior can be deduced from the previous discussion. Figure 5 shows the voltage trends measured in both active layers when zoom gestures are executed along each axis and in an oblique direction.

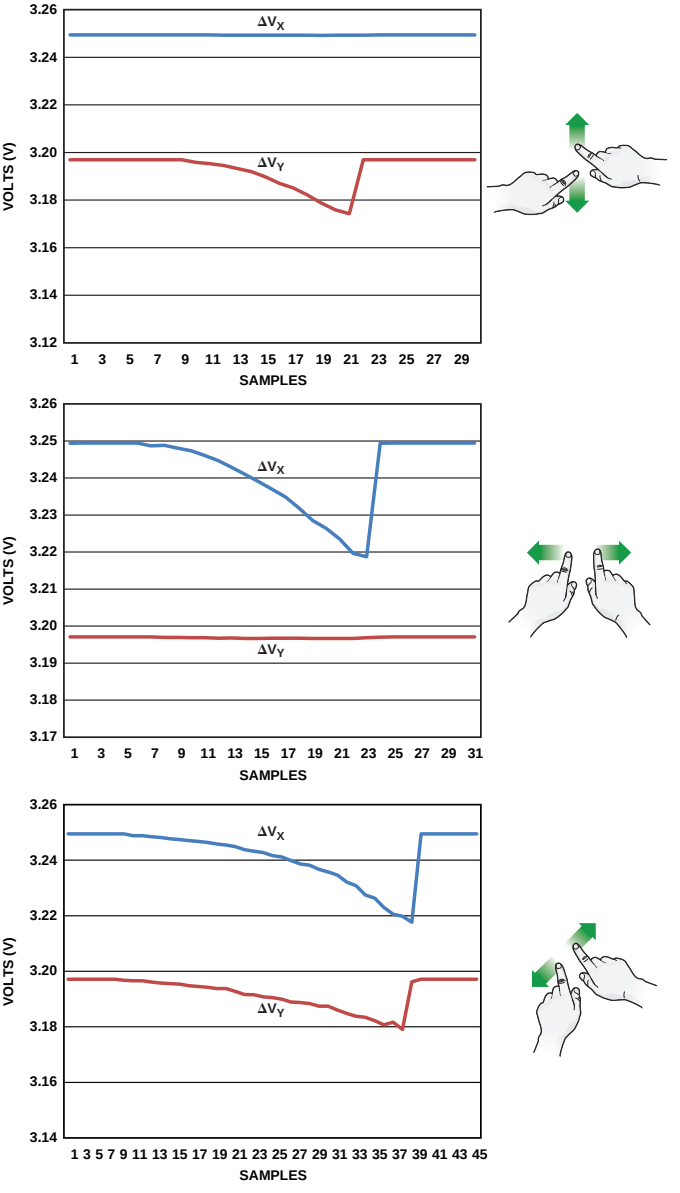

Figure 5. Voltage trends when zooms are executed in differing directions.

Detecting Gestures with the AD7879

The AD7879 touch-screen controller is designed to interface with 4-wire resistive touch screens. In addition to sensing touch, it also measures temperature and the voltage on an auxiliary input. All four touch measurements—along with temperature, battery, and auxiliary voltage measurements—can be programmed into its on-chip sequencer.

The AD7879, accompanied by a pair of low-cost op amps, can perform the above pinch and zoom gesture measurements, as shown in Figure 6.

The following steps describe the procedure to recognize gestures:

1) In the first semi-cycle, a dc voltage is applied to the top (active) layer, and the voltage at the X+ pin (corresponding to $V_{Y+} - V_{Y-}$) is measured. This provides information related to motion (together or apart) in the Y direction.
2) In the second semi-cycle, a dc voltage is applied to the bottom (active) layer, and the voltage at the Y+ pin (corresponding to $V_{X+} - V_{X-}$) is measured. This provides information related to motion (together or apart) in the X direction.

The circuit in Figure 6 requires the differential amplifiers to be protected against shorts to V_{DD}. During the first semi-cycle, the output of the lower amplifier is shorted to V_{DD}. During the second semi-cycle, the output of the upper amplifier is shorted to V_{DD}. To avoid this, two external analog switches can be controlled by the AD7879's GPIO, as shown in Figure 7.

In this case, the AD7879 is programmed in slave conversion mode, and only one semi-cycle is measured. When the AD7879 completes the conversion, an interrupt is generated. The host processor reprograms the AD7879 to measure the second semi-cycle and changes the value of the AD7879 GPIO. At the end of the second conversion, results for both layers are stored in the device.

A rotation can be modeled as a simultaneous zoom in one direction and an orthogonal pinch, so detecting one is not difficult. The challenge is discriminating clockwise (CW) and counterclockwise (CCW) gestures; this cannot be achieved by the process described above. Detecting both a rotation and its direction requires measurements on both layers, active and passive, as shown in Figure 8. Since the circuit in Figure 7 cannot meet this requirement, a new topology is proposed in Figure 9.

The topology proposed in Figure 9 allows the following:

- Semi-Cycle 1: Voltage is applied to the Y layer while ($V_{Y+} - V_{Y-}$), V_{X-}, and V_{X+} are measured. The AD7879 generates an interrupt after each measurement is completed, allowing the processor to change the GPIO configuration.
- Semi-Cycle 2: Voltage is applied to the X layer while ($V_{X+} - V_{X-}$), V_{Y-}, and V_{Y+} are measured.

The circuit of Figure 9 permits all the voltages required to achieve full performance to be measured, namely, a) single touch location, b) zoom, pinch, and rotation gesture detection and quantification, and c) CW vs. CCW rotation discrimination. Single-touch operation when performing a dual-touch gesture provides an estimation of the gesture centroid.

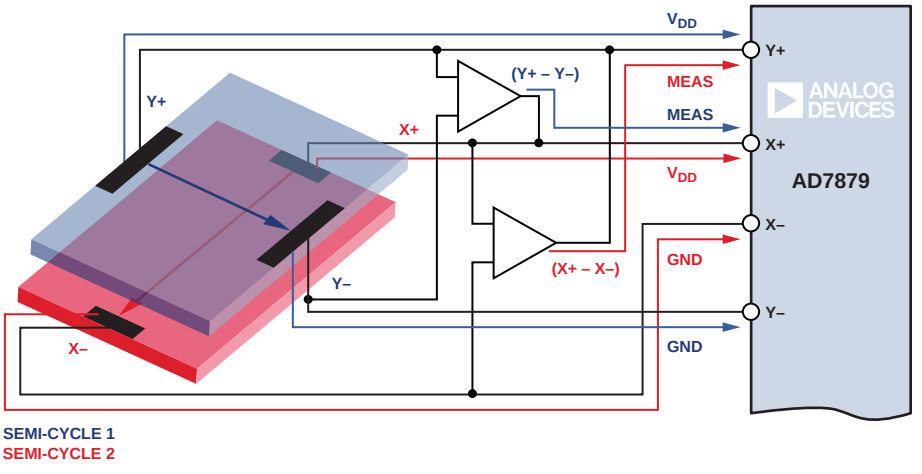

Figure 6. Application diagram for basic gesture detection.

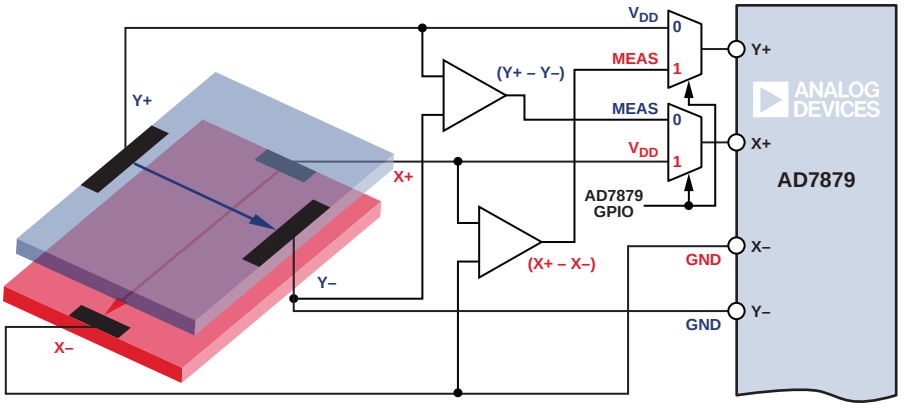

Figure 7. Application diagram that avoids shorting the amplifier outputs to V_{DD}.

Practical Hints

The variations in voltage associated with soft gestures are quite subtle. The robustness of the system can be improved by increasing these variations by means such as adding a small resistance between the electrodes of the screen and the pins of the AD7879; this will increase the voltage drop in the active layer, with some loss of accuracy of single-touch positioning.

An alternative is to add a resistor to only the low-side connection, sensing just the X– and Y– electrodes when they are active layers. By doing this, some gain can be applied, since the dc value is pretty low.

Analog Devices offers a variety of amplifiers and multiplexers that fulfill the needs of the applications shown in Figure 6, Figure 7, and Figure 9. The AD8506 dual op amp and ADG16xx family of analog multiplexers, which offers low on resistance with a single 3.3-V supply, were used to test the circuits.

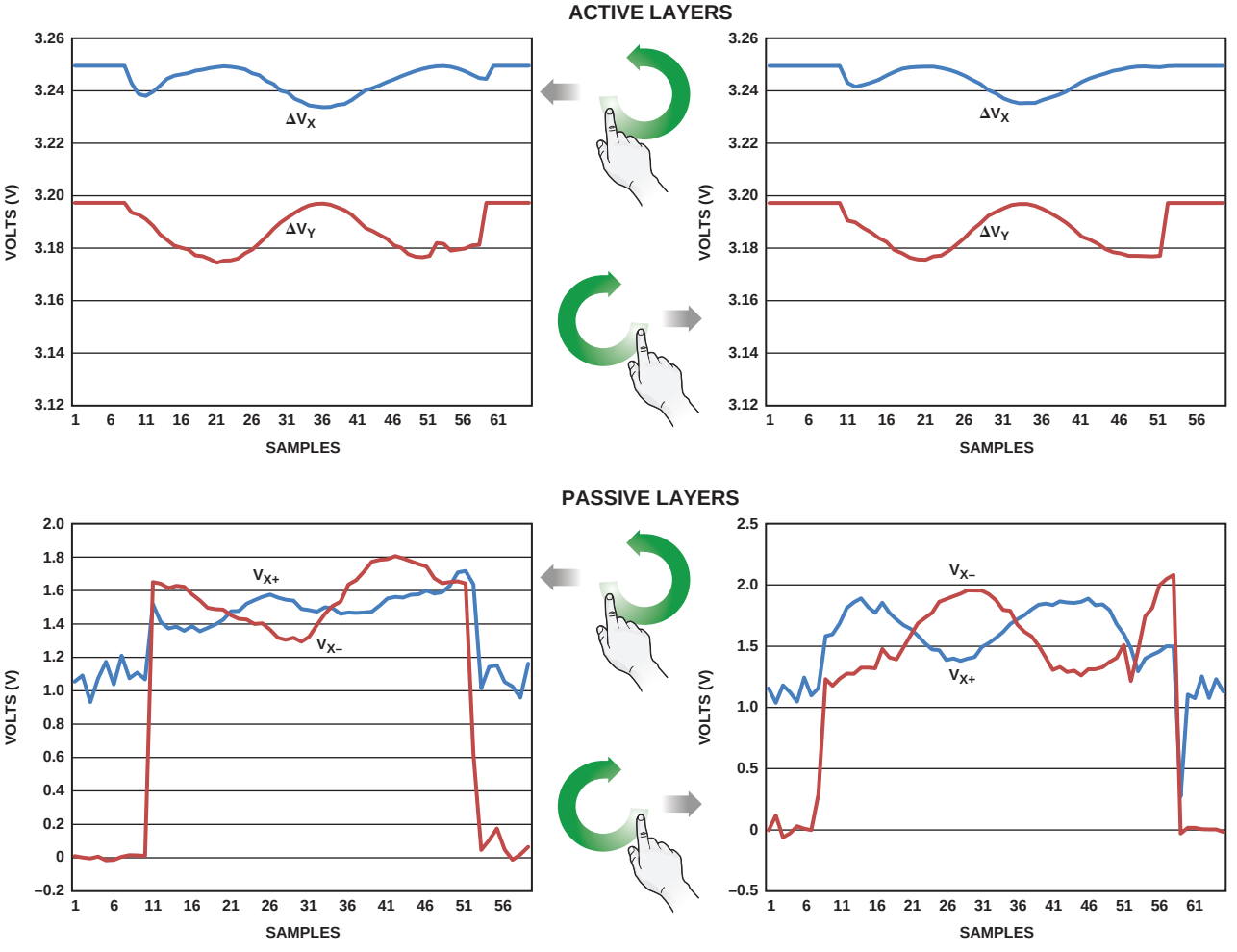

Figure 8. Voltage measurements when CW and CCW rotations are executed.

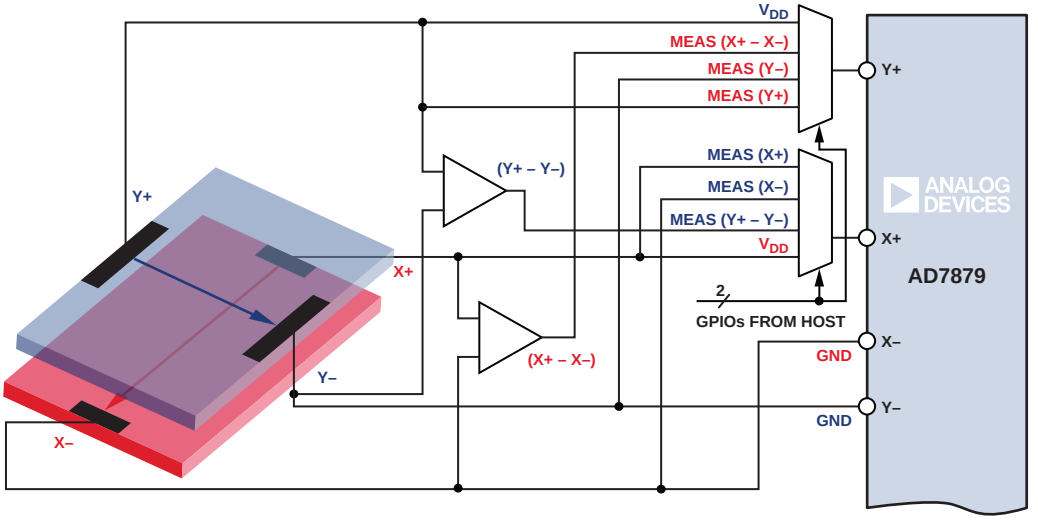

Figure 9. Application diagram for single touch location and gesture detection.

Conclusion

Zooms, pinches, and rotations can be detected using the AD7879 controller with minimum ancillary circuitry. These gestures can be identified with measurements in the active layer only. Rotation direction discrimination can be achieved by measuring the voltage in the passive layer, which can be achieved by using two GPIOs from the host processor. Fairly simple algorithms executed in this processor can identify zooms, pinches, and rotations, estimating their range, angle, and direction.

Acknowledgments

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The authors wish to thank Colin Lyden, John Cleary, and Susan Pratt for fruitful discussions.

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(Information on all ADI components can be found at www.analog.com.)

[1] Finn, Gareth. "New Touch-Screen Controllers Offer Robust Sensing for Portable Displays." *Analog Dialogue*, Vol. 44, No. 2. February 2010.

http://www.analog.com/library/analogDialogue/archives/44-02/touch_screen.html.

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Low-Power, Unity-Gain Difference Amplifier Implements Low-Cost Current Source

By David Guo

In "Difference Amplifier Forms Heart of Precision Current Source," published in *Analog Dialogue* in September 2009, the AD8276 unity-gain difference amplifier and AD8603 micropower op amp implement a precision current source. Figure 1 shows how the circuit can be simplified for use in low-cost, low-current applications.

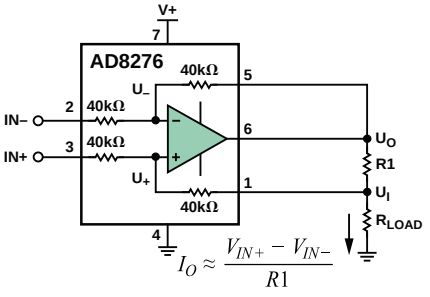

Figure 1. Simple current source for low-cost and low-current applications.

The output current, I_O, is approximately equal to the differential input voltage, $V_{IN+} - V_{IN-}$, divided by $R1$, as shown in the following derivation.

$$\frac{V_{IN-} - U_-}{40k} = \frac{U_- - U_O}{40k} \Rightarrow U_- = \frac{V_{IN-} + U_O}{2}$$

$$\frac{V_{IN+} - U_+}{40k} = \frac{U_+ - U_I}{40k} \Rightarrow U_+ = \frac{V_{IN+} + U_I}{2}$$

$$U_- = U_+ \Rightarrow V_{IN+} - V_{IN-} = U_O - U_I$$

Thus, the differential input voltage appears across R1.

$$R1 << 40k \Rightarrow I_O \approx I_{R1} \Rightarrow I_O \approx \frac{V_{IN+} - V_{IN-}}{R1}$$

Experimental Setup

1. AD5750EVB (AD5750 driver and AD5662 16-bit *nano*DAC®) provides a bipolar input to the AD8276.
2. OI-857 multimeter measures input voltage, output voltage, and resistance.
3. The nominal values of R1 and R_{LOAD} are 280 Ω and 1 kΩ, respectively; the measured values are 280.65 Ω and 997.11 Ω, respectively.
4. The output current is calculated by dividing the measured voltage by R_{LOAD}.

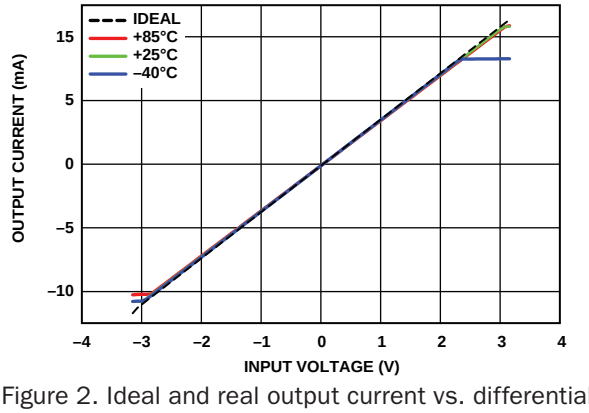

Figure 2. Ideal and real output current vs. differential input voltage.

Experimental Results

Figure 2 shows the output current vs. the input voltage. The differential input voltage, which varies from –3.2 V to +3.2 V, is plotted on the X-axis; the output current is plotted on the Y-axis. The four lines show the ideal current and the real outputs at –40°C, +25°C, and +85°C.

Figure 3 shows the output current error vs. the input voltage. The three lines show the error at –40°C, +25°C, and +85°C.

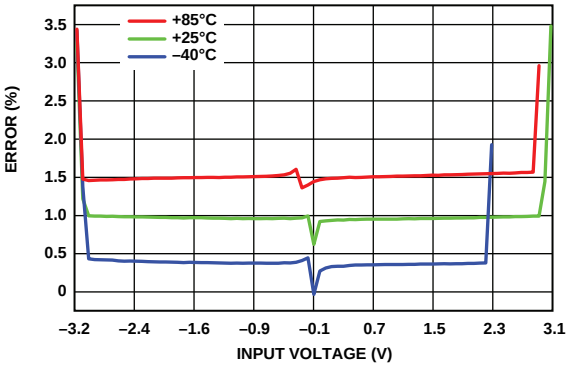

Figure 3. Output current error vs. input voltage.

The real output current is limited by the short-circuit output current of the AD8276, as shown in Figure 4. Here, the short-circuit current is about 8 mA at –40°C.

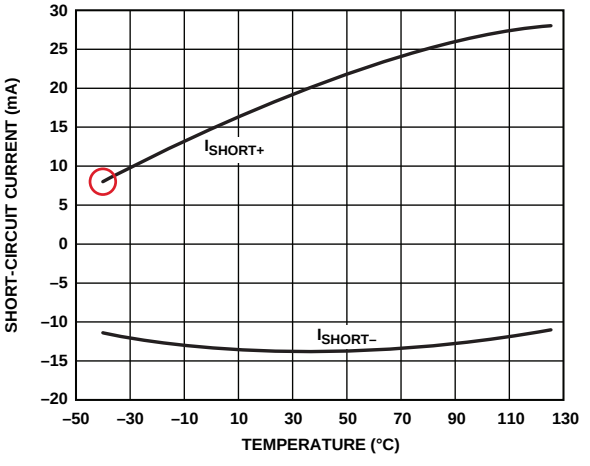

Figure 4. AD8276 short-circuit output current vs. temperature.

Conclusion

By removing the external boost transistor and buffer and adding a single resistor, one can use the AD8276 to construct a low-cost, low-current source with a total error less than about 1.5% over the –40°C to +85°C temperature range. The output current range over temperature is about –11 mA to +8 mA when powered with a ±15-V supply. A unipolar source could be created with a single +5 V supply.

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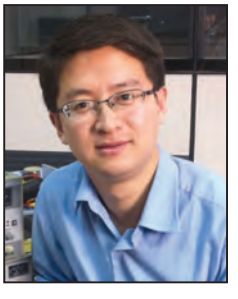

Ask The Applications Engineer—40

Switch and Multiplexer Design Considerations for Hostile Environments

By Michael Manning

Introduction

Hostile environments found in automotive, military, and avionic applications push integrated circuits to their technological limits, requiring them to withstand high voltage and current, extreme temperature and humidity, vibration, radiation, and a variety of other stresses. Systems engineers are rapidly adopting high-performance electronics to provide features and functions in application areas such as safety, entertainment, telematics, control, and human-machine interfaces. The increased use of precision electronics comes at the price of higher system complexity and greater vulnerability to electrical disturbances including overvoltages, latch-up conditions, and *electrostatic discharge* (ESD) events. Because electronic circuits used in these applications require high reliability and high tolerance to system faults, designers must consider both the environment and the limitations of the components that they choose.

In addition, manufacturers specify absolute maximum ratings for every integrated circuit; these ratings must be observed in order to maintain reliable operation and meet published specifications. When absolute maximum ratings are exceeded, operational parameters cannot be guaranteed; and even internal protections against ESD, overvoltage, or latch-up can fail, resulting in device (and potentially further) damage or failure.

This article describes challenges engineers face when designing analog switches and multiplexers into modules used in hostile environments and provides suggestions for general solutions that circuit designers can use to protect vulnerable parts. It also introduces some new integrated switches and multiplexers that provide increased overvoltage protection, latch-up immunity, and fault protection to deal with common stress conditions.

Standard Analog Switch Architecture

To fully understand the effects of fault conditions on an analog switch, we must first look at its internal structure and operational limits.

A standard CMOS switch (Figure 1) uses both N- and P-channel MOSFETs for the switch element, digital control logic, and driver circuitry. Connecting N- and P-channel MOSFETs in parallel permits bidirectional operation, allowing the analog input voltage to extend to the supply rails, while maintaining fairly constant on resistance over the signal range.

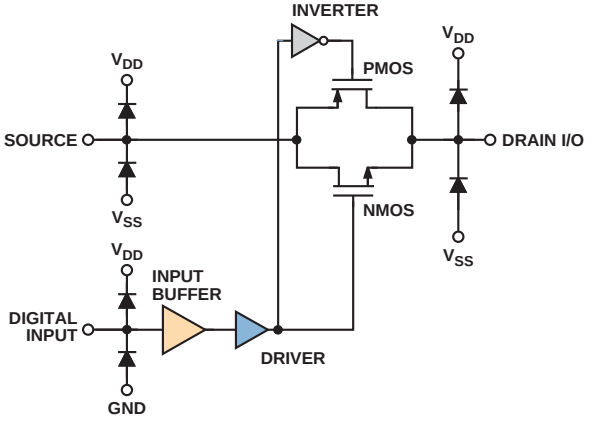

Figure 1. Standard analog switch circuitry.

The source, drain, and logic terminals include clamping diodes to the supplies to provide ESD protection, as illustrated in Figure 1. Reverse-biased in normal operation, the diodes do not pass current unless the signal exceeds the supply voltage. The diodes vary in size, depending on the process, but they are generally kept small to minimize leakage current in normal operation.

The analog switch is controlled as follows: the N-channel device is *on* for positive gate-to-source voltages and *off* for negative gate-to-source voltages; the P-channel device is switched by the complementary signal, so it is *on* at the same time as the N-channel device. The switch is turned *on* and *off* by driving the gates to opposite supply rails.

With a fixed voltage on the gate, the effective drive voltage for either transistor varies in proportion to the polarity and magnitude of the analog signal passing through the switch. The dashed lines in Figure 2 show that when the input signal approaches the supplies, the channel of one device or the other will begin to saturate, causing the on resistance of that device to increase sharply. The parallel devices compensate for one another in the vicinity of the rail voltages, however, so the result is a fully rail-to-rail switch, with relatively constant on resistance over the signal range.

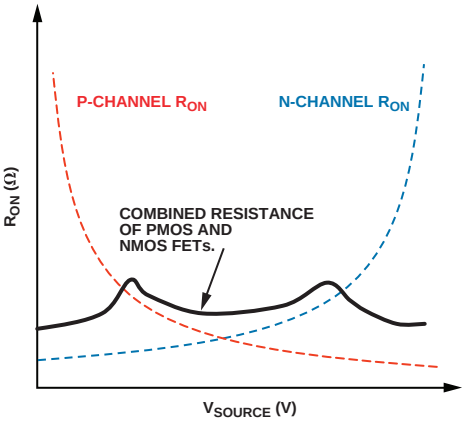

Figure 2. Standard analog switch R_{ON} graph.

Absolute Maximum Ratings

Switch power requirements, specified in the device data sheet, should be followed in order to guarantee optimal performance, operation, and lifetime. Unfortunately, power supply failures, voltage transients in harsh environments, and system or user faults that occur in the course of real-world operation may make it impossible to meet data sheet recommendations consistently.

Whenever an analog switch input voltage exceeds the supplies, the internal ESD protection diodes become forward-biased, allowing large currents to flow, even if the supplies are turned off, causing ratings to be exceeded. When forward-biased, the diodes are not rated to pass currents greater than a few tens of milliamperes; they can be damaged if this current is not limited. Furthermore, the damage caused by a fault is not limited to the switch but can also affect downstream circuitry.

The Absolute Maximum Ratings section of a data sheet (Figure 3) describes the maximum stress conditions a device can tolerate; it is important to note that these are *stress* ratings only. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. The designer should always follow good engineering practice by building margin into the design. The example here is from a standard switch/multiplexer data sheet.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Figure 3. Absolute Maximum Ratings section of a data sheet.

In this example, the V_{DD} to V_{SS} parameter is rated at 18 V. The rating is determined by the switch's manufacturing process and design architecture. Any voltage higher than 18 V must be completely isolated from the switch, or the intrinsic breakdown voltages of elements associated with the process will be exceeded, which may damage the device and lead to unreliable operation.

Voltage limitations that apply to the analog switch inputs—with and without power supplies—are often due to the ESD protection circuitry, which may fail as a result of fault conditions.

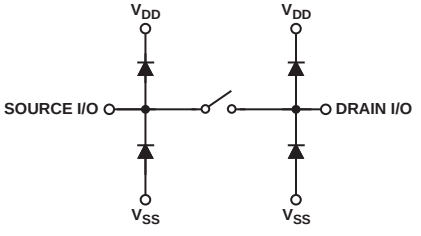

Figure 4. Analog switch—ESD protection diodes.

Analog and digital input voltage specifications are limited to 0.3 V beyond V_{DD} and V_{SS}, while digital input voltages are limited to 0.3 V beyond V_{DD} and ground. When the analog inputs exceed the supplies, the internal ESD protection diodes become forward-biased and begin to conduct. As stated in the Absolute Maximum Ratings section, overvoltages at IN, S, or D are clamped by internal diodes. While currents exceeding 30 mA can be passed through the internal diodes without any obvious effects, device reliability and lifetime may be reduced, and the effects of electromigration, the gradual displacement of metal atoms in a conductor, may be seen over time. As heavy current flows through a metal path, the moving electrons interact with metal ions in the conductor, forcing atoms to move with the flow of electrons. Over time this can lead to open- or short circuits.

When designing a switch into a system, it is important to consider potential faults that may occur in the system due to component failure, user error, or environmental effects. The next section will discuss how fault conditions that exceed the absolute maximum ratings of a standard analog switch can damage the switch or cause it to malfunction.

Common Fault Conditions, System Stresses, and Protection Methods

Fault conditions can occur for many different reasons; some of the most common system stresses and their real-world sources are shown in Table 1:

Table 1.

Fault Type	Fault Causes
Overvoltage:	• Loss of power • System malfunction • Hot-swap connects and disconnects • Power-supply sequencing issues • Miswiring • User error
Latch-Up:	• Overvoltage conditions (as listed above) • Exceeding process ratings • SEU (single-event upsets)
ESD	• Storage/assembly • PCB assembly • User operation

Some stress may not be preventable. Regardless of the source of the stress, the more important issue is how to deal with its effects. The questions and answers below cover these fault conditions: overvoltages, latch-up, and ESD events—and some common methods of protection.

OVERVOLTAGE

What Is an Overvoltage Condition?

Overvoltage conditions occur when analog or digital input conditions exceed the absolute maximum ratings. The following three examples highlight some common issues designers need to consider when using analog switches.

1. Loss of power with signals present on analog inputs (Figure 5).

In some applications, the power supply to a module is lost, while input signals from remote locations may still be present. When power is lost, the power supply rails may go to ground—or one or more may float. If the supplies go to ground, the input signals can forward-bias the internal diode, and current from the switch input will flow to ground—damaging the diode if the current is not limited.

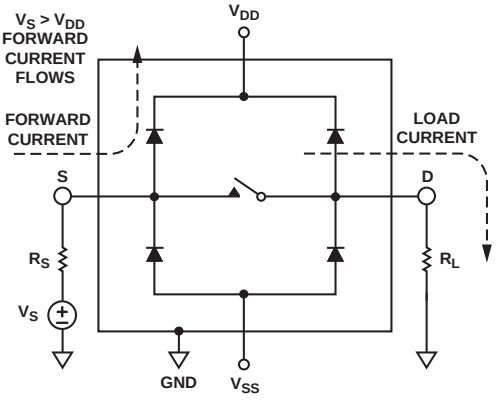

Figure 5. Fault paths.

If loss of power causes the supplies to float, the input signals can power the part through the internal diodes. As a result, the switch—and possibly any other components running from its V_{DD} supply—may be powered up.

2. Overvoltage conditions on analog inputs.

When analog signals exceed the power supplies (V_{DD} and V_{SS}), the supplies can be pulled to within a diode drop of the fault signal. Internal diodes become forward-biased and currents flow from the input signal to the supplies. The overvoltage signal can also pass through the switch and damage parts downstream. The explanation for this can be seen by considering the P-channel FET (Figure 6).

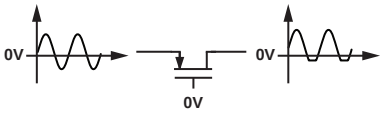

Figure 6. FET switch.

A P-channel FET requires a negative gate-to-source voltage to turn it on. With the switch gate equal to V_{DD}, the gate-to-source voltage is positive, so the switch is off. In an unpowered circuit, with the switch gate at 0 V or where the input signal exceeds V_{DD}, the signal will pass through the switch—as there is now a negative gate-to-source voltage.

3. Bipolar signals applied to a switch powered from a single supply.

This situation is similar to the previously described overvoltage condition. The fault occurs when the input signal goes below ground, causing the diode from the analog input to ground to forward-bias and current to flow. When an ac signal, biased at 0 V dc, is applied to the switch input, the parasitic diodes can be forward-biased for some portion of the negative half-cycle of the input waveform. This happens if the input sine wave goes below approximately –0.6 V, turning the diode on and clipping the input signal, as shown in Figure 7.

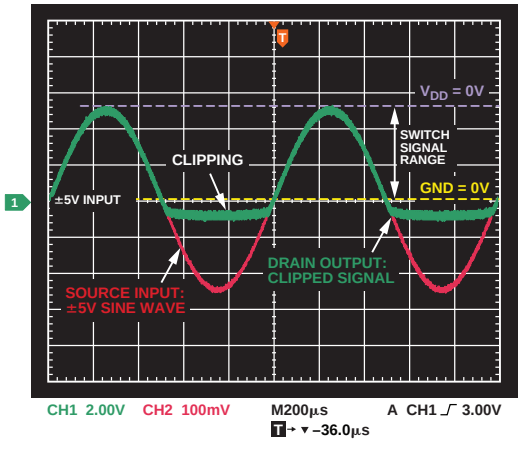

Figure 7. Clipping.

What's the Best Way to Deal with Overvoltage Conditions?

The three examples above are the results of analog inputs exceeding a supply—V_{DD}, V_{SS}, or GND. Simple protection methods to counter these conditions include the addition of external resistors, Schottky diodes to the supplies, and blocking diodes on the supplies.

Resistors, to limit current, are placed in series with any switch channel that is exposed to external sources (Figure 8). The resistance must be high enough to limit the current to approximately 30 mA (or as specified by the absolute maximum ratings). The obvious downside is the increase in R_{ON}, ΔR_{ON}, per channel, and ultimately the overall system error. Also, for applications using multiplexers, faults on the source of an off channel can appear at the drain, creating errors on other channels.

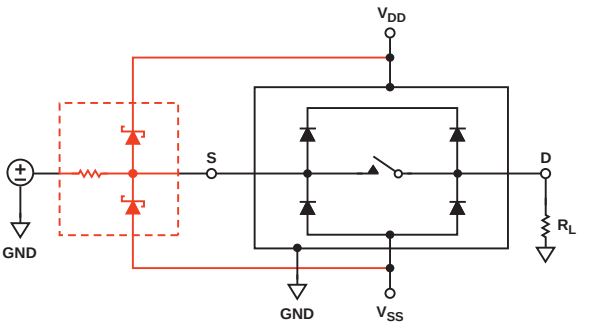

Figure 8. Resistor-diode protection network.

Schottky diodes connected from the analog inputs to the supplies provide protection, but at the expense of leakage and capacitance. The diodes work by preventing the input signal from exceeding the supply voltage by more than 0.3 V to 0.4 V, ensuring that the internal diodes do not forward bias and current does not flow. Diverting the current through the Schottky diodes protects the device, but care must be taken not to overstress the external components.

A third method of protection involves placing blocking diodes in series with the supplies (Figure 9), blocking current flow through the internal diodes. Faults on the inputs cause the supplies to float, and the most positive and negative input signals become the supplies. As long as the supplies do not exceed the absolute maximum ratings of the process, the device should tolerate the fault. The downside to this method is the reduced analog signal range due to the diodes on the supplies. Also, signals applied to the inputs may pass through the device and affect downstream circuitry.

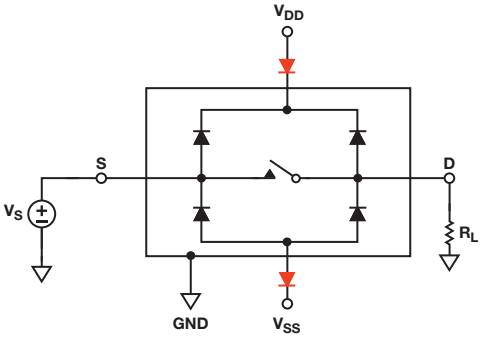

Figure 9. Blocking diodes in series with supplies.

While these protection methods have advantages and disadvantages, they all require external components, extra board area, and additional cost. This can be especially significant in applications with high channel count. To eliminate the need for external protection circuitry, designers should look for integrated protection solutions that can tolerate these faults. Analog Devices offers a number of switch/mux families with integrated protection against power off, overvoltage, and negative signals.

What Prepackaged Solutions Are Available?

The ADG4612 and ADG4613 from Analog Devices offer low on resistance and distortion, making them ideal for data acquisition systems requiring high accuracy. The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion.

The ADG4612 family offers power-off protection, overvoltage protection, and negative-signal handling, all conditions a standard CMOS switch cannot handle.

When no power supplies are present, the switch remains in the off condition. The switch inputs present a high impedance, limiting current flow that could damage the switch or downstream circuitry. This is very useful in applications where analog signals may be present at the switch inputs before the power is turned on, or where the user has no control over the power supply sequence. In the off condition, signal levels up to 16 V are blocked. Also, the switch turns off if the analog input signal level exceeds V_{DD} by V_T.

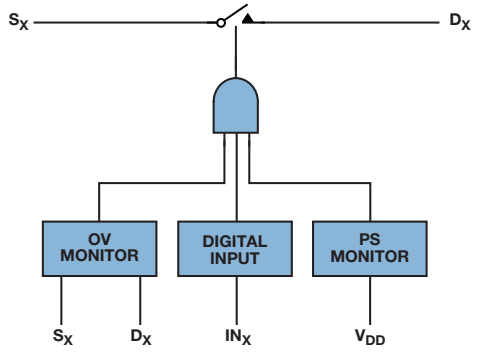

Figure 10. ADG4612/ADG4613 switch architecture.

Figure 10 shows a block diagram of the family's power-off protection architecture. Switch source- and drain inputs are constantly monitored and compared to the supply voltages, V_{DD} and V_{SS}. In normal operation the switch behaves as a standard CMOS switch with full rail-to-rail operation. However, during a fault condition where the source or drain input exceeds a supply by a threshold voltage, internal fault circuitry senses the overvoltage condition and puts the switch in isolation mode.

Analog Devices also offers multiplexers and channel protectors that can tolerate overvoltage conditions of +40 V/–25 V beyond the supplies with power (±15 V) applied to the device, and +55 V/–40 V unpowered. These devices are specifically designed to handle faults caused by power-off conditions.

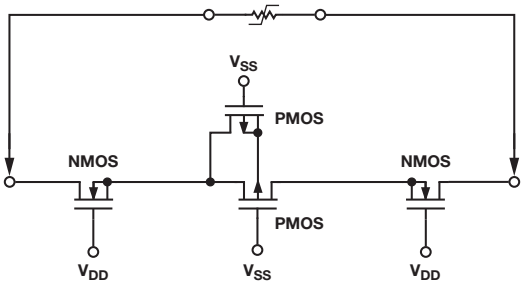

Figure 11. High-voltage fault-protected switch architecture.

These devices comprise N-channel, P-channel, and N-channel MOSFETs in series, as illustrated in Figure 11. When one of the analog inputs or outputs exceeds the power supplies, one of the MOSFETs switches off, the multiplexer input (or output) appears as an open circuit, and the output is clamped to within the supply rail, thereby preventing the overvoltage from damaging any circuitry following the multiplexer. This protects the multiplexer, the circuitry it drives, and the sensors or signal sources that drive the multiplexer. When the power supplies are lost (through, for example, battery disconnection or power failure) or momentarily disconnected (rack system, for example), all transistors are off and the current is limited to subnanoampere levels. The ADG508F, ADG509F, and ADG528F include 8:1 and differential 4:1 multiplexers with such functionality.

The ADG465 single- and ADG467 octal channel protectors have the same protective architecture as these fault-protected multiplexers, without the switch function. When powered, the channel is always in the on condition, but in the event of a fault, the output is clamped to within the supply voltages.

LATCH-UP

What Is a Latch-Up Condition?

Latch-up may be defined as the creation of a low-impedance path between power supply rails as a result of triggering a parasitic device. Latch-up occurs in CMOS devices: intrinsic parasitic devices form a PNPN SCR structure when one of the two parasitic base-emitter junctions is momentarily forward-biased (Figure 12). The SCR turns on, causing a continuing short between the supplies. Triggering a latch-up condition is serious: in the "best" case, it leads to device malfunction, with power cycling required to restore the device to normal operation; in the worst case, the device (and possibly power supply) can be destroyed if current flow is not limited.

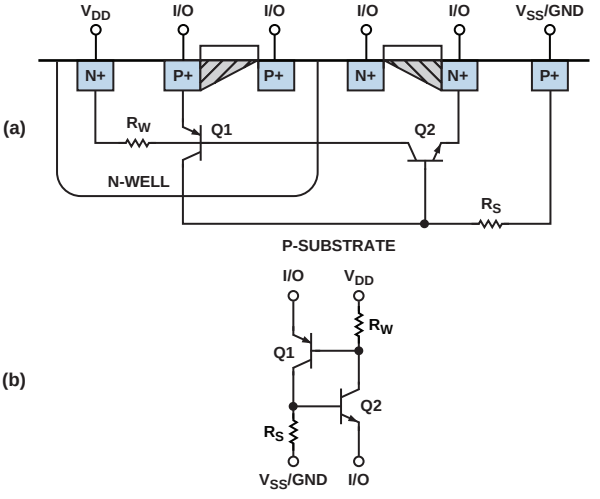

Figure 12. Parasitic SCR structure: a) device b) equivalent circuit.

The fault and overvoltage conditions described earlier are among the common causes of triggering a latch-up condition. If signals on the analog or digital inputs exceed the supplies, a parasitic transistor is turned on. The collector current of this transistor causes a voltage drop across the base emitter of a second parasitic transistor, which turns the transistor on, and results in a self-sustaining path between the supplies. Figure 12(b) clearly shows the SCR circuit structure formed between Q1 and Q2.

Events need not last long to trigger latch-up. Short-lived transients, spikes, or ESD events may be enough to cause a device to enter a latch-up state.

Latch-up can also occur when the supply voltages are stressed beyond the absolute maximum ratings of the device, causing internal junctions to break down and the SCR to trigger.

The second triggering mechanism occurs if a supply voltage is raised enough to break down an internal junction, injecting current into the SCR.

What's the Best Way to Deal with Latch-Up Conditions?

Protection methods against latch-up include the same protection methods recommended to address overvoltage conditions. Adding current-limiting resistors in the signal path, Schottky

diodes to the supplies, and diodes in series with the supplies—as illustrated in Figure 8 and Figure 9—all help to prevent current from flowing in the parasitic transistors, thereby preventing the SCR from triggering.

Switches with multiple supplies may have additional power-supply sequencing issues that may violate the absolute maximum ratings. Improper supply sequencing can lead to internal diodes turning on and triggering latch-up. External Schottky diodes, connected between supplies, will adequately prevent SCR conduction by ensuring that when multiple supplies are applied to the switch, V_{DD} is always within a diode drop (0.3 V for Schottky) of these supplies, thereby preventing violation of the maximum ratings.

What Prepackaged Solutions Are Available?

As an alternative to using external protection, some ICs are manufactured using a process with an epitaxial layer, which increases the substrate- and N-well resistances in the SCR structure. The higher resistance means that a harsher stress is required to trigger the SCR, resulting in a device that is less susceptible to latch-up. An example is the Analog Devices *i*CMOS® process, which made possible the ADG121x, ADG141x, and ADG161x switch/mux families.

For applications requiring a latch-up proof solution, new trench-isolated switches and multiplexers guarantee latch-up prevention in high-voltage industrial applications operating at up to ±20 V. The ADG541x and ADG521x families are designed for instrumentation, automotive, avionics, and other harsh environments that are likely to foster latch-up. The process uses an insulating oxide layer (trench) placed between the N-channel and the P-channel transistors of each CMOS switch. The oxide layers, both horizontal and vertical, produce complete isolation between devices. Parasitic junctions between transistors in junction-isolated switches are eliminated, resulting in a completely latch-up proof switch.

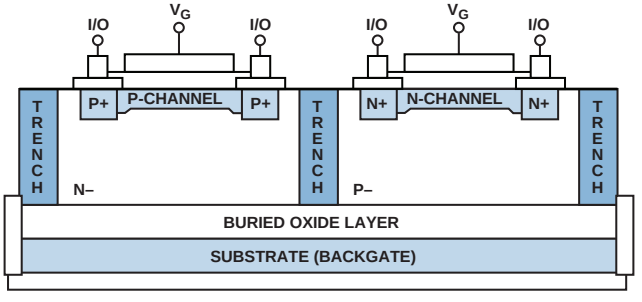

Figure 13. Trench isolation in latch-up prevention.

The industry practice is to classify the susceptibility of inputs and outputs to latch-up in terms of the amount of excess current an I/O pin can source or sink in the overvoltage condition before the internal parasitic resistances develop enough voltage drop to sustain the latch-up condition.

A value of 100 mA is generally considered adequate. Devices in the ADG5412 latch-up proof family were stressed to ±500 mA with a 1-ms pulse without failure. Latch-up testing at Analog Devices is performed according to EIA/JEDEC-78 (IC Latch-Up Test).

ESD—ELECTROSTATIC DISCHARGE

What Is an Electrostatic Discharge Event?

Typically the most common type of voltage transient that a device is exposed to, ESD, can be defined as a *single, fast, high-current transfer of electrostatic charge between two objects at different electrostatic potentials*. We frequently experience this after walking across an insulating surface, such as a rug, storing a charge, and then touching an earthed piece of equipment—resulting in a discharge through the equipment, with high currents flowing in a short space of time.

ICs can be damaged by the high voltages and high peak currents generated by an ESD event. The effects of an ESD event on an analog switch can include reduced reliability over time, the degradation of switch performance, increased channel leakage, or complete device failure.

ESD events can occur at any stage of the life of an IC, from manufacturing through testing, handling, OEM user, and end-user operation. In order to evaluate an IC's robustness to various ESD events, electrical pulse circuits modeling the following simulated stress environments were identified: *human body model* (HBM), *field-induced charged device model* (FICDM), and *machine model* (MM).

What's the Best Way to Deal with ESD Events?

ESD prevention methods, such as maintaining a static-safe work area, are used to avoid any build up during production, assembly, and storage. These environments, and the individuals working in them, can generally be carefully controlled, but the environments in which the device later finds itself may be anything but controlled.

Analog switch ESD protection is generally in the form of diodes from the analog and digital inputs to the supplies, as well as power supply protection in the form of diodes between the supplies—as illustrated in Figure 14.

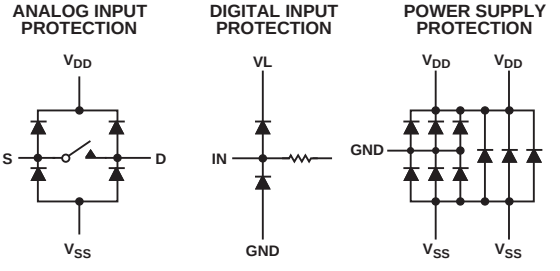

Figure 14. Analog switch ESD protection.

The protection diodes clamp voltage transients and divert current to the supplies. The downside of these protection devices is that they add capacitance and leakage to the signal path in normal operation, which may be undesirable in some applications.

For applications that require greater protection against ESD events, discrete components such as Zener diodes, metal-oxide varistors (MOVs), transient voltage suppressors (TVS), and diodes are commonly used. However, they can lead to signal integrity issues due to the extra capacitance and leakage on the signal line; this means design engineers need to carefully consider the trade-off between performance and reliability.

What Prepackaged Solutions Are Available?

While the vast majority of ADI switch/mux products meet HBM levels of at least ±2 kV, others go beyond this in robustness, achieving HBM ratings of up to ±8 kV. ADG541x family members have achieved a ±8-kV HBM rating, a ±1.5-kV FICDM rating, and a ±400-V MM rating, making them industry leaders, combining high-voltage performance and robustness.

Conclusion

When switch or multiplexer inputs come from remotely located sources, there is an increased likelihood that faults can occur. Overvoltage conditions may occur due to systems with poorly designed power-supply sequencing or where hot-plug insertion is a requirement. In harsh electrical environments, transient voltages due to poor connections or inductive coupling may damage components if not protected. Faults can also occur due to power-supply failures where power connections are lost while switch inputs remain exposed to analog signals. Significant damage may result from these fault conditions, possibly causing damage and requiring expensive repairs. While a number of protective design techniques are used to deal with faults, they add extra cost and board area and often require a trade-off in switch performance; and even with external protection implemented, downstream circuitry is not always protected. Since analog switches and multiplexers are often a module's most likely electronic components to be subjected to a fault, it is important to understand how they behave when exposed to conditions that exceed the absolute maximum ratings.

Switch/mux products, like devices mentioned here, are available with integrated protection, allowing designers to eliminate external protection circuitry, reducing the number and cost of components in board designs. Savings are even more significant in applications with high channel count.

Ultimately, using switches with fault protection, overvoltage protection, immunity to latch-up, and a high ESD rating yields a robust product that meets industry regulations and enhances customer and end-user satisfaction.

Author

Michael Manning [michael.manning@analog.com] graduated from National University of Ireland, Galway, with a BSc in applied physics and electronics. In 2006, he joined Analog Devices as an applications engineer in the switch/multiplexer group in Limerick, Ireland. Previously, Michael spent five years as a design and applications engineer in the automotive division at ALPS Electric in Japan and Sweden.

APPENDIX
ANALOG DEVICES SWITCH/MULTIPLEXER PROTECTION PRODUCTS:

High-Voltage Latch-Up Proof Switches

Part Number	Configuration	Number of Switch Functions	R_{ON} (Ω)	Max Analog Signal Range	Charge Injection (pC)	On Leakage @ 85°C (nA)	Supply Voltages	Packages	Price @ 1k ($U.S.)
ADG5212	SPST/NO	4	160	V_{SS} to V_{DD}	0.07	0.25	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.18
ADG5213	SPST/ NO-NC	4	160	V_{SS} to V_{DD}	0.07	0.25	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.18
ADG5236	SPST/ NO-NC	2	160	V_{SS} to V_{DD}	0.6	0.4	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.26
ADG5412	SPST/NO	4	9	V_{SS} to V_{DD}	240	2	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.18
ADG5413	SPST/NO-NC	4	9	V_{SS} to V_{DD}	240	2	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.18
ADG5433	SPST/NO-NC	3	12.5	V_{SS} to V_{DD}	130	4	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.15
ADG5434	SPST/NO-NC	4	12.5	V_{SS} to V_{DD}	130	4	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	SOP	3.04
ADG5436	SPST/NO-NC	2	9	V_{SS} to V_{DD}	0.6	2	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.26

High-Voltage Latch-Up Proof Multiplexers

Part Number	Configuration	R_{ON} (Ω)	Max Analog Signal Range	Charge Injection (pC)	On Capacitance (pF)	On Leakage @ 85°C (nA)	Supply Voltages	Packages	Price @ 1000 to 4999 ($U.S.)
ADG5204	(4:1) × 2	160	V_{SS} to V_{DD}	0.6	30	0.5	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.26
ADG5408	(8:1) × 1	14.5	V_{SS} to V_{DD}	115	133	4	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.41
ADG5409	(4:1) × 2	12.5	V_{SS} to V_{DD}	115	81	4	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.41
ADG5404	(4:1) × 1	9	V_{SS} to V_{DD}	220	132	2	Dual (±15 V), Dual (±20 V), Single (+12 V), Single (+36 V)	CSP, SOP	2.26

Low-Voltage Fault-Protected Multiplexers

Part Number	Configuration	Number of Switch Functions	Max Analog Signal Range	Fault Response Time (ns)	Fault Recovery Time (µs)	–3 dB Bandwidth (MHz)	Packages	Price @ 1k ($U.S.)
ADG4612	SPST/NO	4	–5.5 V to V_{DD}	295	1.2	293	SOP	1.84
ADG4613	SPT/NO-NC	4	–5.5 V to V_{DD}	295	1.2	294	CSP, SOP	1.84

High-Voltage Fault-Protected Multiplexers

Part Number	Switch/ Mux Function x #	R_{ON} (Ω)	Max Analog Signal Range	$t_{TRANSITION}$ (ns)	Supply Voltages (V)	Power Dissipation (mW)	Packages	Price @ 1000 to 4999 ($U.S.)
ADG438F	(8:1) × 1	400	V_{SS} + 1.2 V to V_{DD} – 0.8 V	170	Dual (±15 V)	2.6	DIP, SOIC	3.68
ADG439F	(4:1) × 2	400	V_{SS} + 1.2 V to V_{DD} – 0.8 V	170	Dual (±15 V)	2.6	DIP, SOIC	3.68
ADG508F	(8:1) × 1	300	V_{SS} + 3 V to V_{DD} – 1.5 V	200	Dual (±12 V), Dual (±15 V)	3	DIP, SOIC	3.31
ADG509F	(4:1) × 2	300	V_{SS} + 3 V to V_{DD} – 1.5 V	200	Dual (±12 V), Dual (±15 V)	3	DIP, SOIC	3.31
ADG528F	(8:1) × 1	300	V_{SS} + 3 V to V_{DD} – 1.5 V	200	Dual (±12 V), Dual (±15 V)	3	DIP, LCC	3.91

High-Voltage Channel Protectors

Part Number	Configuration	Number of Switch Functions	R_{ON} (Ω)	Max Positive Supply (V)	Max Negative Supply (V)	Packages	Price @ 1k ($U.S.)
ADG465	Channel Protector	1	80	20	20	SOIC, SOT	0.84
ADG467	Channel Protector	8	62	20	20	SOIC, SOP	2.40

High-Resolution Temperature Measurement

By Moshe Gerstenhaber and Michael O'Sullivan

The AD8494 thermocouple amplifier includes an on-chip temperature sensor, normally used for cold-junction compensation, allowing the device to be used as a standalone Celsius thermometer by grounding the thermocouple inputs. In this configuration, the amplifier produces a 5-mV/°C output voltage between the output and (the normally grounded) reference pins of the on-chip instrumentation amplifier. One drawback of this approach is the poor system resolution achieved when measuring narrow temperature ranges. Consider this: a 10-bit ADC running on a single 5-V supply has 4.88-mV/LSB resolution. This means that the system shown in Figure 1 has a resolution of about 1°C/LSB. If the temperature range of interest is narrow, say 20°C, the output varies by 100 mV, utilizing only 1/50 of the ADC's available dynamic range.

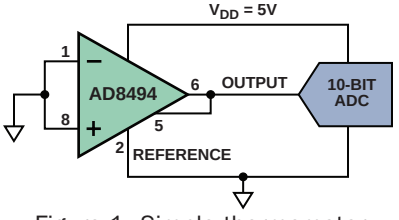

Figure 1. Simple thermometer.

The circuit shown in Figure 2 solves this problem. As before, the amplifier produces a 5 mV/°C voltage between the output and reference pins of the instrumentation amplifier. Now, however, the reference pin is driven by the AD8538 operational amplifier (configured as a unity-gain follower), so the 5-mV/°C voltage appears across R1. The current flowing through R1 also flows through R2, generating a temperature-sensitive voltage across the series combination that is $(R1 + R2)/R1$ times the voltage across R1. With the values shown, the output voltage varies at 20 × 5 mV/°C = 100 mV/°C, so a 20°C temperature change produces a 2-V output voltage change. The new 0.05°C/LSB system resolution is a 20:1 improvement over the original circuit. The AD8538 buffers the resistor network, driving the reference pin with a low impedance in order to maintain good common-mode rejection and gain accuracy.

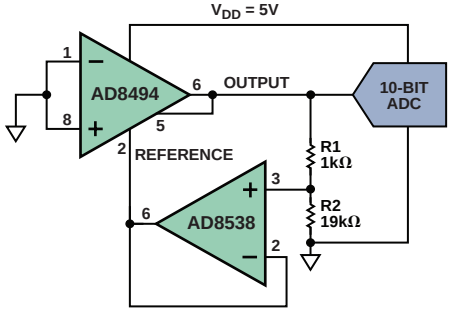

Figure 2. High-resolution temperature measurement.

Care must be taken to match the system sensitivity to the desired temperature range. For example, the output voltage is 2.5 V at 25°C, so the system can accurately measure from 5°C to 45°C as the output voltage varies from 0.5 V to 4.5 V.

A circuit such as the one shown in Figure 3 offers higher sensitivity and customizable temperature ranges. The resistance divider formed by R3 and R4 simulates the thermocouple voltage required to offset the amplifier, zeroing its output voltage at the desired level. If V_{DD} is noisy, a precision voltage reference and divider circuit could be used to provide a quieter, more accurate offset adjustment. As shown, the circuit has an output voltage of about 0.05 V at 25°C, 100 mV/°C sensitivity (0.05°C/LSB resolution), and an operational range of approximately 25°C to 75°C.

The AD8494 has an initial offset error of ±1°C to ±3°C, so the user must include an offset calibration to improve absolute accuracy.

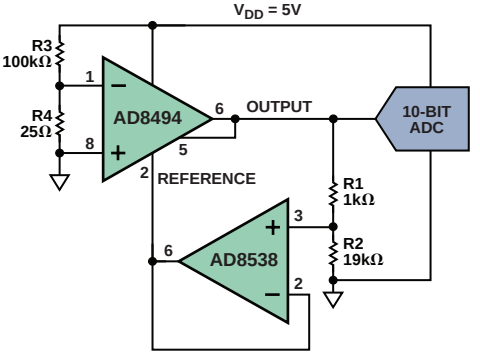

Figure 3. Higher resolution temperature measurement with offset adjustment.

Authors

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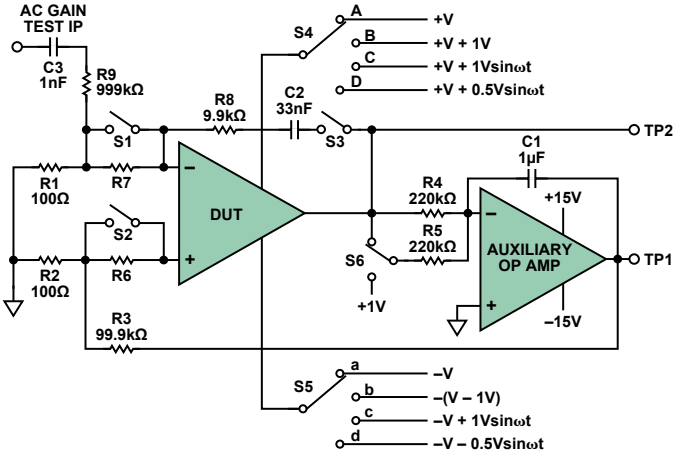
Michael O'Sullivan [michael-a.osullivan@analog.com] has worked at Analog Devices since 2004. Currently the product and test engineering manager of the Integrated Amplifier Products Group, he supports product characterization and release of very-high-precision specialty amplifiers such as instrumentation and difference amplifiers. Previously, Mike worked as a product engineer in the semiconductor field for over 14 years.

Simple Op Amp Measurements

By James M. Bryant

Op amps are very high gain amplifiers with differential inputs and single-ended outputs. They are often used in high precision analog circuits, so it is important to measure their performance accurately. But in open-loop measurements their high open-loop gain, which may be as great as 10^7 or more, makes it very hard to avoid errors from very small voltages at the amplifier input due to pickup, stray currents, or the Seebeck (thermocouple) effect.

The measurement process can be greatly simplified by using a servo loop to force a null at the amplifier input, thus allowing the amplifier under test to essentially measure its own errors. Figure 1 shows a versatile circuit that uses this principle, employing an auxiliary op amp as an integrator to establish a stable loop with very high dc open-loop gain. The switches facilitate performance of the various tests described in the simplified illustrations that follow.



SWITCH POSITIONS

FIGURE	S1	S2	S3	S4	S5	S6
2	1	1	0	A	a	0
3	0/1	0/1	0	A	a	0
4	1	1	0	A	a	0/1
5	1	1	0	A	a	0
6	1	1	0	A/B	a/b	0
7	1	1	0	A/B	a/b	0
8	1	1	1	C	c	0
9	1	1	1	D	d	0

Figure 1. Basic op amp measurement circuit.

The circuit of Figure 1 minimizes most of the measurement errors and permits accurate measurements of a large number of dc—and a few ac—parameters. The additional "auxiliary" op amp does not need better performance than the op amp being measured. It is helpful if it has dc open-loop gain of one million or more; if the offset of the device under test (DUT) is likely to exceed a few mV, the auxiliary op amp should be operated from ±15-V supplies (and if the DUT's input offset can exceed 10 mV, the 99.9-kΩ resistor, R3, will need to be reduced).

The supply voltages, +V and –V, of the DUT are of equal magnitude and opposite sign. The total supply voltage is, of course, 2 × V. Symmetrical supplies are used, even with "single supply" op amps, with this circuit, as the system ground reference is the midpoint of the supplies.

The auxiliary amplifier, as an integrator, is configured to be open-loop (full gain) at dc, but its input resistor and feedback capacitor limit its bandwidth to a few Hz. This means that the dc voltage at the output of the DUT is amplified by the full gain of the auxiliary amplifier and applied, via a 1000:1 attenuator, to the noninverting input of the DUT. Negative feedback forces the output of the DUT to ground potential. (In fact, the actual voltage is the offset voltage of the auxiliary amplifier—or, if we are to be really meticulous, this offset plus the voltage drop in the 100-kΩ resistor due to the auxiliary amplifier's bias current—but this is close enough to ground to be unimportant, particularly as the changes in this point's voltage during measurements are unlikely to exceed a few microvolts).

The voltage on the test point, TP1, is 1000 times the correction voltage (equal in magnitude to the error) being applied to the input of the DUT. This will be tens of mV or more and, so, quite easy to measure.

An ideal op amp has zero offset voltage (V_{OS}); that is, if both inputs are joined together and held at a voltage midway between the supplies, the output voltage should also be midway between the supplies. In real life, op amps have offsets ranging from a few microvolts to a few millivolts—so a voltage in this range must be applied to the input to bring the output to the midway potential.

Figure 2 shows the configuration for the most basic test—offset measurement. The DUT output voltage is at ground when the voltage on TP1 is 1000 times its offset.

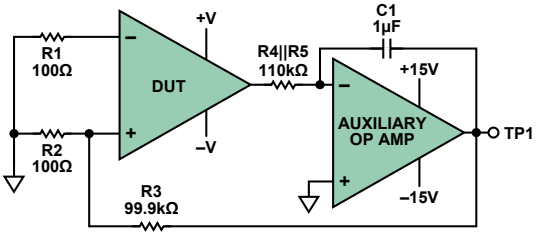


Figure 2. Offset measurement.

The ideal op amp has infinite input impedance and no current flows in its inputs. In reality, small "bias" currents flow in the inverting and noninverting inputs (I_{B-} and I_{B+}, respectively); they can cause significant offsets in high-impedance circuits. They can range, depending on the op amp type, from a few femtoamperes (1 fA = 10^{-15} A—one electron every few microseconds) to a few nanoamperes, or even—in some very fast op amps—one or two microamperes. Figure 3 shows how these currents can be measured.

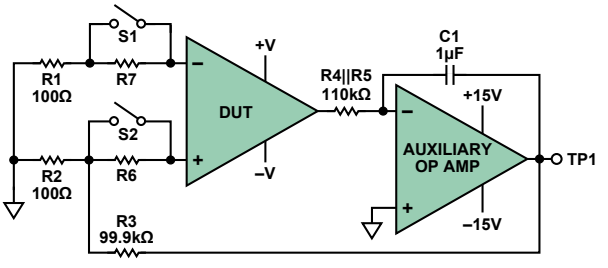


Figure 3. Offset and bias current measurement.

The circuit is the same as the offset circuit of Figure 2, with the addition of two resistors, R6 and R7, in series with the DUT inputs. These resistors can be short circuited by switches S1 and S2. With both switches closed, the circuit is the same as Figure 2. When S1 is open, the bias current from the inverting input flows in R_S, and the voltage difference adds to the offset. By measuring the change of voltage at TP1 (= 1000 I_{B-}/R_S), we can calculate I_{B-}; similarly, by closing S1 and opening S2 we can measure I_{B+}. If the voltage is measured at TP1 with S1 and S2 both closed, and then both open, the "input offset current," I_{OS}, the difference between I_{B+} and I_{B-}, is measured by the change. The values of R6 and R7 used will depend on the currents to be measured.

For values of I_B of the order of 5 pA or less, it becomes quite difficult to use this circuit because of the large resistors involved; other techniques may be required, probably involving the rate at which I_B charges low-leakage capacitors (that replace R_S).

When S1 and S2 are closed, I_{OS} still flows in the 100-Ω resistors and introduces an error in V_{OS}, but unless I_{OS} is large enough to produce an error of greater than 1% of the measured V_{OS}, it may usually be ignored in this calculation.

The open-loop dc gain of an op amp can be very high; gains greater than 10^7 are not unknown, but values between 250,000 and 2,000,000 are more usual. The dc gain is measured by forcing the output of the DUT to move by a known amount (1 V in Figure 4, but 10 V if the device is running on large enough supplies to allow this) by switching R5 between the DUT output and a 1-V reference with S6. If R5 is at +1 V, then the DUT output must move to –1 V if the input of the auxiliary amplifier is to remain unchanged near zero.

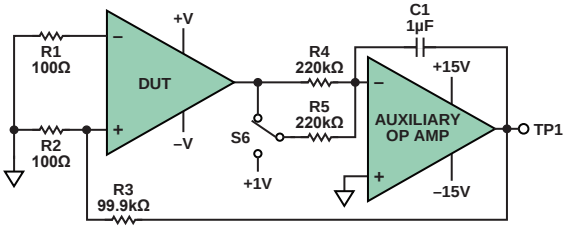


Figure 4. DC gain measurement.

The voltage change at TP1, attenuated by 1000:1, is the input to the DUT, which causes a 1-V change of output. It is simple to calculate the gain from this (= 1000 × 1 V/TP1).

To measure the open-loop ac gain, it is necessary to inject a small ac signal of the desired frequency at the DUT input and measure the resulting signal at its output (TP2 in Figure 5). While this is being done, the auxiliary amplifier continues to stabilize the mean dc level at the DUT output.

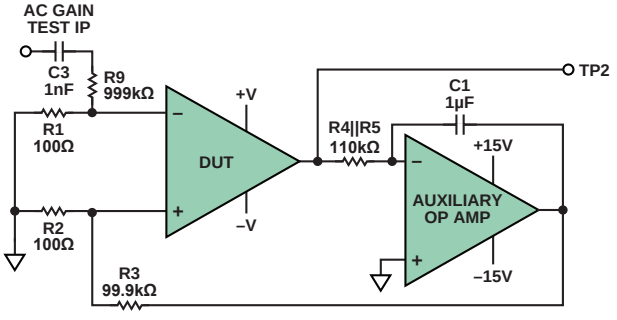


Figure 5. AC gain measurement.

In Figure 5, the ac signal is applied to the DUT input via a 10,000:1 attenuator. This large value is needed for low-frequency measurements, where open-loop gains may be near the dc value. (For example, at a frequency where the gain is 1,000,000, a 1-V rms signal would apply 100 µV at the amplifier input, which would saturate the amplifier as it seeks to deliver 100-V rms output). So ac measurements are normally made at frequencies from a few hundred Hz to the frequency at which the open-loop gain has dropped to unity—or very carefully with lower input amplitudes if low-frequency gain data is needed. The simple attenuator shown will only work at frequencies up to 100 kHz or so, even if great care is taken with stray capacitance; at higher frequencies a more complex circuit would be needed.

The *common-mode rejection ratio* (CMRR) of an op amp is the ratio of apparent change of offset resulting from a change of common-mode voltage to the applied change of common-mode voltage. It is often of the order of 80 dB to 120 dB at dc, but lower at higher frequencies.

The test circuit is ideally suited to measuring CMRR (Figure 6). The common-mode voltage is not applied to the DUT input terminals, where low-level effects would be likely to disrupt the measurement, but the *power-supply* voltages are altered (in the *same*—that is, common—direction, relative to the input), while the remainder of the circuit is left undisturbed.

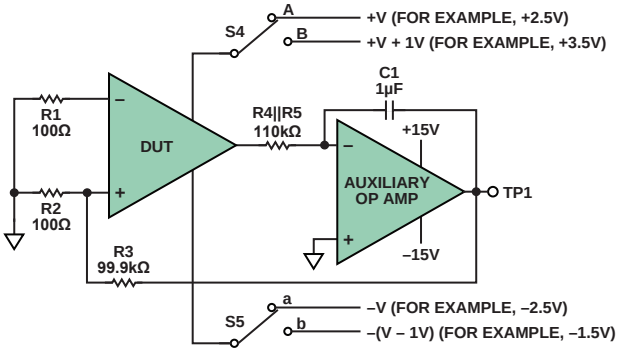


Figure 6. DC CMRR measurement.

In the circuit of Figure 6, the offset is measured at TP1 with supplies of ±V (in the example, +2.5 V and –2.5 V) and again with both supplies moved up by +1 V to +3.5 V and –1.5 V. The change of offset corresponds to a change of common mode of 1 V, so the dc CMRR is the ratio of the offset change and 1 V.

CMRR refers to change of offset for a change of common mode, the total power supply voltage being unchanged. The *power-supply rejection ratio* (PSRR), on the other hand, is the ratio of the change of offset to the change of total power supply voltage, with the common-mode voltage being unchanged at the midpoint of the supply (Figure 7).

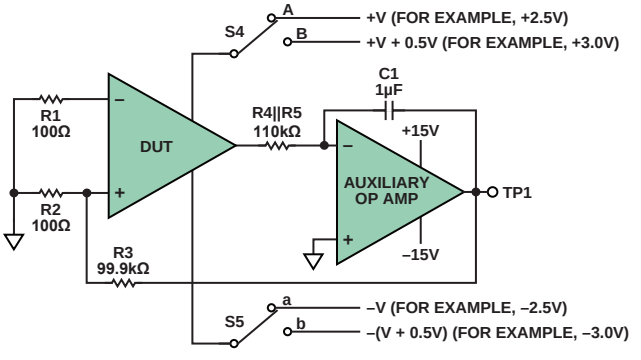


Figure 7. DC PSRR measurement.

The circuit used is exactly the same; the difference is that the *total* supply voltage is changed, while the common level is unchanged. Here the switch is from +2.5 V and –2.5 V to +3 V and –3 V, a change of total supply voltage from 5 V to 6 V. The common-mode voltage remains at the midpoint. The calculation is the same, too (1000 × TP1/1 V).

To measure ac CMRR and PSRR, the supply voltages are modulated with voltages, as shown in Figure 8 and Figure 9. The DUT continues to operate open-loop at dc, but ac negative feedback defines an exact gain (×100 in the diagrams).

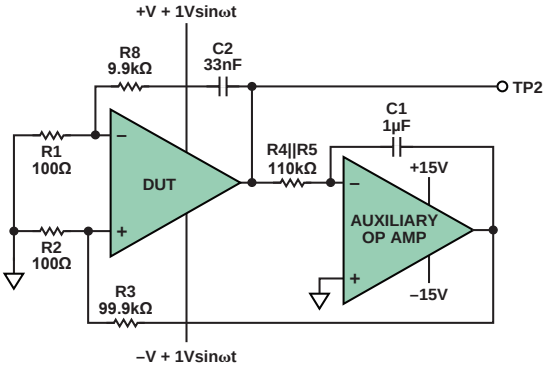


Figure 8. AC CMRR measurement.

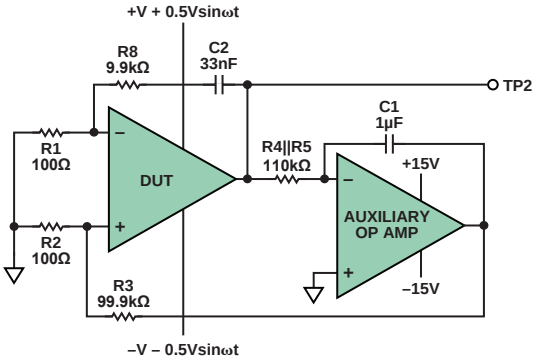


Figure 9. AC PSRR measurement.

To measure ac CMRR, the positive and negative supplies to the DUT are modulated with ac voltages with amplitude of 1-V peak. The modulation of both supplies is the same phase, so that the actual supply voltage is steady dc, but the common-mode voltage is a sine wave of 2 V p-p, which causes the DUT output to contain an ac voltage, which is measured at TP2.

If the ac voltage at TP2 has an amplitude of x volts peak ($2x$ volts peak-to-peak), then the CMRR, referred to the DUT input (that is, before the ×100 ac gain) is $x/100$ V, and the CMRR is the ratio of this to 1 V peak.

AC PSRR is measured with the ac on the positive and negative supplies 180° out of phase. This results in the amplitude of the supply voltage being modulated (again, in the example, with 1 V peak, 2 V p-p) while the common-mode voltage remains steady at dc. The calculation is very similar to the previous one.

Conclusion

There are, of course, many other op amp parameters which may need to be measured, and a number of other ways of measuring the ones we have discussed, but the most basic dc and ac parameters can, as we have seen, be measured reliably with a simple basic circuit that is easily constructed, easily understood, and remarkably free from problems.

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