Analog Dialogue

Volume 42, Number 2, 2008 | A forum for the exchange of circuits, systems, and software for real-world signal processing

In This Issue

Analog Dialogue Since 1967

www.analog.com/analogdialogue

ANALOG DEVICES

Editors' Notes

HD Digital Radio

Everyone has heard of high-definition television (HDTV), and millions of viewers have experienced the vivid picture and lifelike sound in a consumer electronics store, sports bar, or friend's house—if not in their own home theater. On the other hand, it's uncommon to find someone who has heard of HD radio, and rare to find someone who has actually listened to one.

HD Digital Radio,[1] an upgrade to standard analog AM/FM radio, provides FM-quality sound from AM stations and CD-quality sound from FM stations, all without the hiss, static, and fading commonly experienced with standard radio broadcasts. In addition, HD digital radio includes a text channel that can identify songs and artists in real time, or provide enhanced data services such as news updates, sports scores, or weather forecasts. HD digital radio also enables stations to use multicast channels to broadcast multiple programming options. According to trademark holder iBiquity Digital Corporation,[2] the HD in HD Radio does not stand for high definition or hybrid digital, but is part of their brand for digital radio technology.

HD radio stations bundle analog audio with compressed digital audio and textual data, allowing the received signal to be compatible with both analog and HD radios. Using digital in-band on-channel (IBOC)[3] technology, the HD radio signal occupies the same radio spectrum as standard radio broadcasts. Digital signals are broadcast as upper and lower sidebands around the analog channel, making optimum use of the available radio spectrum. The two sidebands contain redundant information. The two signals can be combined to provide additional gain, or the stronger signal can be used to minimize adjacent channel and multipath interference. The digital signal is cached to avoid momentary interruptions.

Being a bit of a gadget hound, I ordered an HD radio to try it out. Just after it arrived, our admin announced that she was leaving ADI to rejoin her family in the Midwest. The radio became a going away gift, forcing me to wait patiently for a second one to arrive. The second radio came with three FM antennas: a short wire, a telescoping metal whip, and a longer wire dipole. Initial performance was disappointing; the short wire was useless at my home in the Boston suburbs and the whip received only a few strong HD signals. The dipole worked great, however, allowing reception of more than thirty HD channels. The first thing that I noticed was that the HD signal was "brighter" than the analog signal, with better high-frequency performance and better stereo imaging. My second observation was the complete lack of hiss and background noise.

The thing that made me fall in love with my HD radio, however, was the HD-2 multicast channels. Currently commercial free, these stations compete with satellite radio, but require no subscriptions or other fees. In Boston we're lucky to have several genres, including rock, jazz, classical, country, and folk—all digital and all commercial free.

Readers: What are your experiences with analog, satellite, or HD radio? Your comments are welcome.

Scott Wayne [scott.wayne@analog.com]

[1]www.hdradio.com
[2]www.ibiquity.com
[3]www.ibiquity.com/hd_radio/iboc_white_papers

IN THIS ISSUE

The Wit and Wisdom of Dr. Leif—6. From the recently discovered archives of Dr. Leif, Niku Chen has recovered a piece entitled, "Noise Figure and Logarithmic Amplifiers." Log amps are uniquely equipped as RF measurement elements at frequencies from near-dc to beyond 10 GHz because of their wide dynamic range, temperature stability, excellent log conformance, and ease of use—with measurements provided directly in decibels. *Noise figure* is a valuable metric when log amps are used in the signal path, as it indicates the system's ability to extract information in the presence of noise. Despite the antiquity of this document, there is much that is fresh even now, late in the third decade of the 21st century. Read it on page 3.

"Hot Swap," always a useful confidence factor for anyone contemplating the insertion of a module into a hot socket, is a *necessity* in high-availability systems, such as servers, network switches, RAID storage, and other forms of communications infrastructure, that must operate with near-zero downtime over their useful life. The article on page 9 gives us an insight into the design and application of hot-swap controllers, key elements of pluggable modules for such systems.

In wireless base stations, the power amplifier (PA) dominates the performance in terms of power dissipation, linearity, efficiency, and cost. Monitoring and controlling the PA makes it possible to maximize the output power while achieving optimum linearity and efficiency. The article on page 14 discusses the elements of a monitoring-and-control solution for the PA using discrete components—and describes an integrated solution.

... AND ON THE BACK BURNER:

In principle, you apply a digital input to a DAC, and it provides an accurate output. In reality, the accuracy of the output voltage is subject to gain- and offset errors from the DAC and other components in the signal chain. The system designer must compensate for these errors in order to produce an accurate output voltage. "Open-Loop Calibration Techniques for Digital-to-Analog Converters," on page 18, provides some useful suggestions.

The principle of employing a user touch to cause a capacitance change to activate a switch is well understood, but implementing a PCB sensor design with proper shielding and routing poses a challenge. ADI provides a complete capacitive-sensing solution, including controller, evaluation tools, sensor design libraries, and software for the host microcontroller, described in "AC Shield Enhances Remote Capacitive Sensing" on page 18.

Consumer electronics, which tends to be lower frequency and less demanding than typical clock buffering applications, can use inexpensive high-speed op amps as an alternative to traditional clock buffers. High-speed amplifiers are less expensive than traditional clock buffers, yet can accommodate a wide range of designs. "Inexpensive High-Speed Amplifiers Make Flexible Clock Buffers," on page 19, offers sound advice on this topic.

Dan Sheingold [dan.sheingold@analog.com]

Analog Dialogue

www.analog.com/analogdialogue **dialogue.editor@analog.com**

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 42 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. For history buffs, the *Analog Dialogue* archives include all regular editions, starting with Volume 1, Number 1 (1967), plus three special anniversary issues.

If you wish to subscribe to the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

ISSN 0161-3626

Noise Figure and Logarithmic Amplifiers

[The Wit and Wisdom of Dr. Leif—6*]

By Barrie Gilbert

[Ed. *When Dr. Leif was about thirty, well before the turn of the century, he joined Analog Devices as an IC designer. He came with ample prior experience—both for this work and for his age. This wealth of experience included abundant knowledge about measurement instruments and control systems, traceable to his teenage years making radio receivers, transmitters, and TV sets, using surplus components purchased through telak companies (today's term, from "tele-acquisition," used during the first decade of the century).*

Dr. Leif has spent about as much of his time in teaching analog circuit principles as in direct design. Earlier, he wrote numerous "memos"—brief monographs—which were at one time widely consulted by his fellow designers and avidly read by newcomers to the company. Many of these were later transferred to e-form. Regrettably, these versions were lost during the period known as the "Information Age," as the "written word" was entrusted to progressively obsolescent generations of storage modalities and media. It was a time when everyone was suffocating under a glut of "data" while experiencing a dearth of deep-seated knowledge about analog design: "The Fundaments," as Newton Leif likes to call the essential principles, the roots of physical phenomena.

Recently, when a young engineer named Niku Chen joined his team at our Design Center in Solna, he encouraged her interest in recovering whatever of this treasure trove she could. Here is one such article that she found, written in 2008, reproduced in facsimile form. We trust it contains few, if any, errors. His prose, written in the American English of first-decade 21st century, is more flowery than we expect in 2029. The header indicates that Leif (who is still with ADI in Solna, and active in the field) was evidently very familiar with the Fundaments of Noise back then. But he also wanders around quite a bit in this odd little piece. These editorial comments are occasionally interpolated.]

Leif 2698:060508 Noise in Logarithmic Amplifiers

We occasionally receive inquiries about the *noise figure* of log amps. Whether this is a valuable metric in their common use as *power measurement* elements is for the user to decide. However, whenever a log-limiting amplifier is used in the *signal path* (in PM or FM applications), noise figure is clearly important, since it provides a measure of that system's ability to extract *information* from a signal in the presence of noise. Accordingly, this metric should be provided, in the event it is required for inclusion into a user's spreadsheet estimation of a system's performance. This memo is for field application engineers and customers alike.

Monolithic, fully calibrated logarithmic amplifiers (*log amps*), pioneered by Analog Devices over the past twenty years, are uniquely equipped as RF measurement elements at frequencies from near-dc up to 12 GHz in the latest products. Their special value stems in part from having a wide "dynamic range" and in part from presenting their measured values directly as decibel quantities. They are temperature-stable and exhibit excellent conformance to a "log law." The focus of this memo is on some limitations imposed by basic noise mechanisms. As always, in digging down to root causes, some side trips will be needed.

Log amps come in three basic forms. However, in their capacity as *RF power-measurement* devices, we are mainly concerned here with the first two types:

1. Those employing multistage amplification and progressive limiting[1] generate a close approximation to the logarithm in a piecewise fashion. Some of these parts also make available the output of the final limiting-amplifier stage, for extracting time-encoded information (PM or FM, baseband bit streams). These include the AD608, AD640/AD641 and the extensive AD8306/AD8307/AD8309/AD8310/AD8311/AD8312/AD8313/AD8314/AD8315/AD8316/AD8317/AD8318/AD8319 family, as well as closely matched dual log amps, such as the AD8302 (which also measures *phase*), and the ADL5519, having an unprecedented 1 kHz to 10 GHz measurement range.†

   These *progressive-compression log amps* include a rectifier (detector) with each of five to 10 low-gain (8 dB to 12 dB) stages, whose outputs are summed to produce a filtered voltage that is a decibel-scaled measure of average power. Where the final hard-limited signal is also provided (as in the 100-dB range products AD8306/AD8309), the logarithmic measure is often viewed as ancillary, and referred to as the *received-signal-strength indicator* (RSSI).

2. Those using an *exponential-gain amplifier* (X-AMP® architecture)[2] with a 60-dB typical gain span, followed by a *single* detector whose filtered output is compared to a reference level; the integrated error generates a voltage, which adjusts the amplifier gain to null the error (see text associated with Figure 6). That voltage is a representation of the decibel value of the applied signal, due to the accurate exponential (sometimes called "linear-in-dB") gain function. By giving the detector a square-law response, it is the power-equivalent (rms) value of the applied signal that is measured.

   This will be recognized as the general form of an *automatic-gain-control* (AGC) amplifier. Accordingly, we can call them *AGC-style log amps*. The AD8362, AD8363, and AD8364 are of this type, the latter two providing the simultaneous measurement and differencing of two input signals. In this type, there is usually no provision to access the amplified signal. An exception is the AD607 (actually a single-chip superheterodyne receiver), whose decibel-scaled RSSI output spans 100 dB, and whose signal outputs are the I/Q components of the demodulated IF.

3. Those based on the uncannily reliable translinear properties of a bipolar junction transistor (BJT)—the precise logarithmic relationship between its base-emitter voltage (V_{BE}) and its collector current (I_C) over a range of up to 10 *decades* of current (200 dB!). An early exploitation of this property in conjunction with an op amp was due to Paterson.[3]

   Modern products, now known as *translinear log amps*, are similar, deviating only in the details of implementation. This separate class of log amps, used in fiber-optic communication systems to measure optical power and control the gain of optical-mode amplifiers, only measures essentially *static currents*, from as low as 1 picoamp up to several milliamps. Alternatively, using external input resistors, voltages with a large range of amplitudes can also be measured. Examples include the AD8304, AD8305, ADL5306, and ADL5310.

Background

Any system's internal noise is a result of the fundamental thermal energy, kT, thus its absolute operating temperature, T (where k is Boltzmann's constant). In one case of general interest, the root source is an *antenna*, whose noise results from the electromagnetic coupling into the free-space resistance from which it receives its signal, and which has the basic value of 377 Ω. The signal and noise are equally coupled into the system via a first impedance transformation created by the design of the antenna, and thence conveyed by a cable of the same impedance. They operate at their

*[Ed. Note—The two earliest papers in this series, "The Four Dees of Analog, *circa* 2025" (1), and "The Fourth Dee: Turning Over a New Leif" (2) were not numbered when originally published.]

†Information and data sheets on all products mentioned here may be found on the Analog Devices website, www.analog.com.

greatest power efficiency in driving, say, a 300-Ω balanced ("twin" or "ribbon") feeder, or alternatively a 50-Ω (or occasionally a 75-Ω) coaxial cable.

As an aside, the minimum loss in a coaxial cable occurs when its characteristic impedance is 71 Ω. Above this, the resistance of the thinning *inner conductor* increases the loss; below, it is the thinning *dielectric layer* that increases loss. While not optimal, 50 Ω has become the resistance reference level for measurement, largely for reasons of convenience and standardization. Unless otherwise stated, it is the value used in specifying noise figure.

As a power source (really, a *transducer*, from electromagnetic to electrical power), an antenna exhibits a complex impedance $Z_A = \mathrm{Re}(Z_A) + j\mathrm{Im}(Z_A)$. Nevertheless, it acts purely resistive over a generally narrow range of frequencies. Clearly, the *power* it can deliver to an *open circuit*—such as an ideal voltage-responding element—is *zero*, since none of the available current is extracted from the source. Similarly, the power into a short circuit—such as an ideal current-responding element—is zero, since none of the voltage swing is used. The power-transfer theorem shows that the maximum power that can be delivered to a load connected to this source occurs when the resistive part of the load impedance is made equal to $R_A = \mathrm{Re}(Z_A)$, say, 50 Ω (Figure 1).

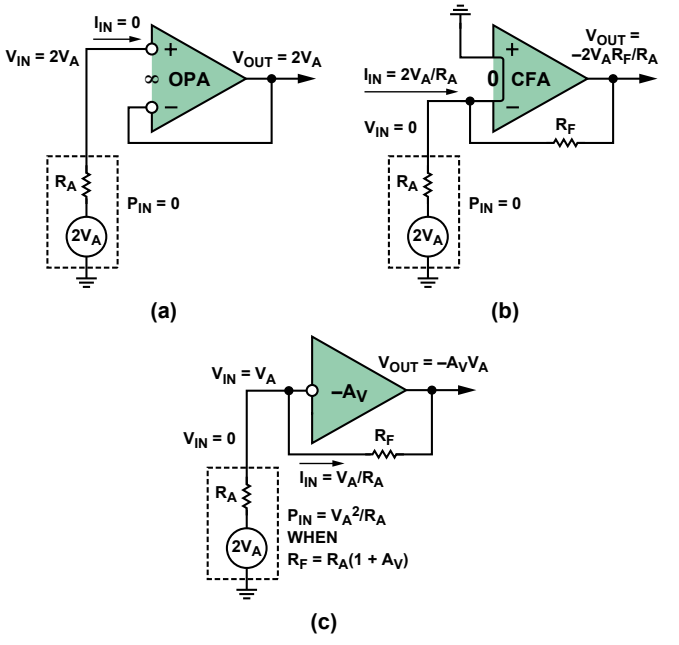


Figure 1. Using either a voltage-follower (a) or a current-feedback amplifier (b), none of the source power is utilized; but when a fixed-gain inverting-mode amplifier (c) is used, augmented by the feedback resistor, R_F, R_{IN} is equal to R_A when R_F is equal to $R_A(1 + A_V)$, resulting in a noise factor of $\sqrt{(2 + A_V)/(1 + A_V)}$.

Log amps intended for RF power measurement (often referred to simply as *RF detectors*) do not generally require extremely low noise figures. Instead, the design emphasis in the first amplifier stage is to minimize the *voltage-noise spectral density* (VNSD), typically a few nV/√Hz, and its noise performance is specified in this way. When this VNSD is integrated over the log amp's RF bandwidth (not the post-detection—or so-called *video*—bandwidth), the rms noise typically amounts to tens of microvolts. Only when this voltage is referred to the impedance level at the input can the device's internal noise be expressed as a power level (as so many dBm: *decibels relative to 1 mW*). The integrated noise voltage sets a bound on the smallest input *voltage* that can be measured with certainty—and thus *indirectly* on the minimum signal power.

Figure 2 shows how this lower bound on the dynamic range can be expressed as power for various choices of impedance. Note that the response, illustrated for a typical scaling of 20 mV/dB (400 mV/decade), is specifically for a sine wave input; a 0-dBV input signifies a sine input whose rms amplitude is 1 V. Below each axis marker is the corresponding power level when the voltage is applied to a termination resistor of 50 Ω or 316 Ω.

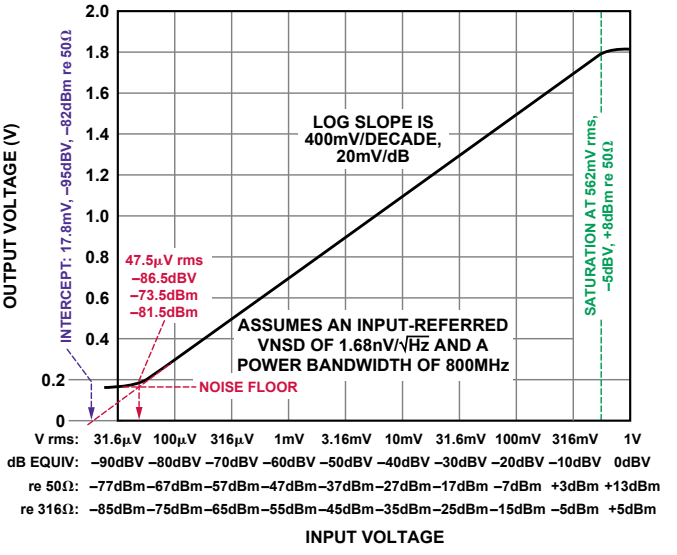


Figure 2. Log amp response to an input voltage, showing the lower bound on dynamic range, and the correspondence between alternative scales.

In an earlier monograph, LEIF 2131:080488,* I discuss how the basic RF log-amp types compare in responding to various other waveforms. For many years the effect of the signal's waveform on the logarithmic intercept (often misleadingly called "offset") went largely unnoticed because early log amps were fairly crude and needed to be manually adjusted *in situ*. As the first *complete, fully calibrated, multistage* log amp, the AD640 changed all that. Elsewhere,[4] I have shown that log amp design need no longer be empirical (as it certainly used to be[5]).

*[Ed. *We may be able to acquire this document (if Niku Chen found it) and publish it in* Analog Dialogue *at a later date*].

Johnson-Nyquist Noise

An ideal matched-input antenna *amplifier* absorbs the maximum available power, while adding no noise of its own. But—apart from naturally occurring noise sources in the surroundings—the antenna will have its own noise, typically referred to the 50-Ω impedance level, just as any resistor generates noise. Note that this is not the consequence of some particular manufacturing technology, although there are additional noise mechanisms at work, to varying degrees, in most practical resistors.

Resistor noise was first noted by Johnson[6] and later analyzed and quantified by Nyquist.[7] It is the electrical manifestation of *the random motion of current carriers* in a conductive medium. Nyquist observed that the *energy* of this motion can be stated in terms of the Boltzmann constant, k, and absolute temperature, T, which translates to *noise power*, P_N (that is, energy/unit-time). It is customary to express time in reciprocal form, as the system bandwidth, B (hertz). The result is as simple as it is fundamental: the noise power associated with a conductor is just kTB (watts).

Now consider a real resistor, R, at an absolute temperature, T, connected to an ideal noise-free resistance, R_O, of equal value. Here, the noise voltage, E_N, of the resistor, R, is halved by virtue of the load, R_O, the latter generating no noise. So the noise power

in R is simply $(E_N/2)^2/R$, which must be equal to the kTB noise power; that is, $E_N^2/(4R) = kTB$. Thus, $E_N = \sqrt{4kTRB}$ V rms.

Noise-figure specifications assume (somewhat arbitrarily) that an antenna "operates at" a temperature of 290 K (16.85°C). What is really being referred to here is not the actual temperature of the metal elements comprising the antenna, nor the air temperature that surrounds it; even less the temperature of the directionally narrow source of the signal. Rather, it is the average temperature of all the material objects within the full scope of the antenna's "view," modified by its polar diagram (sensitivity vs. direction). The background temperature (thus kT), near Stockholm during winter, as perceived by an antenna seeking a source beyond the warm buildings, may actually be much higher than in pointing the antenna to the Nevada sky (though, in fact, air temperature will have a small effect on the antenna's intrinsic noise figure).

At 290 K, the open-circuit VNSD of a 50-Ω antenna, like that of any other resistor, is 894.85 pV/$\sqrt{\text{Hz}}$. Applied to a noise-free load of 50 Ω, the noise voltage at the load is halved, to 447.43 pV/$\sqrt{\text{Hz}}$, so the noise power is this voltage squared divided by 50 Ω, or 4×10^{-21} W/Hz (note: no longer $\sqrt{\text{Hz}}$). Expressed as a *power spectral density* in milliwatts, this is –173.975 dBm/Hz. Not surprisingly, it is called the *thermal noise floor*.

Notice that the impedance level is arbitrary; the noise floor would still be –174 dBm/Hz if the antenna were matched into a 75-Ω load. This is evident when we note that, in the above calculation, the quantity $\sqrt{4kTR}$ was first halved to get $\sqrt{kTR}$ as the load voltage, which was then squared, giving kTR, and then divided by the *same resistance* (assuming matching), coming back to kT.

[Ed. *This is rock bottom. But, of course, the temperatures of the active devices that follow the antenna can be lowered. In today's cosmotronics, a zygomaser (those dual-path masers, operating at cryogenic temperatures) is used as the low-noise amplifier. But a pair of such masers isn't cheap, and they won't fit too well into the typical wrist-worn HSIO Municator!*]

Noise Figure and Noise Mechanisms

If the first-stage amplifier is not ideal, it will add its own noise to the signal. So let's suppose that *an exceptionally quiet op amp* is used as a voltage-mode amplifier. To ensure that the source—for example, an antenna—is properly terminated, a 50-Ω resistor is placed across the signal-input port of this amplifier. Before even considering the op amp's own internal noise, we've degraded the *noise figure* by 3 dB. Here's why. First, the definitions:

$$\text{Noise } \textit{Factor} = \frac{\text{Inherent Signal-to-Noise Power Ratio of the Signal}}{\text{Signal-to-Noise Power Ratio at the System's Output}}$$

$$\text{Noise } \textit{Figure} = 10 \log_{10} (\text{Noise Factor}) \text{ dB}$$

As we've seen, the open-circuited signal voltage, V_{IN}, is associated with an open-circuit noise voltage, say E_N—the *voltage noise spectral density* (VNSD)—integrated over the system bandwidth. Again, imagining a load formed by a *noise-free impedance* of 50 Ω, the signal voltage across this load is halved, to $V_{IN}/2$, while its noise voltage is also halved, to $E_N/2$. Thus, the signal-to-noise voltage ratio and, consequently, the signal-to-noise power ratio, remain unaffected. The noise *factor* is unity, and the noise *figure* (hereafter NF) is 0 dB.

Of course, this is only possible using a noise-free load. Such ideality is conceivable when the load is created from reactances. For example, $\sqrt{L/C}$ has the dimensions of resistance, while an L/C network, in principle, has no loss. Even real L/C networks, have very low loss: they are essentially nondissipative. (By contrast, resistors convert power into heat, which is then lost to the universe.) But even when assisted by the magic of L's and C's, the elements essential to providing power gain, the *active devices* inherently have *ohmic* resistance to degrade the NF.

Shot Noise

Junction devices also exhibit fundamental *shot-noise* phenomena, emerging from a different sort of stochastic mechanism, namely, *the granularity of an electric current crossing a potential barrier*. This was first observed by Schottky[8] in the electrons emitted from the cathode of a vacuum diode. Being released randomly, they form a Poisson sequence of events—each electron, like a honeybee, faithfully carrying its precise little packet of charge, $q = 1.602 \times 10^{-19}$ coulombs.

A similar process arises in injecting carriers from the emitter into the base of a BJT. Fluctuations in emission/injection are due to the continual tiny changes in the carrier energy against the work-function of a cathode, or the band-gap energy of a semiconductor junction. In the latter case (unlike a vacuum diode), some of the injected carriers recombine in the base region(s), where there are other smaller noise mechanisms; and the noise at the collector is modified accordingly. Thus, it is known as *collector shot noise*—but confusingly, since the root cause is at the initial injection site.

You should note that Johnson noise is due to the random *motion* of carriers in a conductive medium, while shot noise is due to the random *occurrence* of these carriers as they encounter a barrier.

It is readily shown that the magnitude of the spectral density of the shot noise current, in A/$\sqrt{\text{Hz}}$, is $\sqrt{2qI}$, where q is the electron charge and I is the mean bias current, taken as I_C for a transistor. For example, at a collector current of 1 mA, this noise amounts to 17.9 pA/$\sqrt{\text{Hz}}$. However, unlike the resistor's noise, *shot noise is temperature-independent* (when all the detailed local mechanisms, including the temperature-dependence of transconductance, are combined for the case of the transistor). It is no more than a manifestation of the granularity of a current. Further, while resistor noise directly represents *power*, shot noise is only a *fluctuation in current* and thus corresponds to some power only when it flows in an impedance, often at some "output."

Now, such an impedance (not the "collector output resistance") exists within a transistor. It is the "incremental emitter resistance," r_e, the inverse of the small-signal transconductance, equal to kT/qI_C. This gives rise to a noise voltage, which can be referred to the base-emitter port; it has a spectral density that is *the product of the noise current and this resistance*, amounting to $kT/qI_C \times \sqrt{2qI_C}$, which reduces to $kT\sqrt{2/qI_C}$.

At I_C = 1 mA and 27°C, this amounts to VNSD of 463 pV/$\sqrt{\text{Hz}}$ (Figure 3). Keep in mind that r_e is *not* an ohmic resistance, but simply the partial derivative, $\partial V_{BE}/\partial I_C$, and thus it is *noise-free* (which is why it is shown using a distinctive symbol). However, it is interesting to note that the said product of the shot noise current and this resistance is identical to the noise voltage generated by a real resistance of *half its value*. Here, for example, r_e is 25.86 Ω, and the noise of a real 12.93-Ω resistor is also 463 pV/$\sqrt{\text{Hz}}$. This is simply because the "shot-noise-times-r_e" can be written as $2\sqrt{(kT)^2/qI} = \sqrt{2kTr_e}$ which is $\sqrt{4kT(r_e/2)}$. This quantity equates to $\sqrt{4kTR}$, the Johnson noise of a resistor, R, only when $R = r_e/2$. This must clearly "work out right." It does leave some perplexing questions, though. Why is there such an amusing convergence of these two apparently very disparate fundamental noise processes? That's a topic for another (long) memo!

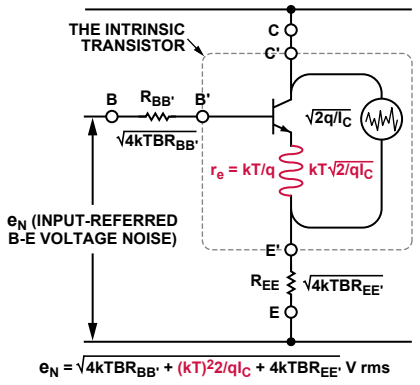


Figure 3. Primary noise sources in a BJT at moderate frequencies.

Aspects of Low-Noise Amplifier Design

The design of matched-impedance low-noise amplifiers is a large topic in its own right; but it is useful to consider how some basic aspects of the BJT (of any modern technology, noting that SiGe and other exotic heterojunction transistors are just BJTs on steroids) set a fundamental lower bound on the noise figure, even before the effects of the unavoidable contacting resistors, $R_{BB'}$ and $R_{EE'}$, are included in the recipe.

Figure 4 shows what at first appears to be a highly rudimentary and incomplete circuit, little more than a diode-connected transistor with a resistor, R_F, in its base, and biased by a current source. Surprisingly, this is a practical (although not optimal) *low-noise amplifier* (LNA): its V_{CE}, the sum of the V_{BE} and the voltage drop across R_F, is quite sufficient for these illustrative purposes; and there are numerous ways to elaborate this basic form while retaining the relevance of this analysis.

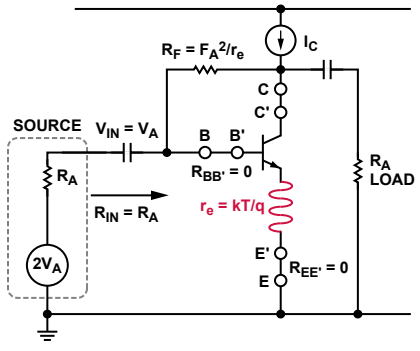


Figure 4. A rudimentary translinear LNA, illustrating the Fundaments.

The approach may be called the *translinear viewpoint of LNAs*, since it starts with an ideal resistance-free transistor model (see "Foundation Design," Leif 1677:011284)* and demonstrates how one can gain profound insights into behavior that turns out to be both beautiful in certain respects, yet deeply complex in others.

*[Ed. *There follows in the Leif monograph a rather philosophical account of how the value of the feedback resistor, R_F, can be seen as necessarily having to equal R_A^2/r_e if a reciprocal match to the source and load is required, without recourse to mathematics. His basic point is that there are only three key resistances in the circuit: The unknown, R_F, and the knowns, R_A and the BJT's r_e. So (according to Leif) there are only two dimensionally correct ways of linking them: either $R_F = r_e^2/R_A$ or $R_F = R_A^2/r_e$. The first of these is clearly incorrect.*]

Now, the strange thing about this little circuit is that *the match is precisely preserved for every value of I_C from zero on up*! This assumes that we arrange for R_F to track r_e in the manner shown, which means giving it the algorithmic value qI_CR_A2/kT. It follows, as is so often the case, that I_C must be *proportional to absolute temperature* (PTAT) to maintain this match—and a temperature-stable gain having the signed value $1 - qI_CR_A/kT$.

This can be seen by setting $I_C = 0$, when R_F is obliged to also be zero. Then the transistor has no transconductance, and the zero-valued resistance, R_F, simply connects the source to the load for a gain of $\times 1$ (that is, 0 dB). At a critical value of current, $I_C = kT/qR_A$, that is, 517.2 μA = 25.86 mV/50 Ω, when R_A = 50 Ω, the gain becomes zero (i.e., $-\infty$ dB), after which it rises, crossing –1 (back to 0 dB again!) at an I_C of precisely 1.034 mA (for T = 300 K).

From that value onward, the gain increases. All the while, the input impedance remains firmly stuck at the value R_A, here 50 Ω. Figure 5 shows the input impedance, voltage gain (which is also the power gain when reciprocally matched), and noise figure. In this ideal simulation, the NF is under 0.4 dB at an I_C of 10 mA at which point the gain is $\times 18.33$ (inverting), that is, 25.3 dB.

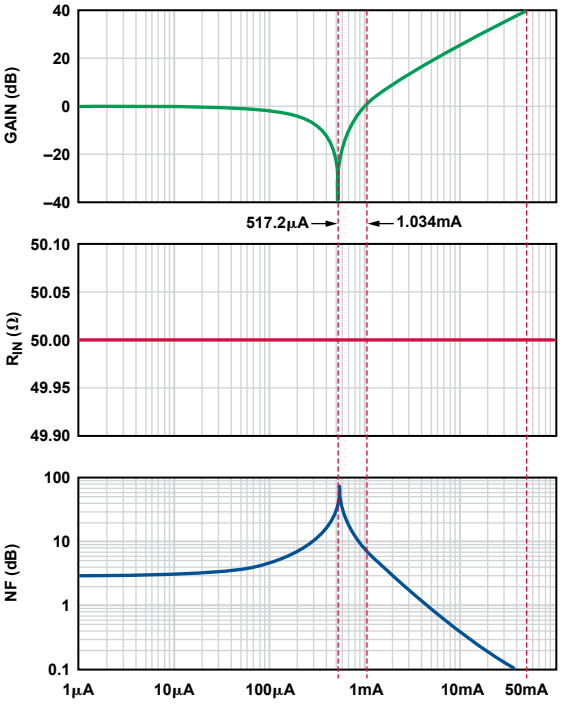


Figure 5. The peculiar behavior of the translinear low-noise amplifier.

This analysis is at once optimistic and pessimistic. It is optimistic in neglecting the noise contributions of the transistor resistances, notably $R_{BB'}$ and $R_{EE'}$, and the consequence of finite small-signal current gain, β_{AC}, which creates a noise current, $\sqrt{2qI_C}/\beta_{AC}$, which flows in the effective source impedance (including R_{BB}). It is very important to keep in mind that β_{AC} at high frequencies is very much lower than at dc. Its magnitude is closely equal to the device's f_T—for a given geometry and bias—divided by the signal frequency, f_S (and its phase is +90°). Thus, for an f_T of 10 GHz (it is never as high as its peak value) and an f_S of 2 GHz, this BJT's common-emitter current-gain is a pitiful 5!

Thus, in this example, one-fifth of the collector shot noise, that is, $0.2\sqrt{2qI_C}$ = 11.3 pA/$\sqrt{\text{Hz}}$ appears in the base when I_C = 10 mA. This operates on the total base impedance, thus at the very least the source impedance of 50 Ω (it need not be resistive), generating 566 pV/$\sqrt{\text{Hz}}$ of VNSD. This is *over 12 times* the 46.3 pV/$\sqrt{\text{Hz}}$ due to the r_e-induced shot noise at this current!

But these figures are pessimistic in neglecting all the ingenious things that can be done using *reactive elements* around the active device; to drastically lower the NF, although invariably at the expense of distortion (commonly expressed in terms of the input-

referred two-tone third-harmonic intercept, *IIP3*, and less usefully in terms of the 1-dB gain-compression point, *P1*dB).

[Ed. *At the top of this page in our copy of Leif's monograph, this penciled note appears: "Niku: Here's a curious aside: using a grounded-base topology with I_C = 517 μA to set R_{IN} to 50 Ω, and thus match a 50-Ω source, you will find by spectral analysis that the P1dB point is never reached. The gain error just grazes −0.9 dB at a certain input level, then asymptotically returns to 0 dB. Isn't that interesting?! Can you figure out what's going on here?" No date is appended.*]

Nonetheless, an NF as low as 0.3 dB is practicable in a *high-gain* transistor amplifier at room temperature when other attributes (such as linearity) can be relaxed. For example, the amplifier in Figure 1(c) exhibits a noise factor of $\sqrt{(2 + A_V)/(1 + A_V)}$ using an *amplifier* with negligible voltage- and current-noise. If we set the gain, A_V, to 20 V/V (26 dB), the NF can be as low as 0.2 dB, that is, 20 $\log_{10}\sqrt{22/21}$ (the first factor is 20 here because we are in the voltage domain), even though the noise due to the feedback resistor is as high as 4.18 nV/Hz when chosen to match a 50-Ω source, that is, to 1.05 kΩ. Of course, in practice (darn it!) the amplifier's input noise will not be negligible.

Power Calibration of a Logarithmic Detector

Very few electronic elements respond directly to power. To do so, they must not only *absorb* some source power, accurately and completely, as does a resistor; but the *heat that is generated in this way* must then be measured with corresponding accuracy. When a resistor was included across the input terminals of our ideal voltage-mode amplifier, the power supplied by the source heated up the resistor by a minuscule amount. Just as an example, if the signal power were −30 dBm—that is, one microwatt—and the thermal resistance of the load were, say, 100°C/W, it would heat up by only 100 microdegrees.

This is a tiny temperature change; but some power detectors *are* nevertheless based directly on measuring the temperature of a low-mass resistor, suspended on ultrathin fibers in such a way as to have an extremely high thermal resistance—perhaps as much as 100,000°C/W. Even then, the temperature changes are only of the order of millidegrees. These *truly fundamental* power-responding elements are still used at high microwave frequencies, but since the turn of the century, high-accuracy inexpensive IC detectors have been available; they can be used with ease from dc to over 12 GHz.

Some TruPwr™ *detectors* of the AD8361 and ADL5500/ADL5501 class use analog-computing techniques to magnitude-square the instantaneous waveform values of a signal, thus producing an intermediate output $V_{SQ} = kV_{SIG}^2$. This crucial first step is then followed by averaging and a square-root operation—finally yielding the *root-mean-square* (rms) value. In designing these products, vigilant attention has to be paid to maintaining low-frequency accuracy at every step, while using circuit techniques that are at the same time accurate with microwave waveforms.

Many of the newer *rms*-measuring products produced by Analog Devices, also in the TruPwr category, use a high-precision AGC technique (Figure 6). They first amplify the signal from an input level which may be only a few millivolts, then apply this signal to one squaring-cell. Its output is compared to that of an identical cell operating with a fixed input (the "target" voltage: V_T). The integrated imbalance in these outputs then either raises or lowers the gain as necessary to restore exact balance between the squarer outputs. Since the variable-gain amplifier used employs X-AMP architecture, it inherently provides an accurate inverse-exponential gain in response to a control voltage, which thus represents the rms amplitude at the input as a precisely scaled *decibel quantity*.

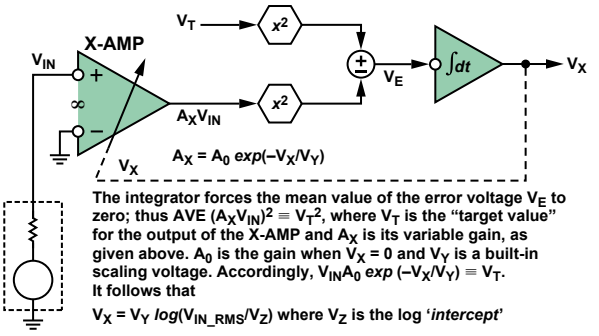
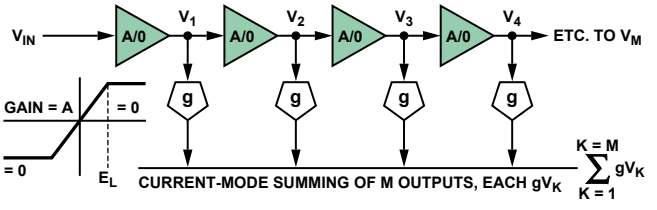


Figure 6. General structure of an AGC-style log amp.

An earlier type of power detector, now universally known as a "logarithmic amplifier" (although it usually performs only the *measurement* function, providing an output proportional to the logarithmic magnitude of the input's *mean* voltage amplitude), uses cascaded gain stages of the hard-limiting kind. It is readily demonstrated that the log function arises naturally as a piecewise approximation when the output of each cell contributes to a progressively increasing sum.[4] Note that this operation does not inherently address the need to respond to the "mean-square" or "true power" of the input—although, as a matter of interest, the response to noise-like signals *does* in fact closely track their rms value. Figure 7 shows an illustrative schematic of this type, *the progressive-compression log amp*.



The amplifiers have a gain A up to a limiting input voltage, $\pm E_L$, above which the incremental gain drops to zero. Each output is converted into a current-mode form in an absolute-value or squaring cell, g, and these currents are summed. In this simplified scheme, the first stage to limit would be the fifth amplifier (not shown). This occurs when $V_{IN} = E_L/A^4$. At some point as the input is increased, the fourth stage starts to limit. This occurs at E_L/A^3. Over this interval—a *ratio of A* at the input—the output changes by "one unit" of gV_K, a signal-independent unit of, say, 100μA. This is the essential nature of the logarithmic function, since "a ratio of A at the input" amounts to 20log(A) decibels.

Figure 7. An illustrative progressive-compression log amp.

Noise Figure and Logarithmic Detectors

It will by now be very clear that *none of these detectors respond to the power* of a signal *being absorbed* at their input. Rather, the response is strictly to the *voltage waveform* of the signal. All of the signal's power is absorbed by the resistive component of the input impedance, which is in part internal to the IC, and in part added externally to lower this impedance, commonly down to 50 Ω. This casts doubt on the value of an NF specification. Ideally, the sensitivity and measurement range of log amps of these types ought never to be specified in "dBm"—which refers to *power* in *decibels above 1 mW*—but always in "dBV," *the decibel level of a voltage relative to 1 V rms*. A signal of this amplitude dissipates 20 mW in a 50-Ω resistive load, which amounts to 13.01 dBm *re* 50 Ω ("*referred to a* 50-Ω load").

Nevertheless, provided the net shunt resistance at the log amp input is known, graphs of its amplitude response may use a common horizontal axis scaled in both dBm and dBV, offset by a fixed amount, which for 50 Ω is 13 dB, as illustrated in Figure 2. Unfortunately, the RF community does not generally think in dBV terms, and this practice is not rigorously followed. In many data sheets only a dBm scale is used, leading to the *appearance of a genuine power response*, which, as has been strenuously noted, is never the case for an RF power sensor.

Even when a log amp's input stage is designed to match the source impedance—which makes better use of all the available power and usefully lowers the noise floor—the response is still to the *voltage* appearing at the input port. Of course, this does not mar its utility as a power-measuring device. At lower frequencies, it is easy to design ICs that explicitly sample both the voltage and current in and through a load. An example of this practice is found in the ADM1191.

Recall that, for the case of a 50-Ω source, loaded by a 50-Ω resistor, the degradation in noise figure, to 3 dB, was entirely due to the additional noise of the *termination* resistor. When the measurement device presents an open circuit to the source either the input is shunted with a 50-Ω resistor to set the *effective power-response scale*; or the input is padded down to 50 Ω from the log amp's finite R_{IN}. The noise voltage associated with the input port is no longer simply the Johnson noise of this resistance; it is now the vector-sum of that noise voltage and the input noise voltage of the measurement device. Furthermore, the log amp's inherent *input noise current* will be multiplied by this net shunt resistance, and the resulting voltage, if significant, may need to be included in the vector sum. However, it is usually already included, indirectly, in the input-referred VNSD specification.

Suppose the latter is stated as 1 nV/$\sqrt{\text{Hz}}$. Next, take the 300 K (27°C) value—the typical operating temperature of a PC board—for the Johnson noise at 25 Ω (the 50-Ω source in shunt with the net 50 Ω of the external loading resistor and the log amp's R_{IN}) as $\sqrt{4kTR} = \sqrt{4k \times 300 \times 25} = 643.6$ pV/$\sqrt{\text{Hz}}$. Now, the vector-sum of these is 1.19 nV/$\sqrt{\text{Hz}}$. Arbitrarily assigning a unit amplitude to the "signal," (noting that the 300 K noise for the 50-Ω source is 910 pV/$\sqrt{\text{Hz}}$) we have

$$\text{Noise } \textit{Factor} = \frac{\text{Voltage SNR of the Source}}{\text{Voltage SNR at the Load}} = \frac{1/0.91 \text{ nV}/\sqrt{\text{Hz}}}{0.5/1.19 \text{ nV}/\sqrt{\text{Hz}}}$$

$$= 2.615 \text{ (a } \textit{voltage} \text{ ratio)}$$

$$\text{Noise } \textit{Figure} = 20 \log_{10}(\text{Noise Factor}) = 20 \log_{10} 2.615 = 8.345 \text{ dB}$$

The more general form for the case of a 50-Ω source and 50-Ω load is $20 \log_{10}(2.2 \times 10^9 \sqrt{0.6436^2 + VNSD^2})$. Below is a short table of noise figure (NF) for several values of the voltage noise spectral density at the log amp's input, assuming a 50-Ω source and a net resistive load at the log amp's input of 50 Ω.

VNSD (nV/$\sqrt{\text{Hz}}$)	NF (dB)
0.00	3.012
0.60	5.728
1.00	8.345
1.20	9.521
1.50	11.095
2.00	13.288
2.50	15.077

Baseline Sensitivity of a Logarithmic Detector

As noted, *noise figure* is a relevant metric when the log amp being quantified is a multistage limiting amplifier, providing signal output, which may also operate as a *detector*, providing an RSSI output—for example, the AD8309. This part is specified as having an input-referred noise (VNSD) of 1.28 nV/$\sqrt{\text{Hz}}$ when driven from a terminated 50-Ω source (that is, with a net 25 Ω of resistance across its input port). From the expression provided above, this amounts to an NF of 9.963 dB. The data sheet value of NF (Page 1) is 6 dB lower, at 3 dB, based on taking the ratio 1.28 nV to the 50-Ω VNSD of 0.91 nV, with a decibel equivalent of $20 \log_{10}(1.28/0.91) = 2.96$ dB.

The baseline sensitivity of a log amp is limited by its bandwidth. For example, assume a total VNSD at the input of a log amp (whether the progressive compression or AGC type) of 1.68 nV/$\sqrt{\text{Hz}}$ and an effective noise bandwidth of 800 MHz. The integrated RTI noise over this bandwidth is 47.5 μV rms (that is, 1.68 nV/$\sqrt{\text{Hz}} \times \sqrt{8} \times 10^8$ Hz). Expressed in dBm re 50 Ω, this is $10 \log_{10}(\text{Noise Power}) = 10 \log_{10}(47.5 \text{ mV}^2/50\ \Omega) = -73.46$ dBm.

This "measurement floor" is a more useful metric than NF, since it shows that measurements of signal power below this level will be inaccurate. Here, it will be found that the *indicated* power for an actual single-tone sine wave input near –73.46 dBm floor will be very close to the same value, assuming the noise waveform is Gaussian. As another example, the input-referred noise spectral density of the AD8318 is found (in the first column of Page 11 of the Rev. B data sheet) to be 1.15 nV/$\sqrt{\text{Hz}}$, which amounts to an integrated noise voltage of 118 μV rms in that part's 10.5-GHz bandwidth. This is a noise power of –66 dBm, re 50 Ω. The user should also be aware that, in a progressive-compression log amp having too few stages, the measurement floor may be determined, not by noise, but simply by insufficient gain.

END NOTES

[1] www.analog.com/library/analogdialogue/cd/vol23n3.pdf#page=3

[2] www.analog.com/library/analogdialogue/cd/vol26n2.pdf#page=3

[3] Paterson, W. L. "Multiplication and Logarithmic Conversion by Operational-Amplifier-Transistor Circuits." *Rev. Sci. Instr.* 34-12, Dec. 1963.

[4] Gilbert, B. "Monolithic Logarithmic Amplifiers." Lausanne, Switzerland. Mead Education S.A. Course Notes. [1988?]

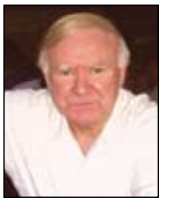
[5] Hughes, R. S. *Logarithmic Amplification: with Application to Radar and EW.* Dedham, MA: Artech, 1986.

[6] Johnson, J. B. "Thermal Agitation of Electricity in Conductors." *Phys. Rev.* 32, 1928, p. 97.

[7] Nyquist, H. "Thermal Agitation of Electronic Charge in Conductors." *Phys. Rev.* 32, 1928, p. 110.

[8] Van der Ziel, A. *Noise*. Prentice Hall, 1954.

THE AUTHOR



Barrie Gilbert (barrie.gilbert@analog.com), the first ADI Fellow, has "spent a lifetime in the pursuit of analog elegance." He joined Analog Devices in 1972, was appointed ADI Fellow in 1979, and manages the Northwest Labs in Beaverton, Oregon. Barrie was born in Bournemouth, England, in 1937. Before joining ADI, he worked with first-generation transistors at SRDE in 1954, and at Mullard, Ltd.; later at Tektronix and Plessey Research Labs. Barrie is an IEEE Fellow (1984) and has received numerous awards. He has some 50 issued patents, has authored about 40 papers, is coauthor of several books, and is a reviewer for several journals. He was awarded an Honorary Doctorate of Engineering from Oregon State University in 1997.

Understanding Hot Swap: Example of Hot-Swap Circuit Design Process

By Marcus O'Sullivan

INTRODUCTION

High-availability systems, such as servers, network switches, redundant-array-of-independent-disk (RAID) storage, and other forms of communications infrastructure, need to be designed for near-zero downtime throughout their useful life. If a component of such a system fails or needs updating, it must be replaced without interrupting the rest of the system. The board or module will have to be removed—and its replacement plugged in—while the system remains up and running. This process is known as *hot swapping*, or in some cases hot plugging[1] (where the module interacts with the system software). To hot swap safely, connectors with staggered pins are often used to ensure that grounds and local power are established before other connections are made. In addition, each printed-circuit board (PCB) or plug-in module has an on-board *hot-swap controller*[2] to facilitate the safe removal and insertion of the module from a live backplane. While in operation, the controller also offers continuous protection from short circuits and overcurrent faults.

Although the currents that must be interrupted and started up can be large, some of the subtleties of high-current design are often given very little consideration. Since the "devil is in the details," this article will focus on the function and significance of the components of a hot-swap control circuit—and provide an in-depth look at design considerations and optimum component selection criteria in the design process using an Analog Devices ADM1177[3] hot-swap controller.

Hot-Swap Topologies

The two system-power levels commonly found in high-availability systems, –48 V and +12 V, use different configurations for hot-swap protection. The –48-V system incorporates low-side hot-swap control and pass-MOSFET; +12-V systems use a high-side controller and pass-MOSFET.

The –48-V approach originated in traditional telecommunications-exchange system technology. Examples can be seen in Advanced Telecommunications Computing Architecture (ATCA) systems, optical networks, base stations, and blade servers. As a voltage commonly obtained from battery stacks, 48 V was chosen because power and signals could be transmitted over distance without significant losses, yet the level is not high enough to risk severe electric shock under ordinary conditions. Negative polarity was chosen because, in the inevitable presence of moisture when exposed to the elements, the migration of metallic ions from anode to cathode is far less corrosive with the *positive* terminal grounded.

In data communications systems, however, where distance is not an important factor, the +12-V supply is more reasonable, making it popular in blade-server and network-system designs. This article will concentrate on +12-V systems.

The Hot-Swap Event

Consider a system with a 12-V backplane and a rack of removable modules. Each module must have the ability to be withdrawn and replaced without affecting the normal operation of any of the adjacent modules in the rack. In the absence of a controller, each of the modules may present a considerable amount of load capacitance to the supply line, usually of the order of millifarads. When a module is first inserted, its uncharged capacitors demand as much current as is available to charge up the load. If this *inrush current* is not limited, it could reduce terminal voltages, causing a significant brownout on the main backplane, resetting many of the adjacent modules on the system, and damaging the module's connectors due to the high initial current.

This can be resolved with a *hot-swap controller* (Figure 1), which carefully controls the inrush current to ensure a safe power-up interval. The hot-swap controller will also continually monitor the supply current after power-up for protection against short circuits and overcurrent conditions during normal operation.

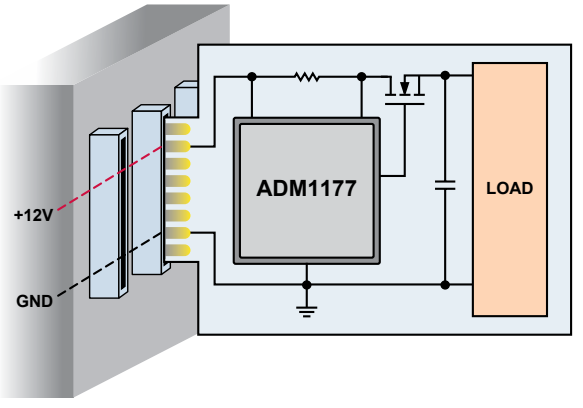


Figure 1. Hot-swap application diagram.

The Hot-Swap Controller

The ADM1177 hot-swap controller consists of three main components (Figure 2): an N-channel MOSFET that serves as the main power-control switch, a sense resistor that measures the current, and the hot-swap controller—which includes a current-sense amplifier—completing the loop to control the MOSFET's pass current.

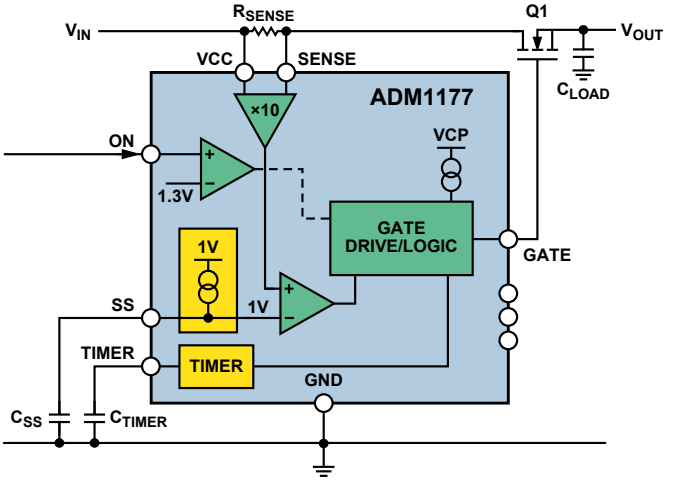


Figure 2. ADM1177 functional block diagram.

Inside the hot-swap controller, a current-sense amplifier monitors the voltage drop across the external sense resistor. This small voltage (typically ranging from 0 mV to 100 mV) must be amplified to a useful level. The amplifier gain in the ADM1177 is 10, so, for example, a 100-mV drop produced by a given amount of current will be amplified to 1 V. This voltage is compared to a fixed or variable reference voltage. With a 1-V reference, a current that produces a voltage greater than 100 mV (±3%) across the shunt will cause the comparator to indicate an overcurrent. The maximum-current trip point is thus principally determined by the shunt resistance, the amplifier gain, and the reference voltage; the shunt resistance value sets the maximum current. A *TIMER* circuit sets a limit to the length of time a given overcurrent condition can exist.

The ADM1177 has a *soft-start* function in which the overcurrent reference is ramped up linearly rather than turned on abruptly, forcing the load current to follow in a similar manner. This is achieved by injecting current from an internal current source into an external capacitor (SS pin) to linearly ramp the comparator's reference input from 0 V to 1 V. The external SS capacitor sets the rate of this ramp. If necessary, the SS pin can also be driven directly by voltage to set the maximum current limit.

An ON circuit, consisting of a comparator and reference circuit, enables the device. It accurately programs the voltage that the supply must reach to enable the controller. Once the device is enabled, the gate begins to charge up. The gate of the N-channel MOSFET used in this type of circuit must be above the source. In order to achieve this over the range of supply voltage (VCC), the hot-swap controller has an integrated charge pump capable of maintaining the GATE pin as much as 10 V higher than VCC. The GATE pin requires a charge-pumped pull-up current to *enable* the MOSFET and pull-down currents to *disable* the MOSFET when necessary. Weak pull-down currents are used for regulation, and stronger pull-down currents are used to quickly disable the MOSFET in the event of a short circuit.

The final essential block of the hot-swap controller is the *TIMER*, which limits the time the current is in regulation during an overcurrent event. MOSFETs are designed to withstand a given amount of power for a prescribed maximum time. The MOSFET manufacturers outline this range, or *safe operating area* (SOA), using a graph such as that shown in Figure 3.

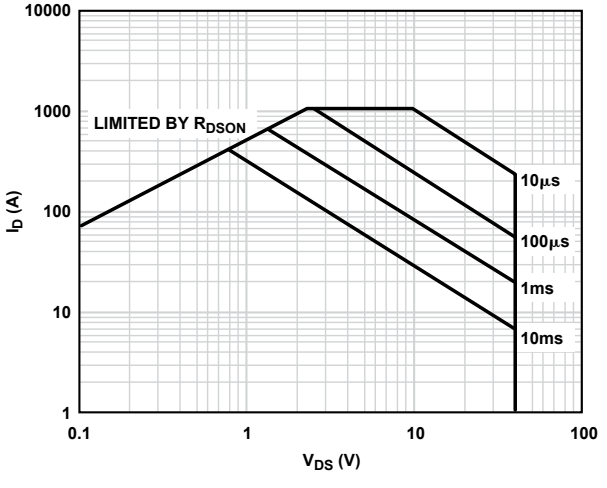


Figure 3. MOSFET SOA graph.

The SOA graph shows a relationship between the combined drain-source voltage, drain current, and the time duration that the MOSFET can withstand this dissipation. For example, the MOSFET in Figure 3 can withstand 10 V and 85 A (850 W) for 1 ms. If this condition persists for a greater duration, the MOSFET will be destroyed. The TIMER circuit can ensure that the length of time the MOSFET is subject to these worst-case conditions is limited by the external TIMER capacitor. For example, if the TIMER was set to 1 ms and the current exceeded the limit for more than 1 ms, the circuit would time out and shut down the MOSFET.

In the ADM1177, to provide a margin of safety, the TIMER current-sense voltage activation threshold is set to 92 mV. The hot-swap controller will thus start timing the current conservatively as the sense voltage approaches the regulated value of 100 mV.

Design Example

Because of the flexibility permitted by the design of controllers like the ADM1177, it may be useful to demonstrate how one would be applied in a 12-V hot-swap design example. The following conditions are assumed for this example:

- Controller is the ADM1177
- V_{IN} = 12 V (±10%)
- V_{MAX} = 13.2 V
- I_{TRIP} = 30 A
- C_{LOAD} = 2000 µF
- V_{ON} = 10 V (a good supply level to switch on the controller)
- $I_{POWERUP}$ = 1 A (dc bias current required by the load during power-up)

To simplify this discussion, the calculations exclude the effects of component tolerances. These tolerances should of course be considered when designing for worst-case conditions.

ON Pin

Consider first the condition to *enable* the controller when the supply voltage exceeds 10 V. If the threshold of the ON pin is 1.3 V, the voltage-divider ratio from V_{IN} to the ON pin needs to be 0.13:1. For accuracy, the pin leakage current should be taken into account when selecting the resistance of the string.

A resistive divider consisting of 10-kΩ and 1.5-kΩ resistors will have a suitable ratio of 0.130.

Sense-Resistor Selection

The sense resistor is chosen based on the load current required to start the TIMER.

$$R_{SENSE} = \frac{V_{SENSETIMER}}{I_{TRIP}} = \frac{0.092\ \text{V}}{30\ \text{A}} \approx 3\ \text{m}\Omega$$

where $V_{SENSETIMER}$ = 92 mV.

The maximum power dissipated by the sense resistor at 30 A is

$$\begin{aligned} P_{RSENSE} &= I_{TRIP}{}^2 \times R_{SENSE} \\ &= (30\ \text{A})^2 \times 0.003\ \Omega \\ &= 2.7\ \text{W} \end{aligned}$$

So the sense resistor should be capable of dissipating 3 W. If a single resistor with the correct power rating or resistance is not available, the sense resistor can be made with multiple resistors.

Load Capacitance Charge Time

The time it takes to charge the load capacitance must be determined prior to selecting the MOSFET. During the *power-up* phase, the controller will usually hit the current limit due to the inrush current demanded by the load capacitance. If the time set by the TIMER pin is insufficient to allow the load capacitors to charge, then the MOSFET will be disabled and the system will not power up. We can use the following equation to determine the ideal value:

$$t_{CHARGE} = \frac{C_{LOAD} \times V_{MAX}}{\frac{V_{REGMIN}}{R_{SENSE}} - I_{POWERUP}}$$

$$= \frac{2000 \times 10^{-6}\ \text{F} \times 13.2\ \text{V}}{32.33\ \text{A} - 1\ \text{A}}$$

$$\approx 842\ \mu\text{s}$$

where V_{REGMIN} = 97 mV, the minimum regulation voltage of the hot-swap controller.

This equation assumes an ideal condition of load current ramping from 0 A to 30 A instantaneously. In reality, the gate charge, Q_{GS}, of larger MOSFETs serves to limit the slew rate of the gate voltage—and hence the power-up current profile—so that a quantity of charge is delivered to the load capacitor without triggering the TIMER function. In Figure 4, the MOSFET with the higher Q_{GS} results in the TIMER being active for a shorter period, $T1$ to $T3$, as compared to the MOSFET with the lower Q_{GS}, which causes the timer to be active during $T0$ to $T2$.

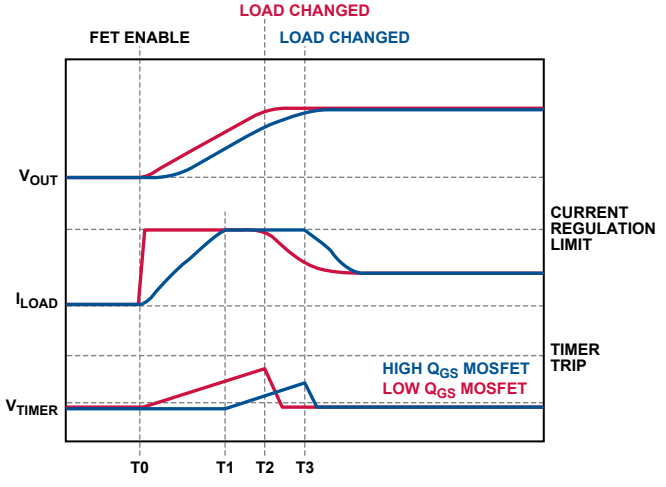


Figure 4. Effect of Q_{GS} on start-up profiles.

This is because the charge delivered between $T0$ and $T1$ accumulates at less than the current limit. Thus, the calculated time required can be reduced accordingly. This amount is difficult to quantify; it depends on the controller gate current and MOSFET specification for gate charge and capacitances. Since it may account for as much as 30% of the total charge current in some cases, it needs to be considered, particularly in designs using large MOSFETs and high currents.

For designs using MOSFETs with lower gate charge, a fast gate ramp can be assumed. This will result in a fast ramp from 0 A to I_{TRIP}, which may cause unwanted transients; in this case, *soft start* should be used.

Soft Start

With soft start, the inrush current is linearly ramped from zero to full scale over a period of time set by the SS capacitor. This will provide an inrush ramp that avoids the sudden impact of the 30-A limit, and is accomplished by ramping up the reference current. Note that the current is in regulation during the SS event, and therefore the TIMER is active from the moment the soft start begins, as can be seen in Figure 5.

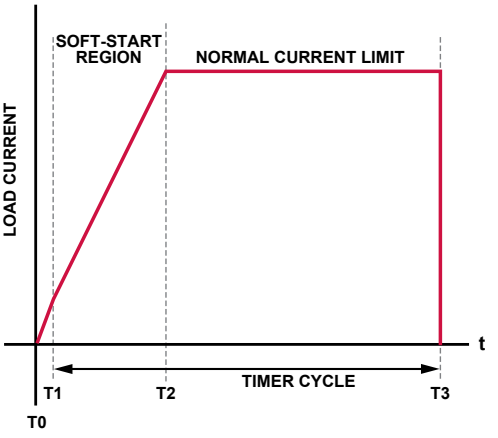


Figure 5. Soft-start effect on TIMER.

Therefore, a soft-start time of no more than 10% to 20% of the total TIMER is recommended. For this example, we can choose a time of 100 µs. The SS capacitance value can be determined as follows:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{SS}}$$

$$= \frac{\left(100 \times 10^{-6}\ \text{s}\right) \times \left(10 \times 10^{-6}\ \text{A}\right)}{1\ \text{V}}$$

$$= 1\ \text{nF}$$

where I_{SS} = 10 µA and V_{SS} = 1 V.

MOSFET and TIMER Selection

The first step to choosing a suitable MOSFET is to select the V_{DS} and I_D criteria. For a 12-V system, V_{DS} should be 30 V or 40 V to handle transients that could destroy the MOSFET. The I_D of the MOSFET should be much larger than the required maximum (see the SOA graph in Figure 3). In high-current applications, one of the most important specifications will be the MOSFET's R_{DSON}. Low values of this parameter will ensure that minimum power is lost in the MOSFET when it is fully enhanced in normal operation—and that minimal heat is generated at full load.

Thermal and Power Considerations

Before considering the SOA specifics and TIMER selection, the power dissipation of the MOSFET at full dc load needs to be considered because overheating must be avoided. As the temperature of the MOSFET increases, its power rating is reduced, or *derated*. In addition, running MOSFETs at high temperatures decreases their life span.

Recall that the hot-swap controller initiates the TIMER at a minimum sense voltage of 92 mV. For this calculation, we need to know the maximum possible dc current that can flow without tripping the TIMER. Assume the worst-case V_{REGMIN} of 97 mV. Then,

$$I_{MAXDC} = \frac{V_{REGMIN}}{R_{SENSE}} = \frac{0.097\ \text{V}}{0.003\ \Omega} = 32.33\ \text{A}$$

Assuming that the MOSFET's maximum R_{DSON} is 2 mΩ, the power is

$$\begin{aligned} P_{MOSFET} &= I_{MAXDC}{}^2 \times R_{DSON} \\ &= (32.33\ \text{A})^2 \times 0.002\ \Omega \\ &\approx 2.1\ \text{W} \end{aligned}$$

The MOSFET's thermal resistance at ambient temperature will be specified in the data sheet. The footprint size and additional copper will have an effect on this value. Assume

$$R_{thJA} = 60°\text{C/W}$$

As the MOSFET is required to dissipate 2.1 W, a worst-case temperature rise of 126°C above ambient can be expected:

$$T_{RISE} = R_{thJA} \times P_{MOSFET} = 126°\text{C}$$

One way to reduce this number is to use two or more MOSFETs in parallel. This will effectively reduce the R_{DSON} and thus the power dissipation in the MOSFETs. With two MOSFETs, a maximum temperature rise of 32°C per MOSFET will be incurred, assuming current is divided evenly between the devices (some tolerance should be allowed). The following shows the power in each MOSFET:

$$\begin{aligned} P_{MOSFET} &= \left(\frac{I_{MAXDC}}{number\ of\ MOSFETs}\right)^2 \times R_{DSON} \\ &= \left(\frac{32.33\ \text{A}}{2}\right)^2 \times 0.002\ \Omega = 0.5227\ \text{W} \end{aligned}$$

$$T_{RISE} = R_{thJA} \times P_{MOSFET} = 31.36°\text{C}$$

With this temperature rise and an assumed ambient temperature of T_A = 30°C, a maximum case temperature of 62°C can be expected for each MOSFET.

$$\begin{aligned} T_{MOSFET} &= T_{RISE} + T_A \\ &= 32°\text{C} + 30°\text{C} = 62°\text{C} \end{aligned}$$

MOSFET SOA Considerations

The next step is to review the SOA graphs to find a suitable MOSFET to handle worst-case conditions. In the worst-case short-circuit-to-ground condition, V_{DS} can be assumed to be the V_{MAX} of 13.2 V, as this will be the maximum voltage present across the MOSFET with its source terminal pulled to GND. In regulation, the worst case will be based on the maximum data sheet specification for the hot-swap controller regulation point. This is equal to 103 mV. The current can then be calculated as follows:

$$I_{MAX} = \frac{V_{REGMAX}}{R_{SENSE}} = \frac{0.103\ \text{V}}{0.003\ \Omega} = 34.33\ \text{A}$$

Before comparing this to the MOSFET SOA graphs, we need to consider the temperature derating of the MOSFET, since the SOA graph is based on data at ambient case temperature, T_C = 25°C. First calculate the power dissipation at T_C = 25°C:

$$P_{D25} = \frac{T_{J\,\max} - T_C}{R_{thJC}} = \frac{150°\text{C} - 25°\text{C}}{1.6°\text{C/W}} = 78.125\ \text{W}$$

where R_{thJC} is specified in MOSFET data sheet.

Now perform the same calculation for T_C = 62°C:

$$P_{D62} = \frac{T_{J\,\max} - T_C}{R_{thJC}} = \frac{150°\text{C} - 62°\text{C}}{1.6°\text{C/W}} = 55\ \text{W}$$

Thus, a derating factor of 1.42 is calculated as follows:

$$DF = \frac{P_{D25}}{P_{D62}} = \frac{78.125\ \text{W}}{55\ \text{W}} = 1.42$$

This needs to be applied to the SOA graph of the MOSFET in Figure 3. The diagonal lines that represent the time maximum power is applied need to be moved downward to reflect the adjusted power ratings.

We earlier used the 1-ms line as an example to illustrate how the curves work. For example, take a point on that line—say (20 A, 40 V); the power at that point is 800 W. Applying the derating formula:

$$P_{DERATED} = \frac{P_{ORIGINAL}}{DF} = \frac{800\ \text{W}}{1.42} = 563\ \text{W}$$

At 40 V, the corresponding current for derated power is 14 A. Plotting this point on the SOA graph establishes a point on the new 62°C-derated 1-ms line. New 10-ms and 100-µs lines can be established in the same way. The new lines are shown in red in Figure 6.

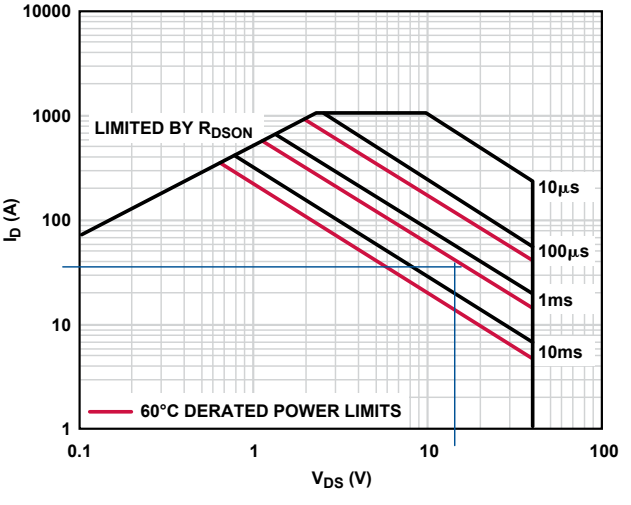


Figure 6. SOA plot including 62°C-derated power limits.

Selecting the TIMER Capacitor

The SOA's new derating lines can be used to recalculate the TIMER value. Draw a horizontal line from $I_{MAX} \approx 35$ A and a vertical line from $V_{MAX} = 13.2$ V (faint blue lines), then determine their intersection point with respect to the red lines. They indicate a time between 1 ms and 10 ms, perhaps ~2 ms. It is difficult to get figures exactly correct in a small region of a graph in log scale, so conservative choices should be made to ensure that adequate tolerance is applied—while considering the effects of these choices on other criteria such as performance and price.

Recall that the estimated time to charge the load was approximately 850 µs. As the soft-start time is established by a linear ramp, it takes longer (than with a step change) to charge the load capacitors. To estimate the total volume of charge, assume that half the SS time is to be added to the calculated time if using soft start; thus add half the SS time (50 µs) to 850 µs, resulting in a total time of approximately 900 µs. If the MOSFET chosen has a large gate charge (e.g., ≥80 nC), this may be further reduced, as discussed earlier. If the time to charge the load is less than the maximum SOA time, the MOSFET is suitable. In this case, the criterion is met (0.9 ms < 2 ms).

A TIMER value of less than 2 ms should be sufficient to protect the MOSFET—and greater than 0.9 ms to charge the load. If a conservative value of 1 ms is selected, the capacitance can be calculated as follows:

$$C_{TIMER} = \frac{t_{TIMER} \times I_{TIMER}}{V_{TIMER}}$$

where $I_{TIMER} = 60$ µA and $V_{TIMER} = 1.3$ V,

$$C_{TIMER} = \frac{\left(1 \times 10^{-3}\,\text{s}\right) \times \left(60 \times 10^{-6}\,\text{A}\right)}{1.3\,\text{V}}$$

$$\approx 47\,\text{nF}$$

When using paralleled MOSFETs, the calculations for TIMER selection will not change. It is critical that the TIMER and short-circuit protection be designed with a single MOSFET in mind. The reason is that the V_{GSTH} can differ significantly among a population of MOSFETs, so a single MOSFET may be required to handle a large proportion of current during regulation.

Hot-Swap Design Complete

The hot-swap design with paralleled MOSFETs can be seen in Figure 7 with the correct component values. The ADM1177 hot-swap controller performs additional functions. It has an integrated on-chip ADC that can be used to translate the supply voltage and load current into digital data—which can be read out through the I²C® bus, providing a fully integrated current- and voltage-monitoring function.

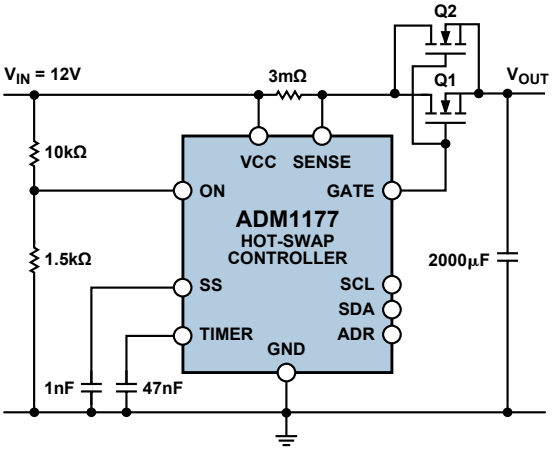


Figure 7. Completed reference design.

THE AUTHOR

Marcus O'Sullivan [marcus.osullivan@analog.com] has been with Analog Devices for over eight years. An applications engineer in the Power Management Group, based in Limerick, Ireland, he holds a BEng degree in electronic engineering from the University of Limerick. Joining ADI after graduation in 1999, he worked as a test-development engineer until 2004, when he took up his current role as applications engineer.

REFERENCES—VALID AS OF JUNE 2008

[1]www.en.wikipedia.org/wiki/hot_swapping
[2]ADI website: www.analog.com (Search) hot swap (Go)
[3]ADI website: www.analog.com (Search) ADM1177 (Go)

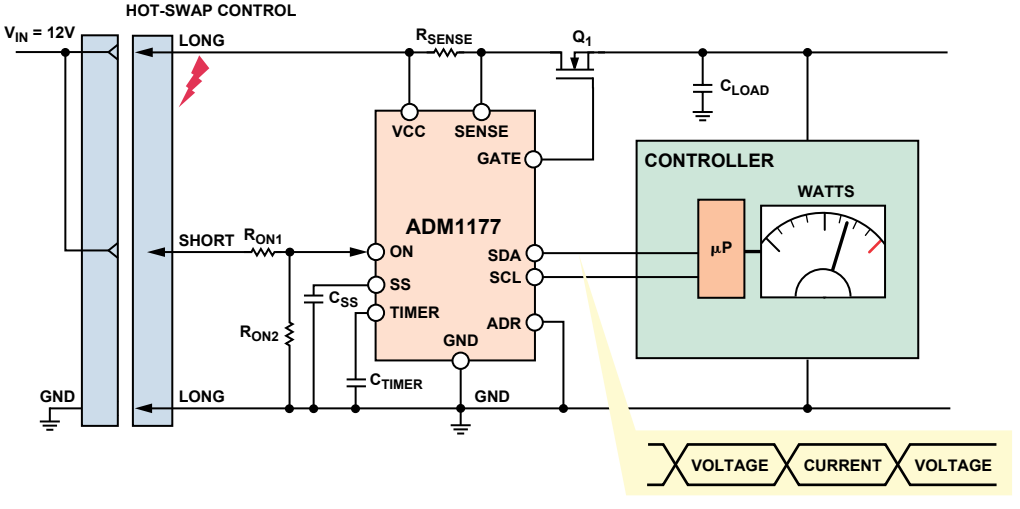


Figure 8. Hot swap with I²C digital power monitoring.

Discrete- and Integrated Control of Power Amplifiers in Base-Station Applications

By Liam Riordan

INTRODUCTION

In wireless base stations, the power amplifier (PA) dominates signal-chain performance in terms of power dissipation, linearity, efficiency, and cost. Monitoring and controlling the performance of a base station's PA makes it possible to maximize the output power while achieving optimum linearity and efficiency. This article discusses the elements of a monitoring-and-control solution for the PA using discrete components—and describes an integrated solution.

Analog Devices has a suite of components that are ideally suited to such tasks. Multichannel digital-to-analog converters (DACs), analog-to-digital converters (ADCs), temperature sensors, and current-sense amplifiers, as well as single-chip integrated solutions, are being applied in base stations to monitor and control a variety of analog signals. Discrete sensors and data converters provide maximum performance and configuration flexibility, while integrated solutions offer lower cost, smaller size, and higher reliability.

Optimizing a base station's power efficiency is a key environmental consideration for companies in the telecom industry. Significant efforts are being made to reduce the overall energy consumption of base stations to lessen their impact on the environment. Electrical energy is the principal source of everyday operating costs in a base station, and the PA can be responsible for more than half of the power dissipation. Thus, optimizing the PA's power efficiency improves operational performance, and provides environmental and financial benefits.

PA Control with Discrete Components

Figure 1 shows a basic power stage using a lateral-diffused metal-oxide semiconductor (LDMOS) transistor. The inherent trade-offs between linearity, efficiency, and gain determine the optimum bias condition for the PA transistor. Maintaining the drain bias current at an optimum value over temperature and time can significantly improve the overall performance of the PA, while ensuring that it stays within regulated output power levels. One way of controlling the gate bias current is to use a resistive divider to set the gate voltage at a fixed optimum value determined during evaluation.

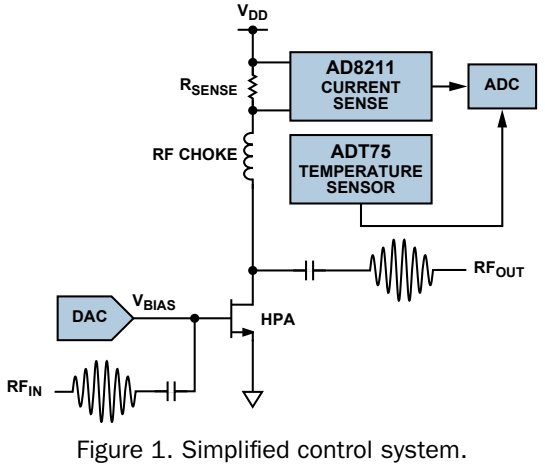


Figure 1. Simplified control system.

Unfortunately, while this fixed-gate-voltage solution can be quite cost effective, it has a serious disadvantage: it does not correct for environmental changes, manufacturing spread, or supply-voltage variations. The two principal factors affecting the PA's drain bias current are variations of the high-voltage supply line and the on-chip temperature.

A better approach is *dynamic control* of the PA gate voltage— using a digital control algorithm to measure the drain current, digitizing it with an ADC, and setting the required bias via a high-resolution DAC or a lower-resolution digital potentiometer. This control system allows the PA to maintain the required bias condition for optimized performance—set by a user-programmable setpoint—despite changes in voltage, temperature, and other environmental parameters.

A key factor in this control approach is accurate measurement of the current furnished to the LDMOS transistor via the high-voltage supply line, using a high-side sensing resistor and an AD8211[1] current-sense amplifier. With a common-mode input range up to +65 V, the AD8211 provides a fixed gain of 20 V/V. The external sense-resistance sets the full-scale current reading. The amplifier output can be multiplexed into an ADC to generate digital data for monitoring and control. Care should be taken to ensure that the output voltage of the current-sense amplifier be as close as possible to the full-scale analog input range of the ADC. Constant monitoring of the high-voltage line enables the power amplifier to continuously readjust its gate voltage, even when voltage surges are sensed on the line, thus maintaining an optimum bias condition.

The drain-to-source current of the LDMOS transistor, I_{DS}, as a function of the gate-to-source voltage, V_{gs}, has two temperature-dependent terms: the effective electron mobility, μ, and the threshold voltage, V_{th}.

$$I_{DS} = \frac{\mu(T) C_{OX} W}{2L} (V_{gs} - V_{th}(T))^2$$

V_{th} and μ decrease with increasing temperature. Hence, temperature changes will cause variations in output power. Measuring ambient and internal temperatures of the PA using one or more ADT75[2] 12-bit temperature sensors makes it possible to monitor the temperature variations on the board. The ADT75, a complete temperature monitoring system in an 8-lead MSOP package, offers ± 1°C accuracy from 0°C to 70°C.

Multiplexing the voltage output of the temperature sensor, the drain current, and other data into an ADC allows temperature measurements to be converted into digital data for monitoring. Depending on the system configuration, it may be necessary to use a number of temperature sensors on the board. For example, if more than one PA is used—or if more than one predriver is required on the front end—a temperature sensor for each amplifier permits better control of the system. For monitoring both the current sensors and the temperature sensors, the AD7992,[3] AD7994,[4] and AD7998[5] multichannel 12-bit ADCs are useful for converting analog measurements into digital data.

The digital information gathered from the current sensors and temperature sensors can be continuously monitored, using control logic or a microcontroller. Dynamic control of the PA gate voltage with a digital potentiometer or DAC—while monitoring the sensor readings and processing the digital data—allows an optimized biased condition to be maintained. The degree of control required on the gate voltage will determine the resolution of the DAC. Telecom companies commonly use multiple PAs in base-station designs, as shown

in Figure 2, to provide added flexibility in selecting a PA for each RF carrier and allow each PA to be optimized toward a particular modulation scheme. Also, combining parallel PA outputs provides improved linearity and overall efficiency. In such cases, the PAs may require multiple cascaded gain stages, including variable-gain amplifiers (VGAs) and predrivers, to meet the gain and efficiency requirements. A multichannel DAC can accommodate the various level-setting- and gain-control requirements of these blocks.

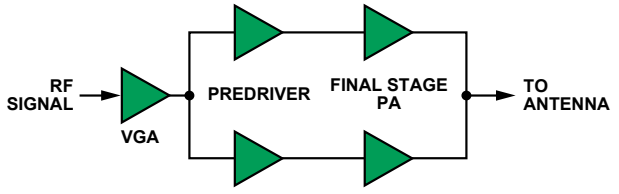


Figure 2. Typical high-power-amplifier signal chain.

To achieve accurate PA gate control, the AD5622,[6] AD5627,[7] and AD5625[8] DACs offer 12-bit, single, dual, and quad outputs, respectively. They have internal buffers with excellent source- and sink capabilities, obviating the need for external buffers in most applications. The combination of low power, guaranteed monotonicity, and fast settling time make these parts ideal for accurate level-setting applications.

Where precision is not a primary specification and 8-bit resolution is acceptable, a digital potentiometer is a more cost-effective option. These digitally variable resistors perform the same electronic adjustment functions as mechanical potentiometers or variable resistors—but with enhanced resolution, solid-state reliability, and superior temperature performance. Nonvolatile and *one-time-programmable* (OTP) digital potentiometers are ideal in *time-division duplexing* (TDD) RF applications where the PA is turned off for the TDD *receive* period and turned on by a fixed gate voltage for the *transmit* period. This preprogrammed start-up voltage reduces the turn-on delay and improves efficiency in turning on the PA transistor for the *transmit* stage. The ability to turn off the PA transistor during the *receive* state prevents transmitter-circuit noise from corrupting the received signal and improves the overall efficiency of the PA. Depending on the number of channels, interface type, resolution, and the requirement for nonvolatile memory, a variety of digital potentiometers are available for this application. For example, the 256-position AD5172,[9] a one-time-programmable, dual-channel, I^{2}C-compatible potentiometer, is well-suited for level-setting applications in RF amplifiers.

For monitoring and controlling gain with optimum linearity and efficiency, accurate measurement of the power levels of complex RF signals on the output of the PA is necessary. The AD8362[10] TruPwr™ rms power detector provides 65-dB dynamic range from 50 Hz to 3.8 GHz, allowing precise rms power measurement of RF signals typically found in W-CDMA, EDGE, and UMTS cellular base stations.

In Figure 3, the output of the power detector, V_{OUT}, is connected to the gain-control terminal of the PA to adjust its gain. The PA output drives the antenna; the directional coupler picks up a fraction of the output, attenuates it appropriately, and applies it to the power detector. The output of the power detector, an rms measure of the transmitter output signal, is compared with the value programmed by the DAC, V_{SET}; and the PA gain is adjusted to null difference. Thus, V_{SET} sets the power gain precisely. The output of the ADC, a digital measure of V_{OUT}, feeds into a larger feedback loop, which can track the transmitted power output, as measured by the AD8362, establishing the value of V_{SET} and the system-determined gain requirement.

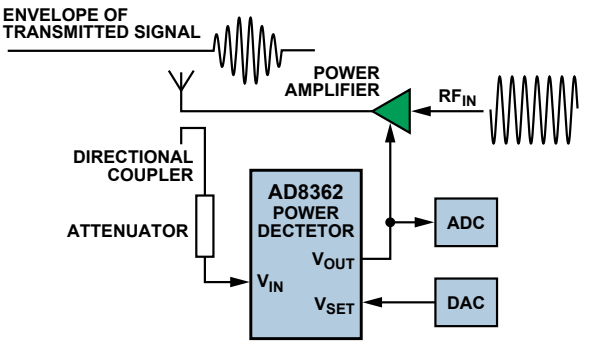


Figure 3. Power throughput detection.

This method of gain control can be used with variable-gain amplifiers (VGAs) and variable-voltage amplifiers (VVAs) that are used in preceding stages of the signal chain. To measure both *transmit*- and *receive* power, the AD8364[11] *dual* detector simultaneously measures two complex input signals. In a system where a VGA or a predriver precedes the PA, and only one power detector is required, the gain on one of the devices is fixed, while V_{OUT} feeds the control input of the other.

If the loop determines that the line current is too high, it sends a command to the DAC to reduce the gate voltage or shut down the part. In some applications, however, if voltage spikes or unacceptably high currents appear on the high-voltage supply line, the digital control loop cannot sense the high-side current, convert the signal to digital, and process the digital data by the external control logic rapidly enough to prevent device damage.

In an analog approach, an ADCMP371[12] comparator and an RF switch can be used to control the RF signal to the PA, as shown in Figure 4. The output voltage of the current sense is directly compared to the fixed voltage set up by the DAC. When a voltage higher than the fixed voltage appears at the output of the current sensor, due to a voltage or current spike, the comparator can toggle a control pin on the RF switch, cutting the RF signal to the gate of the PA almost instantaneously, preventing damage to the PA. This direct control, which bypasses the digital processing, is much faster and provides better protection.

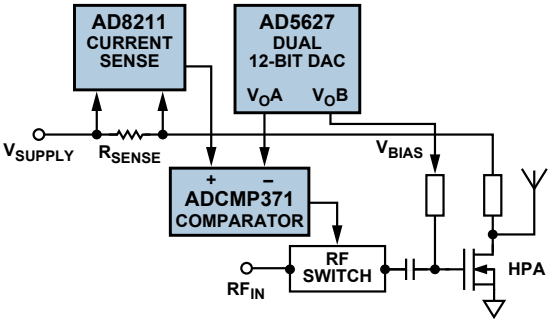


Figure 4. Control-loop protection using an analog comparator.

Combining the elements discussed above, a typical PA monitoring and control configuration, made up of discrete devices, is shown in Figure 5. In this case, the only amplifier being monitored and controlled is the PA itself, but a similar principle would apply to control of any of the amplifiers in the signal chain. All the discrete components are controlled using one master controller and operate off the same I^{2}C bus.

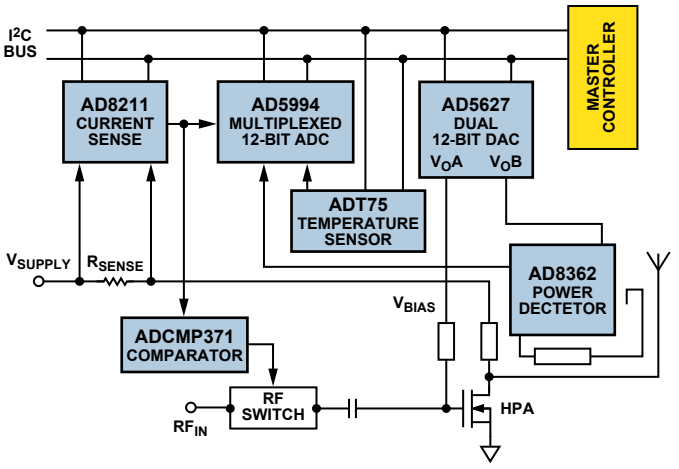


Figure 5. Monitoring and control of a PA with discrete devices.

Depending on the requirements of the signal chain, a number of amplifiers may be needed in the predrive and final stages to increase the overall power gain of the signal ahead of the antenna. Unfortunately, these additional power-gain stages have an adverse effect on the overall efficiency of the PA. To minimize the degradation of the PA's efficiency, the drivers must be monitored and controlled to optimize performance. For example, the user would require a significant number of discrete components to monitor temperature, power, and voltage levels on the VGA, two predrivers, and two final-stage PAs used to gain up the signal in Figure 2.

Integrated Monitoring and Control

To solve this proliferation problem, Analog Devices developed the AD7294,[13] an integrated monitoring and control solution specifically designed to address this issue. The AD7294 contains all the functions and features required for general-purpose monitoring and control of current, voltage, and temperature—integrated onto a single chip.

The AD7294 consists of a 9-channel, 12-bit ADC and a 4-channel DAC with a sink/source capability of 10 mA. It is manufactured on 0.6-μm DMOS technology, which permits the current sensor to measure common-mode levels up to 59.4 V. The ADC has two dedicated current-sense channels, two channels for sensing external-junction temperatures, one channel for sensing the chip's internal-temperature, and four uncommitted ADC inputs for general-purpose monitoring.

The ADC channels have the added benefit of *hysteresis* and *high-* and *low-limit* registers (which can also be found on the AD7992/AD7994/AD7998). The user can preprogram high- and low limits for an ADC channel; the monitored signal will flag an alert if these limits are violated. The hysteresis register gives the user the added capability of determining the reset point for the alert flag if a limit violation occurs. Hysteresis prevents a noisy temperature- or current-sensor reading from continuously toggling the alert flag.

Analog-to-digital conversions can be initiated in two different ways. The *command* mode allows the user to convert a single channel or a sequence of channels on demand. The *autocycle* mode converts automatically on a sequence of preprogrammed channels, an ideal mode of operation for system monitoring—especially for continuously monitoring signals, such as signal power and current sensing—and provides alerts only when the preprogrammed high- or low limits are violated.

Two bidirectional high-side current-sense amplifiers are provided (Figure 7). As the PA drain current flows through a shunt resistor, the small differential input voltage is amplified. The integrated current-sense amplifiers reject common-mode voltages up to 59.4 V and provide an amplified analog signal to one of the multiplexed ADC channels. Both current-sense amplifiers have a fixed gain of 12.5 and utilize an internal 2.5-V output-offset reference. An analog comparator is provided with each amplifier for fault detection above a threshold of 1.2× full-scale voltage.

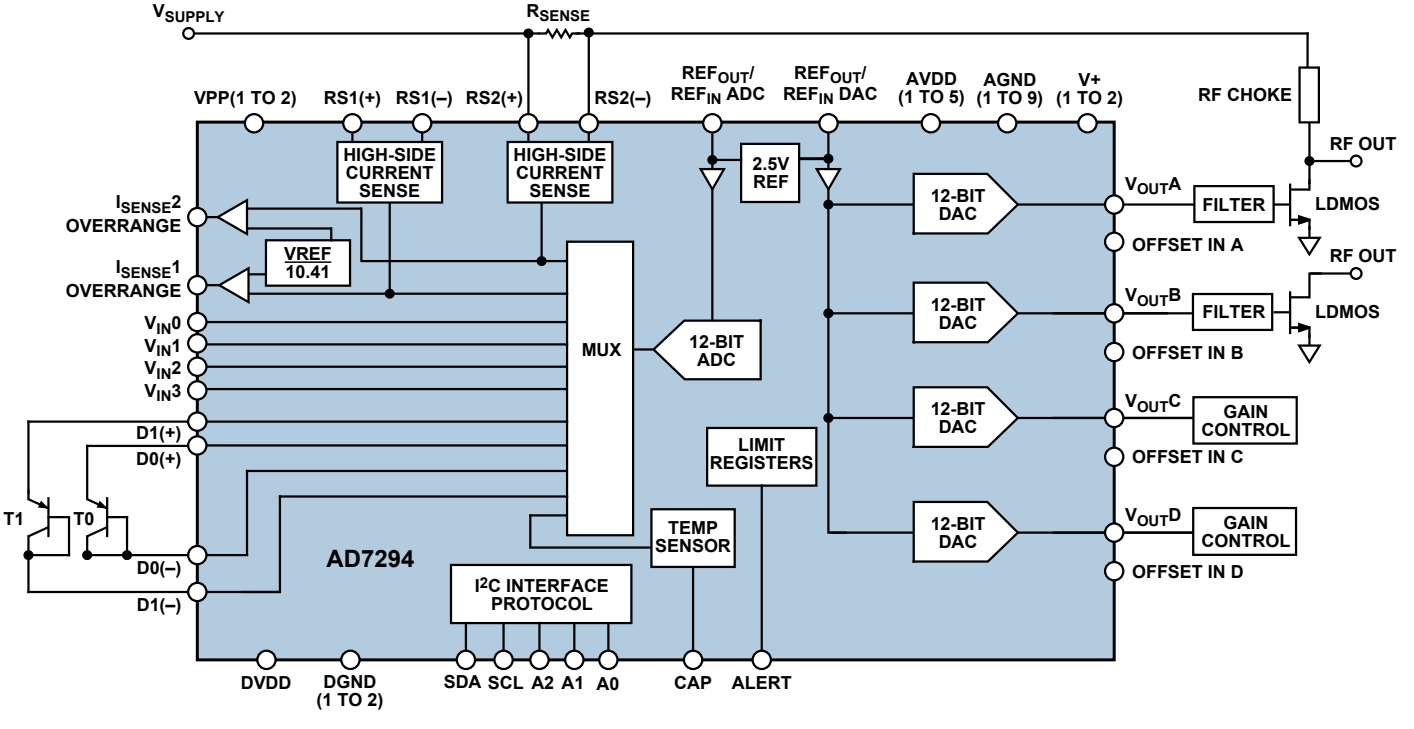


Figure 6. Integrated solution for monitoring and controlling PA stages.

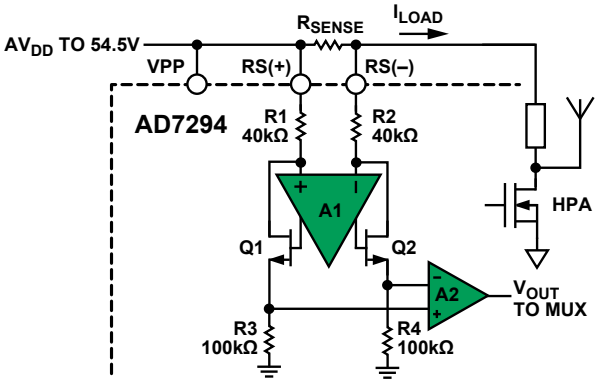


Figure 7. AD7294 high-side current-sense detail.

The four 12-bit DACs provide a digitally controlled voltage (with 1.2-mV resolution) to control the bias currents of the power transistors. They can also be used to provide control voltages for variable-gain amplifiers. The DAC core is a thin film, 12-bit, inherently monotonic string DAC with a 2.5-V reference and 5-V output span. Its output buffer drives the high-voltage output stage. The output range of the DAC, which is controlled by the offset input, can be positioned between 0 V and 15 V. This provides the end user the option of 12-bit-accurate control over a 5-V span, while allowing the flexibility of using bias voltages as high as 15 V, as PA transistors migrate to larger controlling-gate voltages. In addition, the ability of the four DACs to sink or source currents up to 10 mA makes external drive buffers unnecessary.

CONCLUSION

PA vendors are designing ever more complex PA front-end signal chains using a diversity of gain stages and control techniques. Available families of multichannel ADCs and DACs and analog RF components are ideally suited to address differing system partitions and architectures, allowing designers to implement cost-effective distributed control. Alternatively, single-chip solutions, such as the AD7294, provide significant advantages in terms of board area, system reliability, and cost. From a custom design perspective, the wealth of both dedicated-function- and integrated-system building blocks offer unprecedented empowerment to system designers.

REFERENCES—VALID AS OF JUNE 2008

[1] ADI website: www.analog.com (Search) AD8211 (Go)
[2] ADI website: www.analog.com (Search) ADT75 (Go)
[3] ADI website: www.analog.com (Search) AD7992 (Go)
[4] ADI website: www.analog.com (Search) AD7994 (Go)
[5] ADI website: www.analog.com (Search) AD7998 (Go)
[6] ADI website: www.analog.com (Search) AD5622 (Go)
[7] ADI website: www.analog.com (Search) AD5627 (Go)
[8] ADI website: www.analog.com (Search) AD5625 (Go)
[9] ADI website: www.analog.com (Search) AD5172 (Go)
[10] ADI website: www.analog.com (Search) AD8362 (Go)
[11] ADI website: www.analog.com (Search) AD8364 (Go)
[12] ADI website: www.analog.com (Search) ADCMP371 (Go)
[13] ADI website: www.analog.com (Search) AD7294 (Go)

THE AUTHOR

Liam Riordan [liam.riordan@analog.com] joined Analog Devices in 2004 and works in the Precision Converters Applications Group in Limerick, Ireland. He graduated with a BEng in electrical and electronic engineering from University College, Cork.

PRODUCT INTRODUCTIONS: VOLUME 42, NUMBER 2

Data sheets for all ADI products can be found by entering the model number in the search box at www.analog.com.

April

Clock- and Data-Recovery, 1.25-Gbps **ADN2805**
Codec, Audio, high-definition audio **AD1984B**
Codecs, Audio, low-power **SSM2602/SSM2603**
Driver, Line, quad LVDS **ADN4667**
Gyroscope, yaw-rate **ADXRS613**
Inclinometer/Accelerometer, two-axis **ADIS16209**
Processor, Audio, advanced TV **ADAV4622**
Receiver, Line, quad LVDS **ADN4668**
Sensor, Inertial, high-precision, three-axis **ADIS16355**
Switches, *i*CMOS, SPST, low capacitance **ADG1201/ADG1202**
Transceiver, high-performance, ISM band **ADF7021-N**

May

Amplifier, Audio, 2-W, Class-D **SSM2305**
Amplifier, Audio, 3-W, Class-D **SSM2315**
Codec, Audio, high-definition audio **AD1883**
Codecs, Audio, high-definition audio **AD1884A/AD1984A**
DAC, Voltage-Output, 16-bit, 40-channel **AD5370**
Demodulator, Quadrature, 700 MHz to 2.7 GHz **ADL5382**
Driver, Half-Bridge, isolated **ADuM5230**
Monitor, Voltage, 4-channel, 0.8% accuracy **ADM1184**
Processor, Audio, advanced TV **ADAV4601**
Processor, SHARC, 32-/40-bit floating-point **ADSP-21375**
Switch, *i*CMOS, SPDT, low capacitance **ADG1219**

June

ADC, Successive-Approximation, dual, 14-bit, 1-MSPS **AD7264**
Amplifier, Audio, 3-W, Class-D, ALC **SSM2317**
Amplifier, Operational, dual, rail-to-rail **AD8639**
Amplifier, Operational, high-speed, low distortion **ADA4898**
Amplifier, Operational, high-speed, low distortion **ADA4857**
Converters, Capacitance-to-Digital, 12-bit **AD7152/AD7153**
Driver, ADC, differential, low distortion **ADA4939**
Equalizer, CX4, 4-channel, bidirectional, 3.75 Gbps **ADN8102**
Isolators, Digital, 4-channel, integrated 500-mW dc-to-dc **ADuM540x**
Modulator, Sigma-Delta, isolated **AD7400A**
Monitors/Sequencers, Voltage, 4-channel, ±0.8% accuracy **ADM1186-x**
Sensor, Battery, 12-V, automotive **ADuC7034**
Switch, CMOS, dual SPDT, 0.5-Ω on resistance ... **ADG824**
Switch, HDMI/DVI, 2:1, equalization, DDC/CEC buffers **AD8192**
Switches, *i*CMOS, quad SPST, 1.5-Ω on resistance **ADG141x**
Transceiver, on-chip driver amplifier, digital VGA **AD8260**
Transmitter, HDMI/DVI, consumer electronic control **ADV7520**

This article is available in HTML and PDF at *www.analog.com/analogdialogue*. Click on *archives*, then select volume, number, and title.

From the Back Burner

Open-Loop Calibration Techniques for Digital-to-Analog Converters

By Ken Kavanagh [ken.kavanagh@analog.com]

In principle, you give a digital input to a DAC and it provides an accurate output voltage. In reality, the accuracy of the output voltage is subject to gain and offset errors from the DAC and other components in the signal chain. The system designer must compensate for these errors in order to get an accurate output voltage. This can be implemented with external components and post-manufacture trimming. Digital calibration modifies the input sent to the DAC such that the gain and offset errors are taken into account; thus removing the need for external components and trimming.

Performing these calculations in a DSP or microprocessor requires additional overhead that can be costly and time consuming. Some DACs include on-chip registers that allow the calculations to take place in the DAC, freeing the processor to carry out other functions. The AD536x, AD537x, AD538x, and AD539x families of *dense*DAC™ multichannel DACs have eight to 40 channels with 12-bit to 16-bit resolution. Single-supply versions can produce 5-V outputs. Dual-supply versions can produce ±10-V outputs. Each device has dedicated *m* and *c* registers for each channel, allowing per-channel gain and offset calibration.

Figure 1 shows one channel of the AD5370 16-bit, 40-channel DAC. Calculating the values for *m* and *c* registers is described in the following steps:

1. Measure the offset and full-scale errors by setting the DAC input to zero and full scale.
2. Calculate the actual LSB size by dividing the span by the number of possible codes (65,536 in this case).
3. Subtract the number of LSBs corresponding to the excess span from the default *m* register value. For example, an excess span of 50 mV in a 10 V range corresponds to 326 LSBs.
4. Add the number of LSBs corresponding to the offset to the default *c* register value. For example, an offset of –10 mV is 65 LSBs.

The DAC can now be treated as if it were ideal and will calculate appropriate value to compensate for internal and system errors.

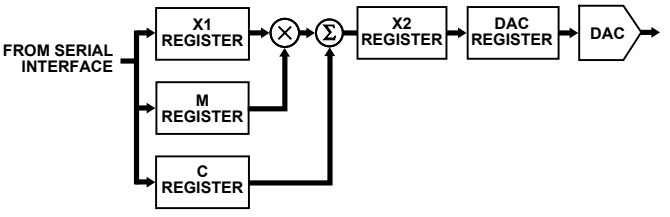


Figure 1. Single channel of AD5370 DAC.

AC Shield Enhances Remote Capacitive Sensing

By Kevin Staunton [kevin.staunton@analog.com]

Capacitive sensing user interfaces are desirable features for the latest consumer electronic products; from cell phones to media players to satellite navigation systems, the trend to enhance the human interface is evolving. The principle of a user touch causing a change in capacitance to activate a switch is well understood, but implementing a PCB sensor design with proper shielding and routing poses a challenge for hardware designers.

The change in capacitance in response to a finger touch is only a fraction of a picofarad, so tiny parasitic capacitances seen by the sensor or sensor traces reduce the dynamic range of the capacitive sensor controller. In addition, inadequate sensor shielding can present coupling paths that create a noisy response, degrading the SNR achievable by the sensor and decreasing the resolution of the user interface. Designed for use with single-electrode capacitance sensors implementing functions such as buttons, scroll bars, and wheels, the AD7147 CapTouch™ controller provides an active AC_{SHIELD} signal that minimizes the problem of parasitic capacitance, remote sensor connection, sensor routing, and shielding of the capacitive sensors.

A common configuration for capacitive sensing is to have the sensor controller on the main board, with the sensors patterned on a separate sensor board, as shown in Figure 1.

The sensor board is often connected to the main board by a cable. This separation prevents high-speed signals from coupling onto the capacitive sensors and reduces the large parasitic capacitance caused by ground planes. In addition, the sensors are the human interface, and sometimes must be remote from the main board. The sensors can be implemented on FR4 or ultrathin transparent ITO material.

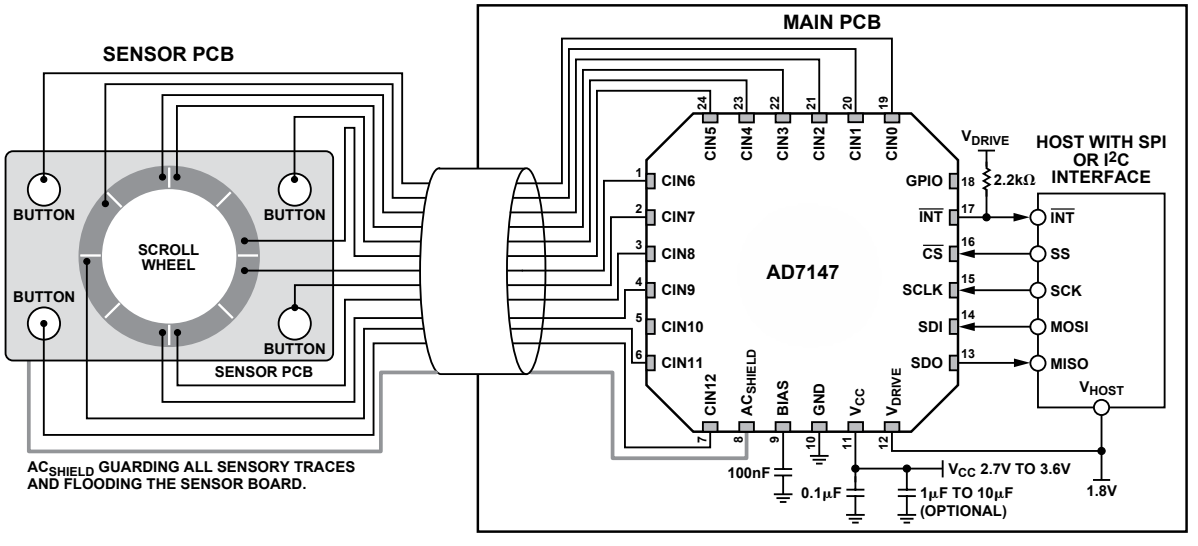


Figure 1. Typical configuration has a controller on the main board with sensors patterned on a separate board.

The AD7147 works by alternately switching the capacitive sensor between an excitation signal and a capacitance-to-digital converter (CDC), as shown in Figure 2.

The advantage of the AC_{SHIELD} signal is that the sensors and the sensor traces can be shielded by a signal that is in phase with the excitation on the sensors. Eliminating the potential between shield and sensor/sensor-traces also eliminates the capacitance. Therefore, to minimize parasitic capacitance and noise coupling, the AC_{SHIELD} signal can be flooded on the sensor board and used as a guard signal along all sensor traces. Use of the AC_{SHIELD} signal in the AD7147 allows a separation of up to 60 cm between controller and sensor(s).

Analog Devices provides a complete solution in capacitive sensing, including the controller, evaluation tools, sensor design libraries, and software for the host microcontroller.

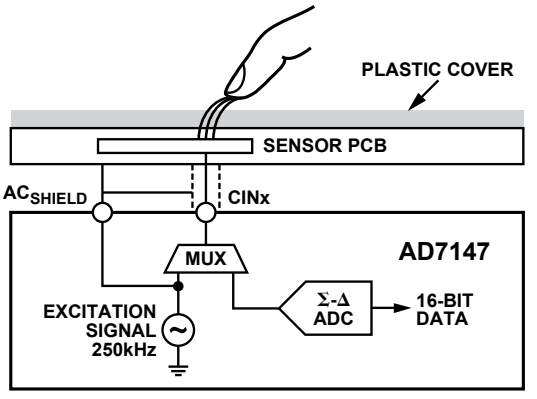


Figure 2. AC_{SHIELD} eliminates capacitance between the sensors and the shield.

Inexpensive High-Speed Amplifiers Make Flexible Clock Buffers

By John Ardizzoni [john.ardizzoni@analog.com]

In consumer electronic applications, which tend to be lower in frequency and less demanding than typical clock buffering applications, inexpensive high-speed op amps (~100 MHz bandwidth) can offer an attractive alternative to traditional clock buffers. High-speed amplifiers can be less expensive than traditional clock buffers, yet they can accommodate a wide range of design configurations.

The ADA4850 (ADA4850-1/ADA4850-2), ADA4851 (ADA4851-1/ADA4851-2/ADA4851-4), ADA4853 (ADA4853-1/ADA4853-2/ADA4853-3) and AD8061 single-supply op amps are excellent choices for low-cost clock buffers. These amplifiers all feature low supply voltage, low supply current, a power-down mode for power-sensitive applications, and rail-to-rail outputs, which enable wide dynamic range.

One advantage of an op amp vs. a traditional clock buffer is flexibility. Op amps allow clock pulses to be buffered, amplified, offset, inverted, summed, subtracted, or filtered. They provide high input impedance, low input bias current, low supply current, independent power-down (for multiple amplifiers in a single package), low output impedance, and low propagation delay.

Designers must recognize and adhere to some operating constraints when using op amps in clock buffer applications. For example, voltage feedback amplifiers specify a gain bandwidth product. As the closed-loop gain of the amplifier circuit increases, its bandwidth decreases. Large gains therefore mean less bandwidth. Cascading multiple amplifers, each with lower gain, allows the amplifier to operate at a higher bandwidth, preserving the overall gain and bandwidth of the signal path.

Single-supply operation is important for portable electronics. By definition, the input common-mode range of a single-supply op amp includes the negative rail (ground); most can go 200 mV below ground. This doesn't mean that the output can swing below ground, however. The output stage of typical rail-to-rail amplifiers uses a common emitter configuration. Therefore, the closest the output can come to the rail is V_{ce} (sat), which can range from tens of millivolts to hundreds of millivolts, depending on the output load.

Fortunately, in these applications, the output does not usually have to swing all the way to ground. When the input gets too close to ground, however (around 100 mV to 200 mV), the output stage can saturate, introducing distortion and long recovery times. In dc-coupled systems, keep the *low* of the signal above 200 mV or use a –200 mV negative supply voltage. Either method will prevent the output stage from going into saturation.

Amplifiers also specify headroom, or how close they can swing to the positive rail, so care must also be taken to address the high side of the input common-mode range as well. If the input voltage gets too high, the output stage will distort and cut off. The ADA4850 and ADA4851 require 2.2 V of headroom, the AD8061 requires 1.8 V, and the ADA4853 requires only 1.2 V.

Figure 1 shows a single-supply noninverting op amp clock buffer with a gain of +2. As configured, the upper limit for the AD8061 is about 33 MHz. Its 2-ns propagation delay is comparable to some dedicated clock buffers.

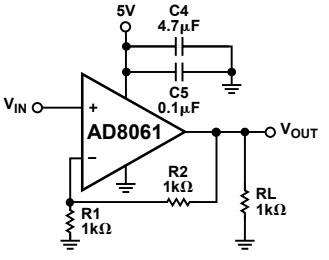


Figure 1. Noninverting op amp clock buffer.

In some applications, ac coupling can be used, allowing higher bandwidth amplifiers to be used for extended frequency performance. These amplifiers can be used in single-supply applications by biasing the amplifier inputs and outputs to midsupply.

Figure 2 shows a schematic using the AD8057 high-speed amplifier. Featuring 325-MHz bandwidth and 1150 V/µs slew rate, it is configured for unity gain. Note that the load resistor is returned to a voltage that is the dc average of the input signal. This ensures that the output will be referenced back to ground. The upper operating range of this configuration is approximately 100 MHz.

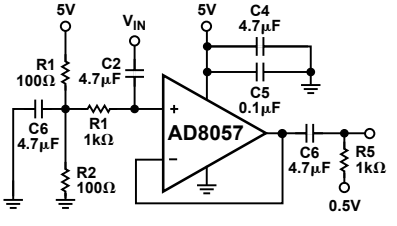


Figure 2. AC-coupled clock buffer (unity gain).

As shown, when a design calls for a clock buffer, a high-speed amplifier can often provide more flexibility at lower cost, enabling high-speed amplifiers to compete with traditional clock buffers in many applications. Either single- or dual-supply amplifiers can be used, depending upon the specific application.

Analog Devices, Inc.
Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA
02062-9106 U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
Analog Devices, Inc.
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia
Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

Printed in the U.S.A. M02000422-40-7/08

ANALOG DEVICES