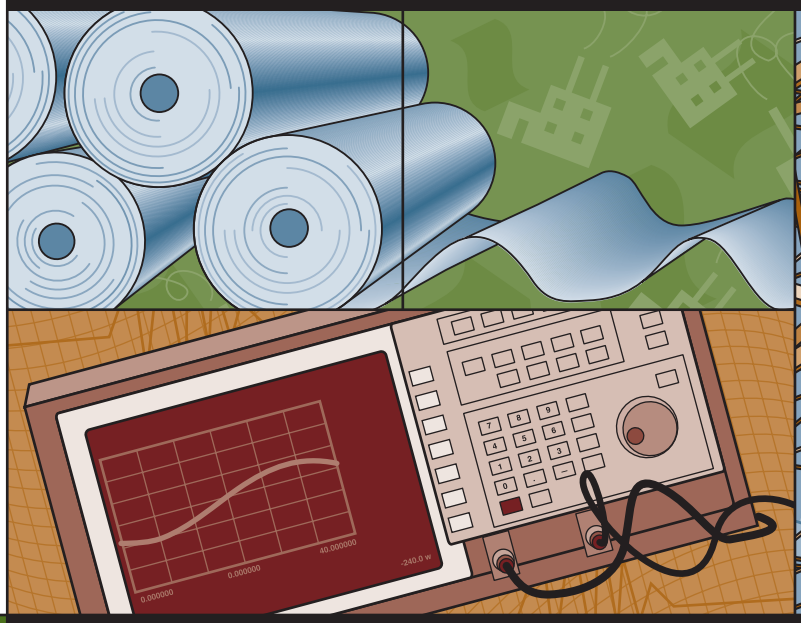
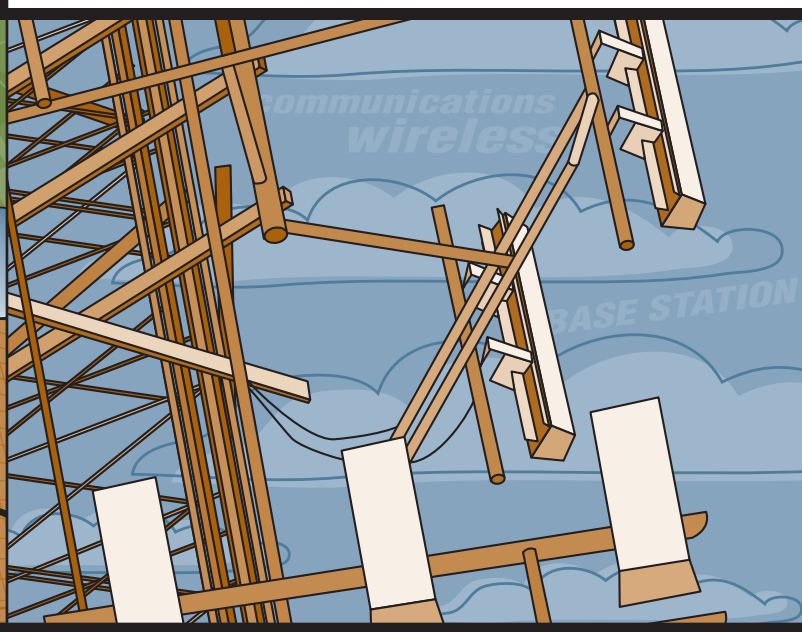
Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing





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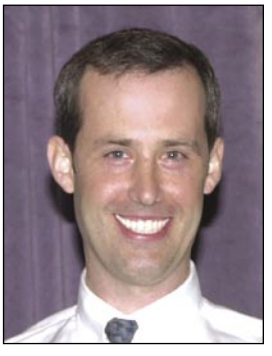
Editor's Notes

We are pleased to note the introduction of a new Fellow at our 2003 General Technical Conference. *Fellow*, at Analog Devices, represents the highest level of achievement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art. Their creative technical contributions in product or process technology, or software, will have led to commercial success with a major impact on the company's net revenues and earnings.

Attributes include roles as mentor, consultant, entrepreneur, organizational bridge, teacher, and ambassador. Fellows must also be effective leaders of teams—and in perceiving customer needs. In the year 2003, one individual—**Mike Judy**—was identified as having the rare combination of technical abilities, accomplishments, and personal qualities to qualify him to enhance our existing roster of Fellows: *Bob Adams* (1999), *Woody Beckford* (1997), *Derek Bowers* (1991), *Paul Brokaw* (1979), *Lew Counts* (1983), *Larry DeVito* (2002), *Dennis Doyle* (2001), *Paul Ferguson* (2001), *Barrie Gilbert* (1979), *Roy Gosser* (1998), *Bill Hunt* (1998), *Josh Kablotsky* (2001), *Jody Lapham* (1988), *Chris Mangelsdorf* (1998), *Jack Memishian* (1980), *Doug Mercer* (1995), *Frank Murden* (1999), *Mohammad Nasser* (1993), *Wyn Palmer* (1991), *Carl Roberts* (1992), *Paul Ruggerio* (1994), *Brad Scharf* (1993), *Larry Singer* (2001), *David Smart* (2000), *Jake Steigerwald* (1999), *Mike Timko* (1982), *Jim Wilson* (1993), and *Scott Wurcer* (1996).

NEW FELLOW



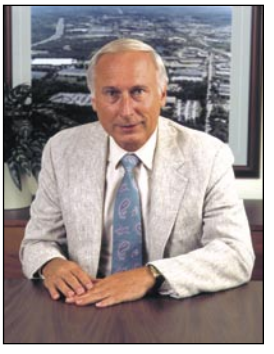
Dr. Michael Judy has made major contributions to our inertial iMEMS® (integrated micro electro-mechanical system) technology, best known for integrated accelerometers (more than 100 million shipped). He holds four patents and has submitted nine additional patent applications in the MEMS arena. He has been responsible for major contributions to both the mechanical structure and the circuit architecture of the ADXL202—a single-sensor, two-axis accelerometer.

Mike's "unique cross-functional mastery of MEMS technology, processes, and circuit design quickly set him apart as an innovator in this very new and burgeoning market," according to Sam Fuller, our V.P. of Research and Development. "In his ten years at ADI, Mike has not only been an outstanding original contributor, but has also built and managed a world-class team of MEMS- and computer-aided-design engineers. His contributions in advancing the MEMS state of the art, developing innovative products, recruiting talent, and forming valued partnerships have directly contributed to our success in the MEMS market. He is the [very] embodiment of the ADI Fellows program."

After receiving his BSEE from MIT and completing his PhD from U.C. Berkeley, Dr. Judy joined ADI in 1993 as a MEMS process-development engineer, where he began contributing heavily to ADI's groundbreaking MEMS process-development effort. He later transitioned to MEMS design and soon assumed responsibility for all MEMS mechanical design and MEMS CAD (computer-aided development) tools.

Mike works at our Cambridge (MA) facility, and lives in Wakefield, MA with his wife Patricia and two children Annabel and Katherine. When not engaged with MEMS or helping to raise his two young children, he enjoys working in his woodshop, hiking in the White Mountains, and windsurfing.

IEEE FOUNDERS MEDAL TO ADI CHAIRMAN



The Institute of Electrical and Electronics Engineers (IEEE) has awarded one of its most prestigious medals, the Founders Medal, to Ray Stata, co-founder and chairman of Analog Devices, Inc. The Founders Medal is awarded "for major contributions in the leadership, planning, and administration of affairs of great value to the electrical and electronics engineering profession." The citation reads: *For leadership in the electronics industry through innovative technological development and visionary contributions in entrepreneurship, management, and education.*

According to IEEE, "One of the founders of Analog Devices, Inc. (ADI) in 1965, Mr. Stata served as president of the company from 1971 to 1991 and as CEO from 1973 to 1996. He has served as chairman of the board since 1973. Responding to industrial shifts, Mr. Stata guided ADI through a number of critical transformations—changing from a producer of modules of discrete components in the 1960s to a market-leading provider of high-performance analog-, mixed-signal-, and digital signal-processing integrated circuits."

(continued on page 14)

Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 37 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com]**.

Solving Power-Management Problems with a Single Chip that Handles up to 7 Channels of Sequencing, Monitoring, and Supervision

By Peter Canty [peter.canty@analog.com]

The design of systems with multiple supply voltages is commonplace today. In such systems as Internet routers, digital subscriber-line access multiplexers (DSLAMs), base stations, and servers, the sequencing and supervision of their multiple supplies has grown in importance. The ADM1060 *supervisor/sequencer* from Analog Devices greatly simplifies this task by providing multiple supply supervisors, sequencing logic, and multiple-output drivers, in a single 28-lead TSSOP device—ideal for applications where board space is at a premium. The configuration of these multiple functions is easily programmed using an intuitive *graphical user interface* (GUI), also provided by Analog Devices.

The increasing number of user demands on designers of the backplanes, line-cards, and blades used in infrastructure and server systems is making the design task increasingly difficult. Customers want more channels at higher data rates for less money. They also require a much higher level of reliability than before: An uptime of 99.999%, commonly known as "*five*-9's *reliability*" (analogous to two minutes of down time per year), is now a basic requirement. Yet these more complex, more reliable boards must still fit in the same central-office and server form factors as before. Power budgets for these systems have not necessarily increased either, so greater attention must now be paid to power consumption.

The additional bandwidth, expressed in both channel count and speed, has resulted in a proliferation of many new-generation microprocessors, DSP devices, FPGAs, and CPLDs. The cores of these devices run at much lower voltages than the traditional 3.3 V or 5 V (for example, 1.2 V, 1.5 V, 1.8 V, and 2.5 V are common core-supply levels). Yet I/O protocols dictate that 3.3-V and 5-V supplies still be provided. In fact, some designs may require a 12-V supply; others need termination voltages as low as 0.75 V; and there are even cases where *negative* supplies are required for op amp rails.

It is not uncommon for many, if not all, of these supplies to be needed on a single board. The requirement could easily be for six, seven, or more supplies. The sequence in which the supplies turn on can be critical to the reliable operation of the system. A good rule of thumb might be to start with the highest supply first and work downwards; but this is not always the case. For instance, some DSP manufacturers recommend that the core of their device be powered up before the I/O, while others recommend the *opposite*. Given the complexity of the PCBs being designed, the truth is that it may be difficult to determine what the optimal power-up sequence is without first designing, building, and testing the board. This "trial-and-error" approach can prove costly, both in terms of manufacturing costs (multiple board-design cycles, or *spins*) and in time to market.

The current discrete approach to supply sequencing, using reset generators, FET drivers, and RC time constants (a typical implementation is shown in Figure 1)—while adequate for a system requiring two or three supplies, becomes very cumbersome when the number rises to six or seven. Another problem is that accurate reset generators have fixed threshold voltages. If—as can be the case with ASIC designs—a supply voltage must be tweaked to a nonstandard value in order to provide maximum performance, a reset generator with the revised threshold may not exist. Also, designs of this nature require the power designer's best guess (albeit an educated one) as to the sequence required. If the guess proves wrong, it is difficult to rectify the issue without a board spin. Further, as the population density of PCBs increases, real estate becomes an issue and a multi-component discrete solution becomes unattractive. Finally, it is not easy to design a power-down sequence, using the same simple reset generators with fixed timeouts and open-drain outputs.

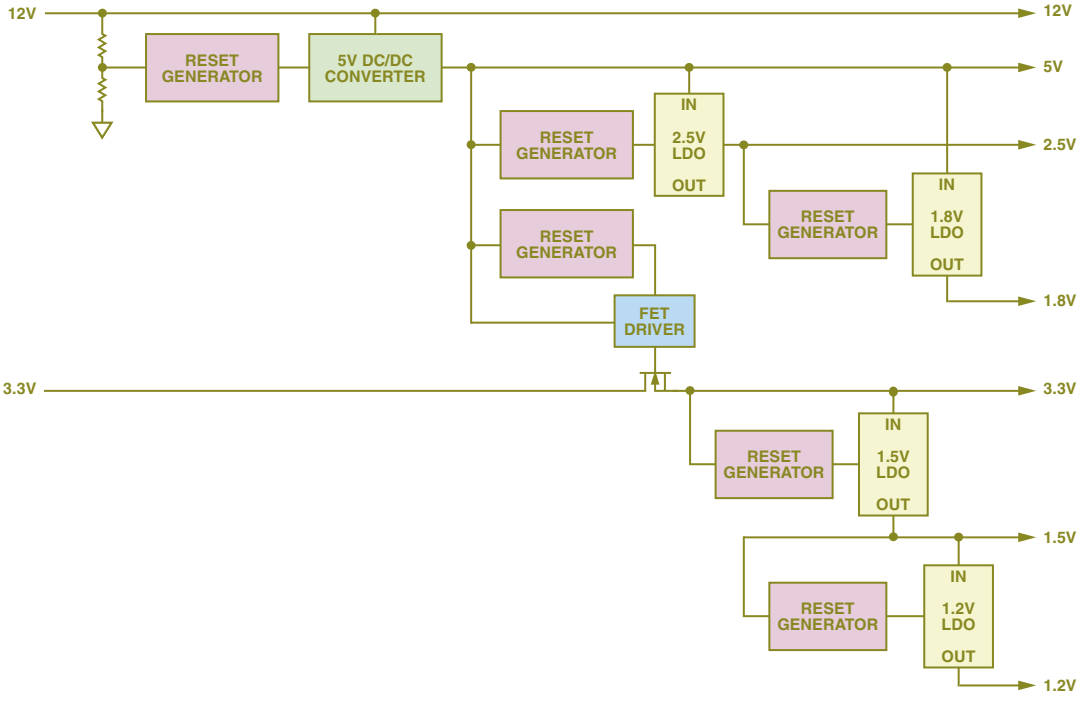

Figure 1. Discrete implementation for sequencing seven supplies.

The solution to be described here is a *single IC*, which provides a total voltage-management solution and encompasses all of the functionality of the discrete design shown in Figure 1. The device needs to—and does—go further, however, in providing the flexibility to change its configuration easily as required. If a reset threshold, the power-up sequence, the power-down sequence, and the watchdog timeout on a processor clock can be altered without laying out the hardware again, the power designer's task is made infinitely easier. Naturally, a single IC (with minimal external components) also addresses the key issue of board real estate. Reduced design time also means reduced time-to-market, since the power designer can implement a design more quickly—with confidence that, if necessary, it can be altered later without a change in hardware.

The Analog Devices ADM1060 *multi-supply supervisory circuit* is such a device. It is a total voltage-management solution in a single small 28-lead TSSOP package. It requires as few as two external components (two decoupling capacitors), making it ideal for applications where board space is at a premium.

The ADM1060 can supervise up to seven supplies. All of the supervisors on the chip use window comparators, so that both overvoltage and undervoltage supply faults can be detected on each of the supply fault input pins. One of the supply fault detectors can supervise a supply up to 14.4 V (analogous to a 12-V supply being overranged by +20%). Four of the supervisors can detect faults from 0.6 V to 6 V (analogous to a 5-V supply being overranged by +20%). The other two supervisors can be used to monitor negative supplies down to –6 V. If supervision of a negative supply is not required, these two pins can be used to monitor supplies up to +6 V. Any threshold voltage within the above ranges can be programmed with 8-bit resolution. Thus, if an ASIC runs optimally with a nonstandard voltage—i.e., not 1.2 V, 1.5 V, 1.8 V, etc., the ADM1060 can be programmed around the modified supply voltage with an accurate fault-detection window. The hysteresis of these comparators is programmable digitally, allowing the user to control the level of noise immunity required.

The ADM1060 does not need a dedicated power pin. The device uses an arbitration scheme to power itself from any one of five of the supply-fault input pins (the negative supply input pins are not used here). Whichever supply is highest is used to power the device. If the highest supply should fail, the ADM1060 seamlessly switches over to the next highest supply to power itself. Thus, even in a failing system, the device continues to be powered, allowing it to maintain supervision of the supplies for as long as possible. For example, it could cause a controlled power-down sequence to be initiated. The ADM1060 requires a minimum of 3.0 V (on one of the supply input pins) to power the device.

The ADM1060 also provides four *general-purpose inputs* (GPI's). These are logic inputs (TTL- or CMOS-compatible) that enable the user to apply control signals, such as POWER_OK, RESET, or MANUAL RESET, and use these to control the sequence in which the supplies turn on. Note that these inputs can also be used to take signals from external supervisory chips, if more than seven supplies need to be supervised and included in the sequencing. A watchdog timer is also included. This circuit is used to ensure that a processor clock continues to toggle (transition from low to high or high to low).

The logical core of the device is the *programmable logic-block array* (PLBA), combined with the *programmable delay block* (PDB). These blocks enable the ADM1060 to sequence the turn-on of the supplies' programmable time delays in the chosen order. A set of different time delays can be programmed for a power-down sequence. For instance, a supply may be required to power up 100 ms after the previous supply—but to turn off instantly if a fault occurs.

The ADM1060 makes available nine output drivers. These *programmable driver outputs* (PDOs) can be used as logic-control signals, such as chip-enable, LDO- (dc/dc brick-)output enable, or simply as status signals, such as POWER_GOOD, or RESET. The output pins all have an open-drain configuration, allowing the user to connect an external resistor to pull the pin up to the desired voltage. However, it is likely that the pull-up voltage is one that is being supervised at one of the inputs of the device and is available on-chip. Therefore, the ADM1060 features a bank of internal pull-up resistors, which can be connected to the pull-up voltage without external components. This is of course significant where minimal board space is available. Four of the output drivers can also provide a high-voltage gate drive to turn on an NMOS FET, which may be placed in a supply path. In this option, a 12-V charge-pump voltage is provided at the output pin.

Communication with the ADM1060 is via an industry-standard 2-wire interface (SMBus). The user can set up the features described using the intuitive GUI provided by Analog Devices. This programming can be done offline, using the Evaluation Kit, or in-system, using a 3-pin header cable (data, clock, and GND). Both are available from Analog Devices. Once satisfied with the configuration, the user can store this in nonvolatile memory, so that each time the device is subsequently powered up, the same configuration is downloaded and set up in the device. An example window from the GUI is shown in Figure 2.

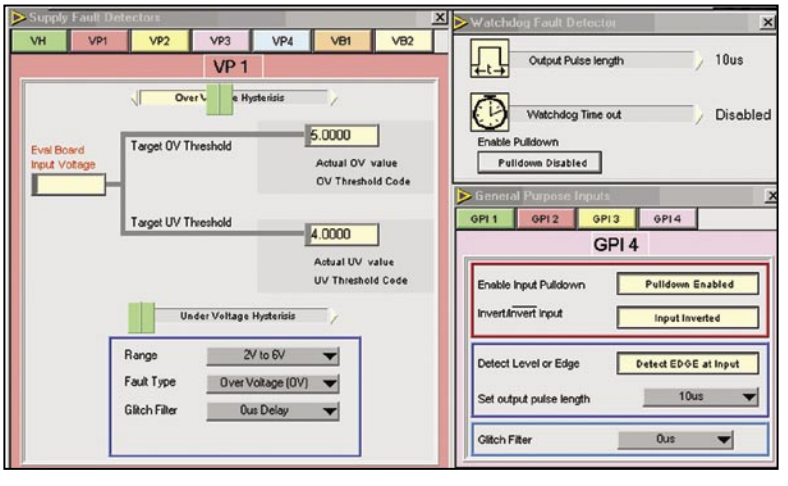

Figure 2. ADM1060 graphical user interface (GUI).

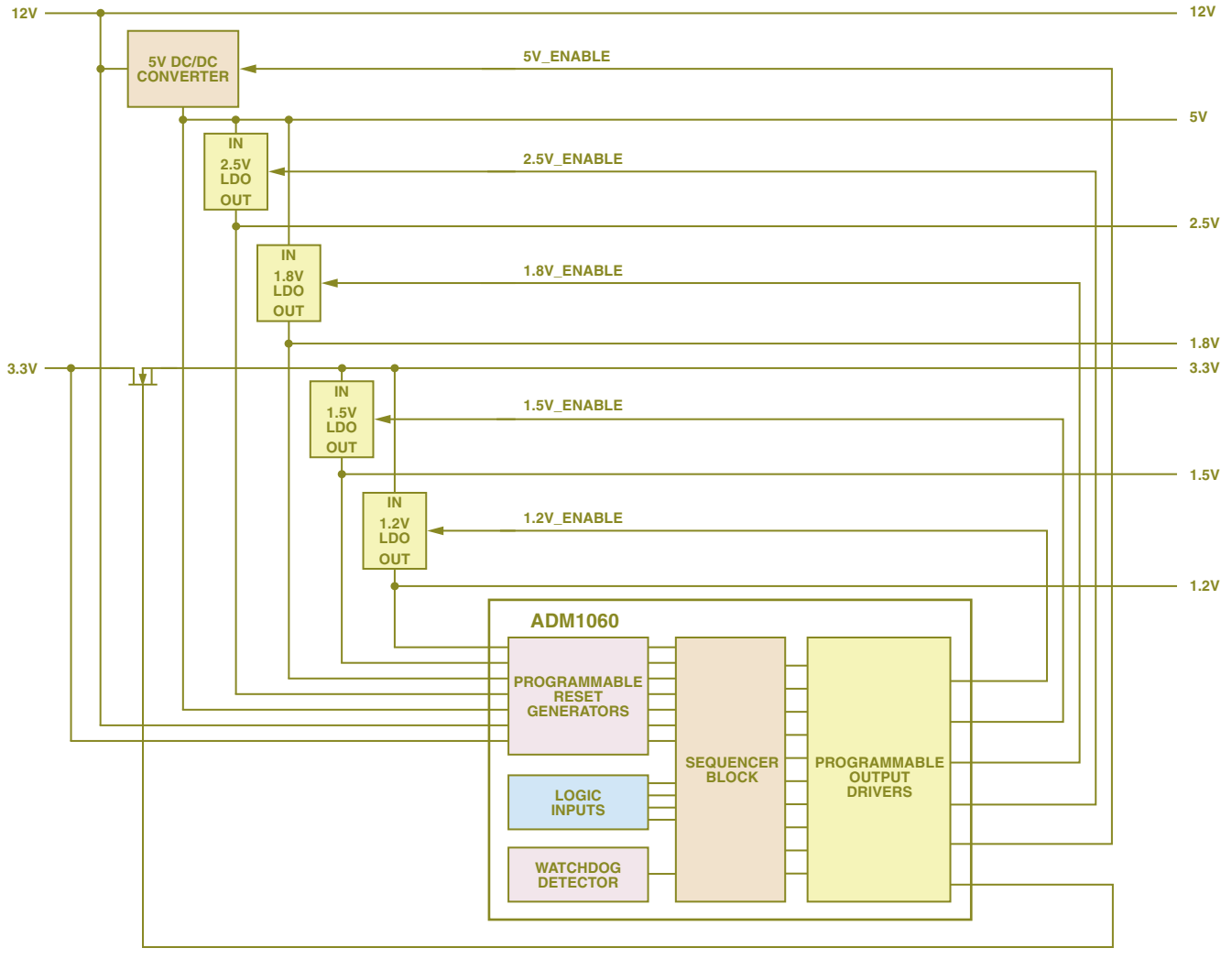

Figure 3. Sequencing the same seven supplies using a single ADM1060.

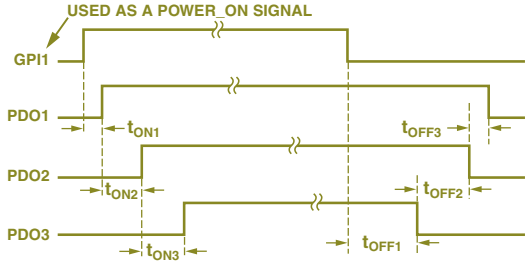

Figure 4. Controlled power on/off sequence using the ADM1060.

Providing the same seven supplies outlined in the discrete design of Figure 1, a sequence could be implemented using a single ADM1060 as shown in Figure 3.

Another very powerful feature of the ADM1060, not easily replicated in a discrete design, is the ability to configure a controlled power-down sequence. Again, using the software provided, a sequence like that shown in Figure 4 can be configured.

CONCLUSION

The requirement for multiple voltages on a single PCB has resulted in a difficult supply sequencing problem for power designers. With six, seven, or more voltages required, discrete solutions are unwieldy and impractical. The ADM1060 from Analog Devices provides a powerful and flexible solution, making the configuration of supply thresholds, logic inputs, and supply sequencing a straightforward *software* design—rather than a costly and error-prone hardware design.

Ask the Applications Engineer—31

By Reza Moghimi [reza.moghimi@analog.com]

AMPLIFIERS AS COMPARATORS?

Q. What is a comparator? How does it differ from an op amp?

A. The basic function of a high-gain comparator is to determine whether an input voltage is higher or lower than a reference voltage—and to present that decision as one of two voltage levels, established by the output's limiting values. Comparators have a variety of uses, including: polarity identification, 1-bit analog-to-digital conversion, switch driving, square/triangular-wave generation, and pulse-edge generation.

In principle, any high-gain amplifier can be used to perform this simple decision. But "the devil is in the details." So there are some basic differences between devices designed as op amps and devices designed to be comparators. For example, for use with digital circuitry, many comparators have latched outputs, and *all* are designed to have output levels compatible with digital voltage-level specifications. There are some more differences of importance to designers—they will be discussed here.

Q. What are some circumstances where one can go either way?

A. Amplifiers should be considered for use as comparators in applications where low offset and drift, and low bias current, are needed—combined with low cost. On the other hand, there are many designs where an amplifier could not be considered as a comparator because of its lengthy recovery time from output saturation, its long propagation delay, and the inconvenience of making its output compatible with digital logic. Additionally, dynamic stability is a concern.

However, there are cost and performance benefits in using amplifiers as comparators—if their similarities and differences are clearly understood, and the application can tolerate the generally slower speed of amplifiers. No one can claim that an amplifier will serve as a drop-in replacement for a comparator in all cases—but for slow-speed situations requiring highly precise comparison, the performance of some newer amplifiers cannot be matched by that of comparators having greater noise and offset. In some applications with slowly changing inputs, noise will cause comparator outputs to slew rapidly back and forth (*see* "Curing comparator instability with hysteresis," *Analog Dialogue,* Volume 34, 2000). In addition, there can be savings in cost or valuable printed-circuit-board (PCB) area in applications where a dual op amp could be used instead of an op amp and a comparator—or in a design where three of the four amplifiers in a quad package are already committed, and two dc or slowly varying signals must be compared.

Q. Can that fourth amplifier be used as a comparator?

A. This is a question that many system designers are asking us these days. It would pointless to buy a quad op amp, use only three channels, and then buy a separate comparator—if indeed that amplifier could be used in a simple way for the comparison function. Be clear, though, that an amplifier can't be used as a comparator interchangeably in all cases. For example, if the application requires comparison of signals in less than a microsecond, adding a comparator is probably the only way to go. But if you understand the internal architectural differences between an amplifier and a comparator, and how these differences affect the performance of these ICs in applications, you may be able to obtain the inherent efficiency of using a single chip.

In these pages, we will describe the parametric differences between these two branches of IC amplifier technology and provide useful hints for using an amplifier as a comparator.

Q. So how do amplifiers and comparators differ?

A. Overall, the *operational amplifier* (op amp) is optimized to provide accuracy and stability (both dc and dynamic) for a specified linear range of output values in precision closed-loop (feedback) circuits. However, when an open-loop amplifier is used as a comparator, with its outputs swinging between their limits, its internal compensation capacitance—used to provide dynamic stability—causes the output to be slow to come out of saturation and slew through its output range. Comparators, on the other hand, are generally designed to operate open loop, with outputs slewing between specified upper and lower voltage limits in response to the sign of the net difference between the two inputs. Since they do not require the op amp's compensation capacitors, they can be quite fast.

If the input voltage to a comparator is more positive than the reference voltage plus the offset—V_{OS} (with zero reference, it's just the offset) plus the required *overdrive* (due to limited gain and output nonlinearity), a voltage corresponding to logic "1" appears at the output. The output will be at logic "0" when the input is less than V_{OS} and the required overdrive. In effect, a comparator can be thought of as a one-bit analog-to-digital converter.

There are different ways of specifying a comparator and an amplifier. As an example, in an amplifier, the *offset voltage* is the voltage that must be applied to the input to drive the output to a specified mid-range value corresponding to ideal zero input. In a comparator this definition is modified to center in the specified voltage range between 1 and 0 at the output. The comparator's "low" output value (logic 0) is specified at less than 0.4 V max in comparators with TTL-compatible outputs, while for a low-voltage amplifier, the *low* output value is very close to its negative rail (e.g., 0 V in a single-supply system). Figure 1 compares the *low* output values of typical amplifier and comparator models, with a –1-mV differential input applied to each.

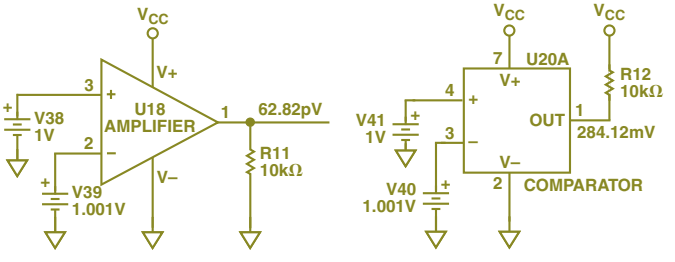

Figure 1. Responses of single-supply amplifier (63 pV) and comparator (280 mV) models to a –1-mV input-voltage difference.

Built to compare two levels as quickly as possible, comparators do not have the internal compensation capacitor ("Miller" capacitor) usually found in op amps, and their output circuit is capable of more flexible excitation than that of op amps. This absence of compensation circuitry gives comparators very wide bandwidth. At the output, ordinary op amps use push-pull output circuitry for essentially symmetrical swings between the specified power supply voltages, while comparators usually have an "open-collector" output with grounded emitter. This means that the output of a comparator can be returned through a low-value collector load resistor ("pullup" resistor) to a voltage different from the main positive supply. This feature allows the comparator to interface with a variety

of logic families. Using a low value of pull-up resistance yields improved switching speed and noise immunity—but at the expense of increased power dissipation.

Because comparators are rarely configured with negative feedback, their (differential) input impedance is not multiplied by loop gain, as is characteristic of op amp circuits. As a result, the input signal sees a changing load and changing (small) input current as the comparator switches. Therefore, under certain conditions, the driving-point impedance must be considered. While *negative* feedback keeps amplifiers within their linear output region, thus maintaining little variation of most internal operating points, *positive* feedback is often used to force comparators into saturation (and provide hysteresis to reduce noise sensitivity). A comparator's input usually accommodates large signal swings, while its output has a limited range due to interfacing requirements, so a lot of rapid level shifting is required within the comparator.

Each of the above differences between an amplifier and a comparator is there for a reason, with the major goal of comparing rapidly varying signals as quickly as possible. But, for comparing slow-speed signals—especially where sub-mV resolution is required—some new rail-to-rail amplifiers from Analog Devices could be better buys than comparators.

Q. OK. I can see that there are overall differences. How do they look to the designer who wants to use an op amp to replace a comparator?

A. Here are six major points:

1. Consider V_{OS} and I_B non-linearity vs. input common-mode voltage

When using voltage comparators, it is common practice to ground one input terminal and use a single ended input. The primary reason has been the poor common-mode rejection of the input stage. In contrast, many amplifiers have very high common mode rejection and are capable of detecting microvolt-level differences in the presence of large common-mode signals. Figure 2 shows the response of an AD8605 op amp to a 100-mV differential step riding on a 3-V common-mode voltage.

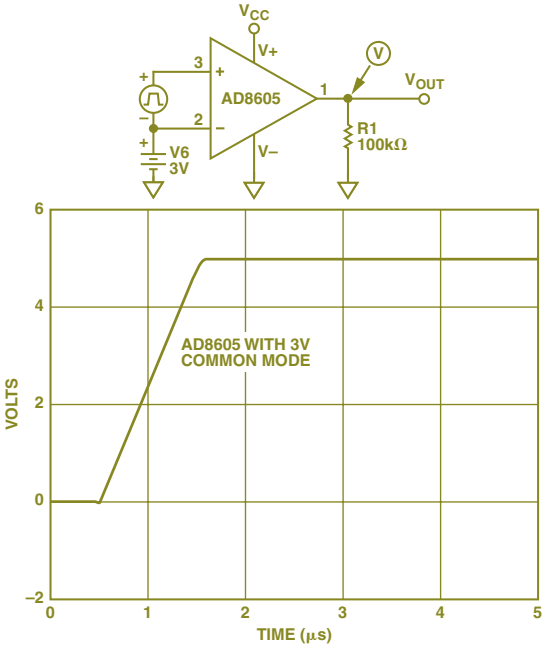

Figure 2. Response of open-loop AD8605 to a 100-mV differential step with 3-V common-mode voltage. Note the essentially linear slewing between the 0- and 5-V rails, and the clean saturation.

But, for many *rail-to-rail-input amplifiers*, *input offset voltage* (V_{OS}) and *input bias current* (I_B) are non-linear over the input common-mode voltage range. With these amplifiers, the user needs to take this variation into account in the design. If the threshold is set at zero common-mode, but the part is used at some other common-mode level, then the logic level that results may not be as anticipated. For example, a part with offset of 2 mV at zero common mode, and 5-to-6 mV over the entire common mode range may give an erroneous output when comparing a difference of 3 mV at some levels in that range.

2. Watch out for input protection diodes

Many amplifiers have protection circuitry at their inputs. When the two inputs experience a differential voltage greater than a nominal diode drop (say, 0.7 V), the protection diodes start conducting and the input breaks down. Therefore, it is critical to look at the input structure of an amplifier and make sure that it can accommodate the expected range of input signals. Some amplifiers, such as the OP777/OP727/OP747, do not have protection diodes; their inputs can accommodate differential signals up to the supply voltage levels. Figure 3 shows the response to a large differential signal at the input of an OP777. Many amplifiers' inputs break down under this condition, while the OP777 responds correctly. CMOS-input amplifiers do not have protection diodes at their input, and their input differential voltage can swing rail-to-rail. But remember that, in some cases, applying a large differential signal at the input causes significant shifts of amplifier parameters.

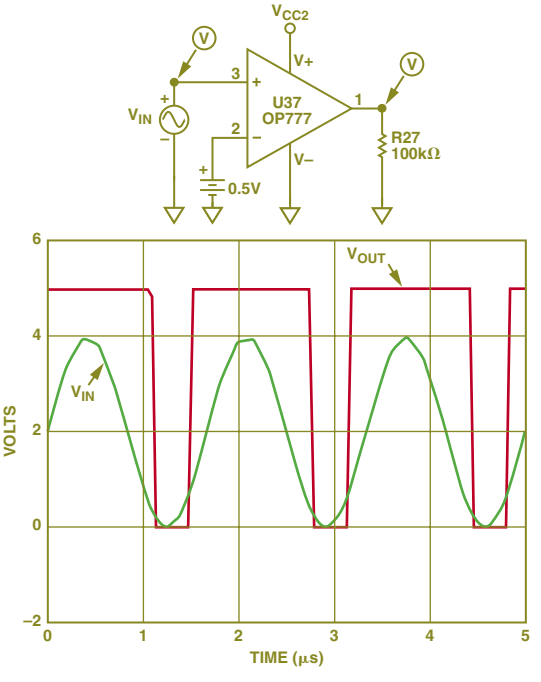

Figure 3. Response of an OP777 amplifier to a ±2-V, 1-kHz signal, biased by +2V, and compared with a +0.5-V dc level. Note that there is no phase inversion for this large swing. However, the gain is quite low at a common-mode level of +0.5 V from the negative rail, as can be seen by the approximately 0.3-V overdrive that is needed.

3. Watch out for input voltage range specs and phase-reversal tendencies

Unlike operational amplifiers that usually operate with the input voltages at the same level, comparators typically see large differential voltage swings at their inputs. But some comparators without rail-to-rail inputs are specified to have a limited common-mode input voltage range. If the inputs

exceed a device's specified common-mode range (even though within the specified *signal* range), the comparator may respond erroneously. This may also be true for some of the older types of amplifiers designed with junction-FET (JFET) and bipolar technologies. As the input common-mode voltage exceeds a certain limit (IVR), the output goes through phase inversion. This phenomenon can be detrimental (*see* in Chapter 6 of *Ask the Applications Engineer*,* the figure that follows the table). Therefore, it is absolutely critical to pick an amplifier that does not exhibit phase reversal when overdriven. This is one type of problem that can be overcome by using amplifiers with rail-to-rail-inputs.

4. *Consider saturation recovery*

Typical op amps are not designed to be used as fast comparators, so individual gain stages will go into saturation when the amplifier output is driven to one of its extremes, charging the compensation capacitor and parasitic capacitances. A design difference between amplifiers and comparators is the addition of clamp circuitry in comparators to prevent internal saturation. When an amplifier is pushed into saturation, it takes time for it to recover and then slew to its new final output value—depending on the output structure and the compensation circuitry. Because of the time it takes to come out of saturation, an amplifier is slower when used as comparator than when it is used under control in a closed-loop configuration. One can find saturation-recovery information in many amplifier data sheets. Figure 4 shows saturation recovery plots for two popular amplifiers (AD8061 and AD8605). The output structures of these amplifiers are standard push-pull rail-to-rail common-emitter.

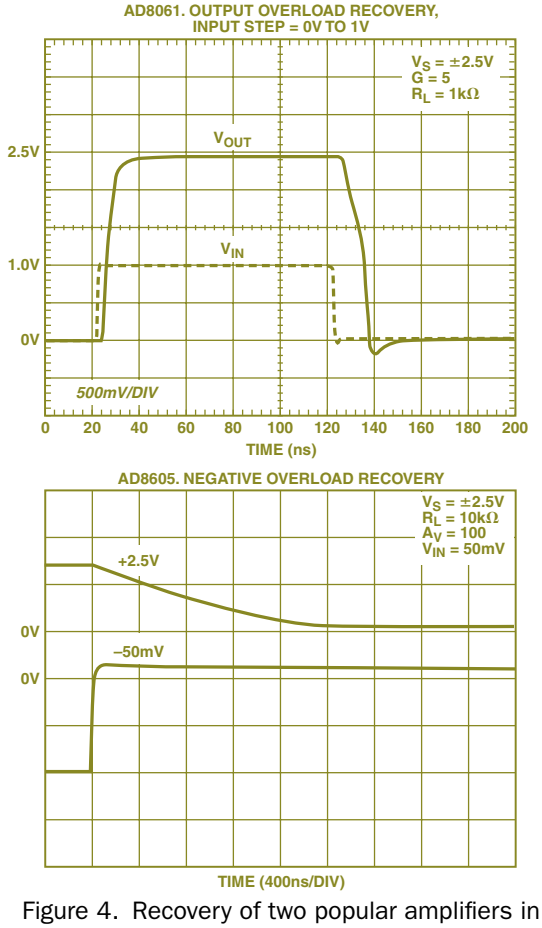

Figure 4. Recovery of two popular amplifiers in closed-loop configuration.

*www.analog.com/library/analogdialogue/anniversary/6.html

5. *Pay attention to factors affecting transition time*

Speed is one of the distinguishing differences between amplifier and comparator families. Propagation delay is the time it takes for a comparator to compare two signals at its input, and for its output to reach the midpoint between the two output logic levels. Propagation delay is usually specified with an *overdrive*, which is the voltage difference between the applied input voltage and the reference that is required for switching within a given time. In the following graphs, the responses of several rail-to-rail CMOS amplifiers are compared with a popular comparator. All amplifiers are configured as shown in Figure 5(a-e) with applied voltage, V_{IN}, = ±0.2 V, centered around 0 V. In the case of the comparator, a 10-kΩ pullup is used instead of a load to ground. The amplifier speeds differ widely, but because of saturation and their lower slew rate, all are much slower than the comparator.

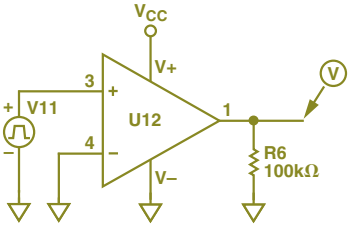

Figure 5a. Amplifier circuit.

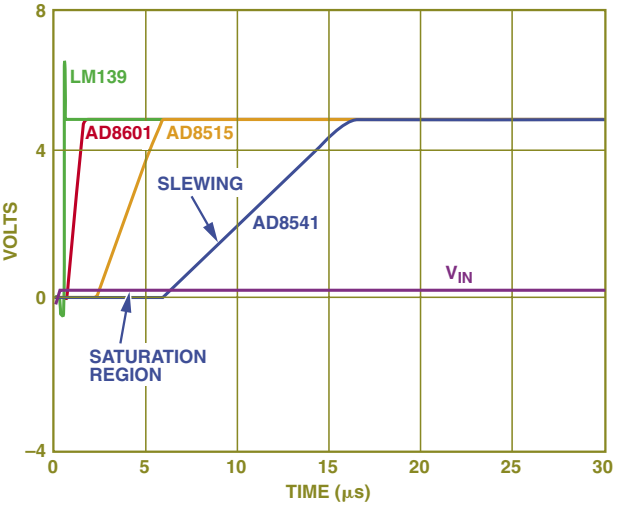

Figure 5b. Positive step.

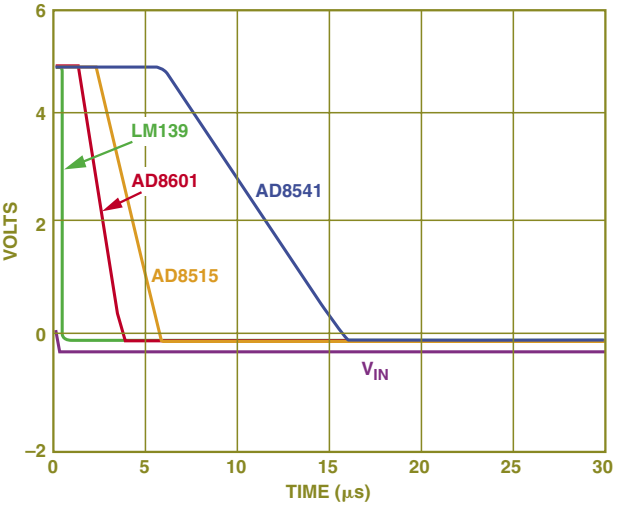

Figure 5c. Negative step.

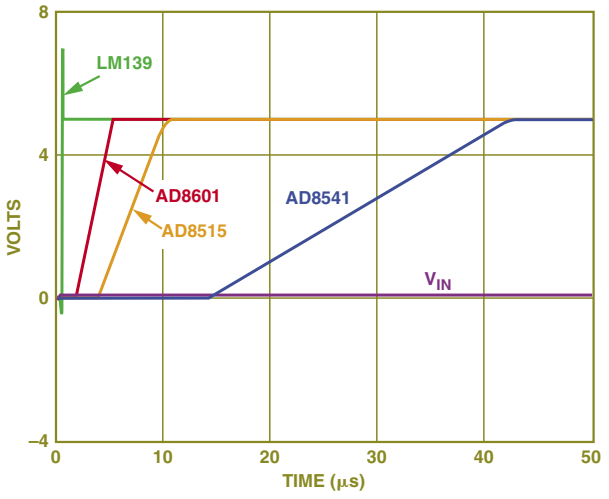

Figure 5d. Positive step.

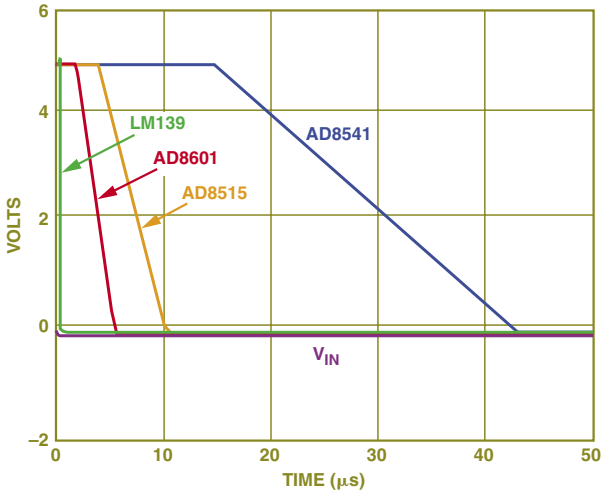

Figure 5e. Negative step.

Figure 5. Responses of comparator and three open-loop amplifier models compared, ±0.2-V drive. a. Amplifier circuit configuration. b. Positive step. c. Negative step. Then, with 50-mV signal applied and overdrive of 20 mV. Period = 10 µs. d. Positive step. e. Negative step.

Part Number	Supply Current (µA)	Offset Voltage (mV)	Supply Range (V)	Slew Rate (V/µs)
AD8515	350	5.00	1.8–5.0	5
AD8601	1,000	0.05	2.7–5.0	4
AD8541	55	6.00	2.7–5.0	3
AD8061	8,000	6.00	2.7–8.0	300
LM139	3,200	6.00	5.0–3.6	---

While most comparators are specified with 2-mV to 5-mV overdrive, most high precision, low input offset amplifiers can reliably operate with as little as 0.05-mV overdrive. The amount of overdrive applied at the input has a significant effect on propagation delay. Figure 6 shows the response of the AD8605 to several values of overdrive voltage.

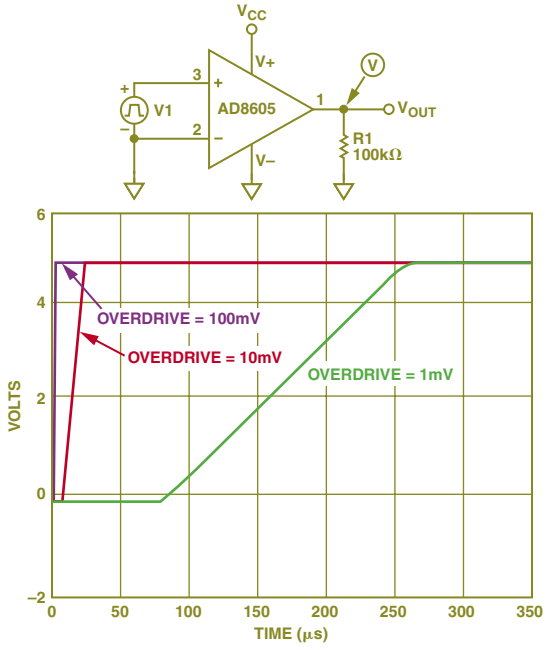

Figure 6. Response of the AD8605 as a comparator to step inputs with overdrive of 1, 10, and 100 mV.

As amplifiers are allowed to consume more power, their speed improves substantially, so that they can compete with comparators in terms of rise and fall times. Figure 7 includes an example of this—for an AD8061, with a 300 V/µs slew rate, in an open loop configuration responding to a sinusoidal zero crossing input, the output recovery time is 19 ns. However, one of the biggest drawbacks to using an amplifier as a comparator is often its power consumption, since one can generally find comparators that draw less supply current (I_{SY}), but still function well. Of course, for instruments using line power, power consumption is usually not a big driving factor. Besides, many amplifiers have a *shutdown* pin—a feature rarely available in comparators; it can be used to conserve power.

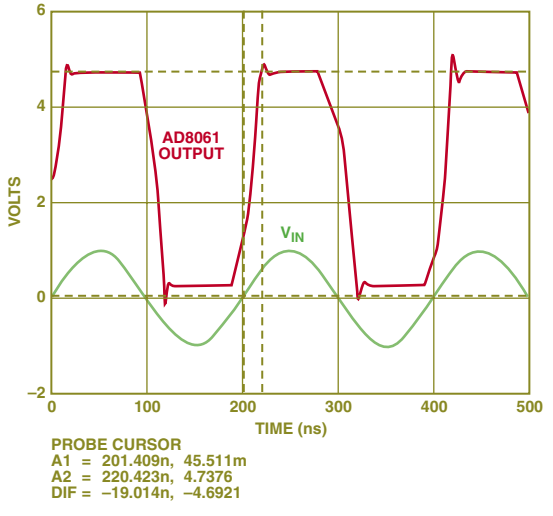

Figure 7. Response of AD8061 as a zero-crossing comparator.

In Figure 8, the AD8061's step response is compared with that of the popular LM139, and two other open-loop amplifiers, connected in the same circuit configuration as in Figure 6. As can be seen, the AD8061 responds within 300 ns, which is faster than LM139. This is achieved at the expense of higher current consumption.

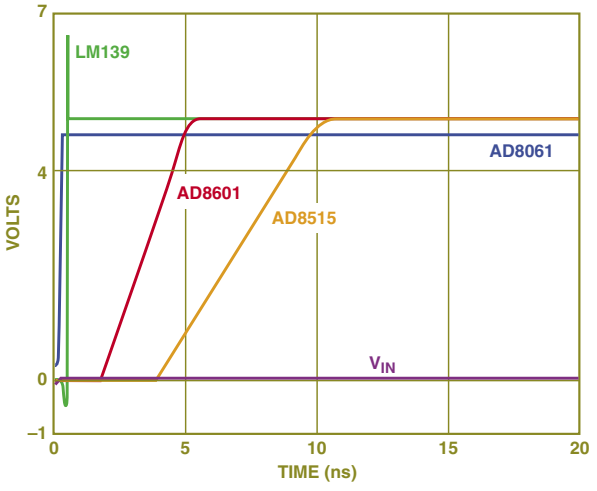

Figure 8. Step response of three amplifiers and a popular comparator. Note the especially fast response of the AD8061.

6. *Consider the way to interface with different logic families*

Many of today's rail-to-rail-output amplifiers operate with single supply of 5 V to 15 V, which can easily provide TTL- or CMOS-compatible output without the need for additional interfacing circuitry. If the logic circuit and op amp share the same supply, then a rail-to-rail op amp will drive CMOS and TTL logic families quite successfully, but if the op amp and logic circuitry need different supply levels, additional interface circuitry will be required. For example, consider an op amp with ±5 V supplies that must drive logic with +5 V supply: Since the logic is liable to be damaged if –5 V is applied to it, careful attention must be paid to the design of interface circuitry.

Figure 9 shows an OP1177 (dual-supply amplifier), interfaced to logic circuitry, and Figure 10 shows its response to 100 mV of overdrive. With ±5-V supplies, quiescent power dissipation is lowered and thermal feedback—due to output stage dissipation—is minimized, compared to ±15-V operation. The lower supply voltage also reduces the OP1177 rise and fall times as the output slews over a reduced voltage range—which in turn reduces the output response time.

Without the protective circuitry on the output of OP1177, the output would swing to $+V_{CC2}$ and $-V_{EE2}$; these levels might be detrimental to downstream logic circuitry. Adding Q2 and D2 prevents the output from going negative and translates the limits to TTL-compatible output levels. D2 clamps the output, so that it will not go below 0.7 V, as can be seen from waveform V(D2,2). The value of V_{CC} of Q2 can be selected (5 V was selected for this analysis) such that a correct logic level results, as shown by waveform V_{OUT}.

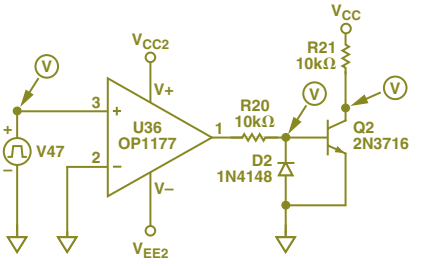

Figure 9. OP1177 connected for comparator operation, with translation and protective circuitry for TTL output.

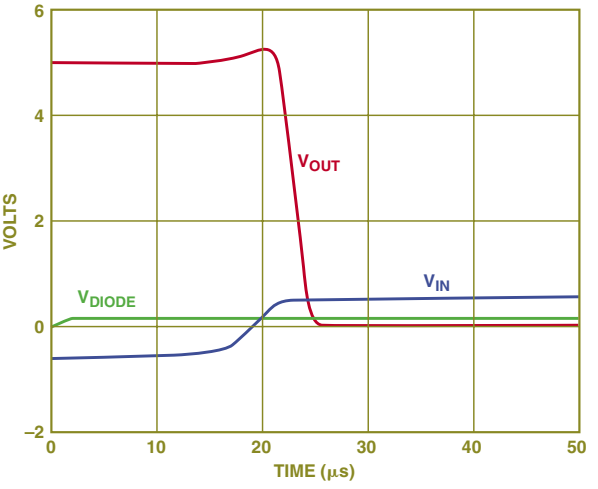

Figure 10. Response waveforms for the OP1177 comparator circuit.

To conserve power, an N-channel MOSFET may be used instead of the NPN transistor shown in Figure 9.

Q. So the bottom line is...

A. An amplifier can be used as a comparator with excellent precision at low frequencies. In fact, for comparing signals with microvolt-level resolution, precision amplifiers are the only practical choice. They can also be an economical choice for multiple-channel op amp users when employment of free amplifier channels to satisfy comparator requirements is feasible. Savvy designers can save money while optimizing their designs if they take the trouble to: understand the similarities and differences between amplifiers and comparators; read the amplifier's data sheet for the right features; understand about trade-offs in recovery time, speed, and power consumption; and are willing to verify designs with amplifiers configured as comparators.

Compact Web Manufacturing Process Defect-Detection System Uses a Camera and ADI Blackfin® Processor

By Hossain Hajimowlana, PhD, PE
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INTRODUCTION

One of the aims of industrial machine vision is to develop computer and electronic systems to replace human vision in quality control of industrial production. Web inspection systems are currently used for defect detection and quality control in numerous applications, such as the manufacture of high-tension-cable insulation, paper, plastic bags, strip steel, fuel pellets, chip packaging, wood, cloth, and weaving machines. Automatic inspection systems have numerous advantages over manual inspection. The manual inspection of surface defects is a tedious, if not impossible, task—often because of the small size of many defects and the very large areas to be inspected.

Conventional inspection systems consist of a line-scan camera, host computer, frame grabber, and one or more dedicated processing circuit boards. In this article, we discuss the development of a new integrated design environment—intended for real-time defect detection—that eliminates the need for an external frame grabber and eliminates or reduces the need for other associated host computer peripheral systems. The processing board, containing a reconfigurable field-programmable gate array (FPGA), is mounted inside a DALSA CCD camera. The FPGA is directly connected to the video data stream and outputs data to an associated ADI Blackfin type ADSP-BF535P processor for further processing. Using an FPGA for low-level processing alone represents an excellent trade-off between software and special-purpose hardware implementations. The processed data may be transferred through a USB or Firewire port to a PC for storage, monitoring, and additional processing. The present system is targeted for web inspection but has potentially broader applicability. Figure 1 shows a basic block diagram of an industrial inspection system that operates without a frame grabber.

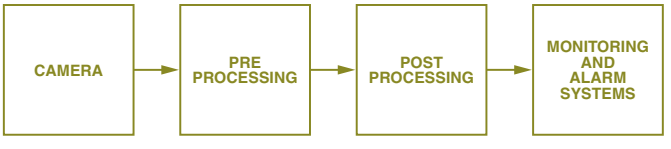

Figure 1. Block diagram of an industrial inspection process.

The defect detection task is delegated to two algorithms. The first one (*preprocessing*) undertakes the role of a conservative gross filter. Its objective is to detect all possible defects. This task will mainly be carried out in real time using the FPGA as a video-stream filter. The intent here is to provide a reliable means of rapidly identifying suspect regions that may or may not be finally classified as defective. In *postprocessing* we aim to identify the type and severity of the defect using an ADI Blackfin ADSP-BF535P processor. Typically this latter process has been carried out in the host computer, but a significant part of the process can be done locally in the modified camera system itself, using the powerful ADI Blackfin processor.

The system described in this article was developed at the University of Windsor, Canada as a PhD research project.

Establishing an appropriate computing environment for *real-time* applications, such as web inspection, is a challenging task. In this article, "real-time" describes any imaging system capable of receiving *and processing* continuous video data. A real-time system must perform *all* of the required operations within the critical time-frame allotted. Even under conditions of extreme system loading, the execution times and logical sequence of the system's response must be correct. The system described in this note can achieve real-time video processing for up to 30 *million* samples per second.

Test Setup

A test fixture that simulates a web manufacturing process with a provision for variable-speed operation has been set up as shown in Figure 2. The test setup comprises a DALSA TDI line-scan camera, a motorized drum with shaft encoder for TDI synchronization, and a dc light source with fiber-optic light guides. Our FPGA/DSP processing board is mounted above the regular camera control boards. Defective samples from various web sources are used for testing and verification of candidate algorithms.

Figure 2. Test setup for production-line simulation.

Hardware

The complete hardware assembly is shown in Figure 3.

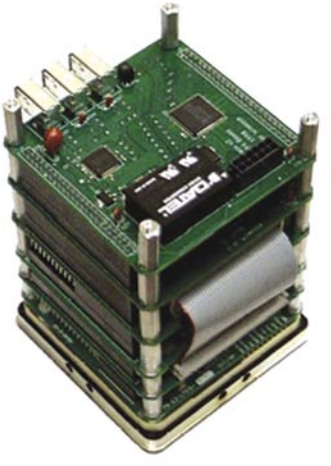

Figure 3. Processing hardware.

Figure 4 shows the block diagram of the processing system. The preprocessed data from the FPGA are stored in a FIFO, which buffers the data for further processing by the *digital signal processor* (DSP). The processing hardware assembly comprises three PCBs—the FPGA board, the DSP board, and a USB/Firewire board for linking to a PC. Other resources are shared between the boards.

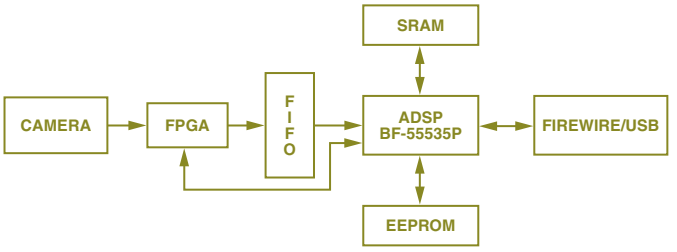

Figure 4. Block diagram of the processing board.

FPGA versus DSP

Our processing board supports processing in either the FPGA or the DSP—or *both*. How does one choose the disposition of processing capability for an application?

A DSP is a specialized microprocessor, typically programmed in C, with the occasional use of assembly code to improve system performance. The DSP is well-suited to extremely complex math-intensive tasks, involving conditional processing. It is limited in performance by the clock rate—and the number of useful operations it can do per clock. In contrast, an FPGA is an uncommitted "sea of gates." The device is programmed by connecting the gates together to form multipliers, registers, adders, and so forth. Math is done in hardware by interconnecting these building blocks. The blocks can range, in degrees of complexity, from a single gate to the very high level of an FIR filter or an FFT—given enough gates and the ability to interconnect them. Performance is limited by the number of available gates on the chip and by the clock rate.

FPGA and DSP thus represent two very different approaches to signal processing—each excelling at different things. There are many high-sampling-rate applications that an FPGA can do easily, but for which a DSP is unsuitable. Equally, there are many complex software problems—easy for a DSP—that the FPGA cannot address.

As a result of these complementary properties, the ideal system would split the work between FPGAs and a digital signal processor. In our web inspection system, most of the operations on an image *per se* are simple and very repetitive; so these primitive operations are best implemented in an FPGA. However, an imaging *pipeline* is often used to identify "blobs" or "regions of interest" in an object being inspected. These blobs can vary in size, and subsequent processing thus tends to be more complex. The algorithms used are often *adaptive*, depending on what the blob turns out to be. All things considered, a DSP-based approach is typically more effective at the back end of the imaging pipeline.

The Xilinx Spartan IIE series FPGA is used in our system, because it has additional *configurable logic block* (CLB) features that operate at greater speeds for memory-based designs—and it supports system clock rates of up to 200 MHz. A CLB includes a four-input function generator, carry logic, and storage element. Each CLB also contains logic that combines function generators to provide functions of five or six inputs.

Currently our design uses an XC2S200E, which has 5292 logic cells and 200K system gates. This FPGA has sufficient resources for many of our target applications and is packaged appropriately for building into a single-board in-camera system.

Choosing the Right DSP

It was very important to choose the right processor for our application. Power, cost and packaging, speed, performance, and availability of the right peripherals and development tools were the main factors in our decision to choose the ADSP-BF535P.

The ADSP-BF535P is a member of the Analog Devices Blackfin DSP product family. It combines a dual-MAC DSP engine, RISC-like microprocessor instruction set, and single-instruction, multiple-data (SIMD) multimedia capabilities into a single instruction-set architecture.

Power

Power plays an important role in web inspection systems. It is not uncommon to use a dozen of these cameras in the field. There may be applications where there is no need to further process the data by DSP, or the application can run at lower DSP clock speed. By using ADSP-BF535P, we did not need to sacrifice power for performance. In Blackfin ADSP-BF535P power can be reduced by reducing the core voltage and frequency. For this purpose, an external companion power management chip, the ADP3053, is available for dynamic control of the core voltage levels. Blackfin DSPs provide additional power control capability by allowing dynamic scheduling of clock inputs to each peripheral. Also, internal clocks are routed only to enabled portions of the device. For example, the 256KB on-chip L2 memory is divided into eight 32KB banks. This feature enables power to be reduced, as these banks are clocked only when they are accessed.

Cost and Packaging

The Blackfin ADSP-BF535P, a general-purpose DSP, typically costs much less than its closest digital-processing counterparts. In this application, its compact PBGA260 packaging format fits neatly into our 3.5" × 3.5" PCB.

Speed

Web inspection systems are demanding processing applications using intensive real-time algorithms. Thus, fast programmable, general-purpose digital signal processors are needed to handle the challenges presented by high speed data rates. Maximum core clock (CCLK) for the ADSP-BF535P is 350 MHz. We were able to successfully run our applications at 300 MHz (less in some cases to reduce power). CCLK pulses are generated via a PLL that has available CCLK to system clock (SCLK) ratios of 1 to 31. With a 20-MHz external oscillator we were able to achieve CCLK of 300 MHz. Depending on the CCLK, a maximum SCLK of 133 MHz can be achieved.

Performance

The Blackfin Processor is highly optimized to execute DSP applications code efficiently. In image processing applications, we usually deal with different sizes and kinds of filters (*infinite impulse response*, IIR; and *finite impulse response*, FIR) or apply *fast Fourier transform* (FFT) to the data. Table I shows some benchmarks done on ADSP-BF535P.

Table I. ADSP-BF535P signal processing algorithm benchmarks

Benchmark Description	Number of Clock Cycles
256-point complex FFT	3,176
Block FIR Filter	[(Number of Samples)/2] × [(Number of Taps)+2]
Biquad IIR Filter	2.5 × (Number of Biquad Sections) + 3.5

Peripherals

The ADSP-21535P contains a rich set of peripherals connected to the core via several high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance. It provides USB and PCI buses for glueless peripheral expansion without the need for costly external components.

For transferring processed data from the camera to a PC at medium data rates, USB seems a great solution. Because of the relatively high power consumption of the processing board, however, we are unable to use the bus-powered feature of USB. One of the most useful features of USB is that it is hot-pluggable, and the scanning camera can be plugged in or out of the monitoring system (a PC in this case) without a need to turn off the PC. For high data rate applications, where a series of monitoring cameras is used, IEEE Std. 1394 Firewire is recommended—it has 30 times more bandwidth than USB 1.1.

Development Tools

We have used VisualDSP++™ to develop and debug our codes. VisualDSP++ includes an integrated development environment (IDE) and a debugger that provides efficient project management, enabling us to move easily between editing, building, and debugging of programs. An evaluation platform for ADSP-BF535 is also available.

Algorithms

Different algorithms have been successfully simulated and implemented in the FPGA/DSP processing system. Here we briefly describe fuzzy logic and 1D AR algorithms. The interested reader can refer to the references for more detail.

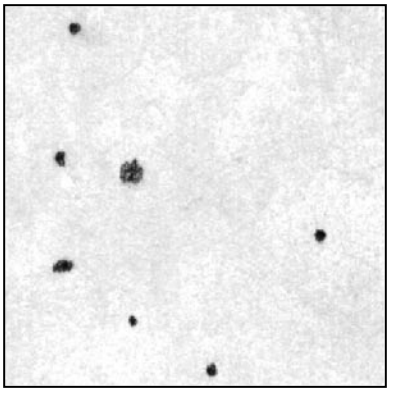

Figure 5. Stain defects on the sample.

Locating the exact position of the defects is performed using the ADSP-BF535P, employing the one-dimensional autoregressive (1D AR) algorithm.

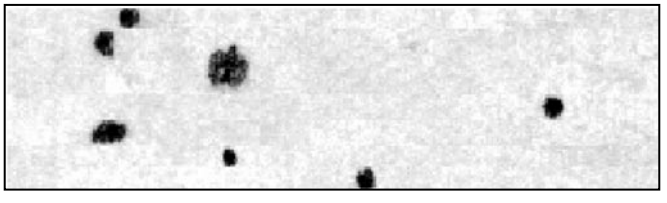

Figure 6. Image of selected defective lines of Figure 5.

Fuzzy Logic

A new and exciting application of fuzzy logic is for defect detection in web inspection systems. Defects in a manual detection system are usually described and identified by linguistic variables, e.g., *darker or brighter* regions; *smaller or larger* objects, so fuzzy logic appears to be a good candidate for defect-detection applications. To apply the algorithm, a set of texture features is derived off line from the "golden" (defect-free) template. These texture features are employed as inputs to the fuzzy decision engine. Outputs are obtained for the entire range of the possible inputs and stored in a look-up table (LUT). The proposed algorithm has been tested on a random texture sample with several stain defects (Figure 5); the image is digitized at a resolution of 256 rows × 256 columns with 8 bits of gray-level information. The result of applying the algorithm is shown in Figure 6.

Hardware Implementation of the 1D AR Algorithm

Figure 7 shows the simplified signal flow of the 1D AR algorithm.

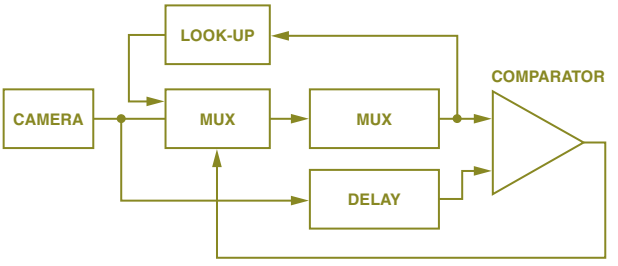

Figure 7. Simplified signal flow diagram of the 1D AR.

The 1D AR algorithm can easily be implemented in ADSP-BF535P and combined with the fuzzy-logic algorithm to detect the exact position of the defects in the defective lines.

The heart of the AR algorithm is an IIR filter (AR predictor). Since IIR filters are faster than FIR filters, they are more suitable for real-time applications. The experiments show that an 8^{th}-order filter is suitable for most of the textures. The computation units perform single-cycle operations, and there is no computation pipeline. The gray levels of the defective lines' pixels can be stored in on-chip SRAM, whence they are transferred out invisibly to external memory—or to the PC, through DMA controllers.

CONCLUSION

We have described an in-camera prototype processing board that basically consists of an FPGA and an ADI Blackfin processor. Some important issues for real-time web inspection systems were discussed, as well as the parameters—such as: power, cost, packaging, speed, performance, and the need for the right peripherals and development tools—that led us to choose ADSP-BF535 for our application. We showed that the Blackfin ADSP-BF535 provides an excellent platform for realizing low-power, high-performance, real-time embedded applications.

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[2] S.H. Hajimowlana, R. Muscedere, G.A. Jullien, J.W. Roberts, "An In-Camera Data Stream Processing System for Defect Detection in Web Inspection Tasks," *Journal of Real Time Imaging*, special issue on real time detection of defects, Spring 1999, Academic Press.

[3] S.H. Hajimowlana, R. Muscedere, G.A. Jullien, J.W. Roberts, "Defect Detection in Web Inspection Using Fuzzy Fusion of Texture Features," Proceedings of ISCAS 2000, Vol. III, pp. 718-721, May 2000.

(continued from page 2)

Having long chronicled in these pages the innovative achievements of ADI in its mastery of signal processing in the respective analog, mixed-signal, and digital fields—and its successful penetration of circuit technology all the way from modules to MEMs—we have long been appreciative of Ray's vision and leadership. We feel that the award of this medal to Ray also validates our own efforts. Indeed, in his acceptance speech, Ray said "My personal success is tightly coupled to the success of my company, Analog Devices, and to the thousands of employees and engineers there who have advanced the frontiers of signal processing. So Analog employees around the world very much share this recognition tonight." We would add that you, our readers, also deserve a share of that recognition for your hearty support of our products and ideas over the years.

However impressive the contributions to ADI's success, these are just the beginnings of Ray's contributions to the industry. According to IEEE:

"Mr. Stata shared his knowledge of business and management practices with other companies worldwide through the Center for Quality Management, which he—together with Professors Thomas Lee and Shoji Shiba from the Massachusetts Institute of Technology (MIT)—founded in 1989. He has served on the Executive Committee of the Council of Competitiveness since 1987, with the aim of helping rehabilitate and foster the competitiveness of American industry in a changing global economic climate.

"His work as co-founder and first president of the Massachusetts High Technology Council has spawned many initiatives, including the "Two-Percent Solution" contribution program—that encourages corporations to dedicate a portion of their research and development budgets to education.

"Mr. Stata is a member of the U.S. National Academy of Engineering and the American Academy of Arts and Sciences, and a Foreign Fellow of the Indian National Academy of Engineering. He has been chairman of the Semiconductor Industry Association, member of the Board of Overseers of the Baldridge National Quality Award, and currently serves as a member of the MIT Corporation. He is the co-author...of two books, *Global Stakes: The Future of High Technology in America and The Innovators: Rediscovering America's Creative Energy.*"

Not resting on his laurels, in accepting the award June 21, 2003, Ray threw down a challenge—one that all longstanding readers of *Analog Dialogue* should heed:

"Looking ahead, I believe one of the great opportunities for me and for IEEE to contribute is to focus on improving the disastrous state of math and physical science education in our K-12 schools, with the goal of encouraging more students to pursue engineering careers. Already through the Educational Activities Board and the Pre-College Education Coordinating Committee, IEEE has many such activities under way.

"For example, the National Science Foundation has funded and sponsored RESEED (Retired Engineers Enhancing Science Education through Experiments and Demonstrations), a program to engage retired engineers to participate in middle-school classrooms with new and exciting approaches to early physical-science education—another way for engineers to make their retirement years rewarding, productive, and *fun*."

For one such program—sponsored by Northeastern University, check http://www.reseed.neu.edu.

***–Dan Sheingold,* Editor**

AUTHORS

Peter Canty (page 3), an Electronics Engineering graduate from University College, Cork, Ireland, joined ADI in 1994 and worked for two years as a Test Development Engineer. After two years at Eastman Kodak, he returned to ADI in 1998, joining the Test Projects Group in Limerick. Since 2000, he has served as an Applications Engineer for the Interface Product Line.

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April

Low distortion **Differential RF/IF Amplifier** is optimized for driving 6-channel, 12-bit ADCs **AD8351**

5-channel, single-supply, **Rail-to-Rail Buffer Amplifier** operates with supply voltages up to 16 V **AD8560**

±2-*g* **Dual-Axis Accelerometer** in ultra-compact package **ADXL311**

Multiphase **IMVP-IV Core Controller** for mobile CPUs **ADP3205**

Dual **MOSFET Driver** has bootstrapped high-side drive and output disable **ADP3418**

CMOS **Switches/Analog Multiplexers** are fully specified with ±5-V, +5-V, and +3-V supplies **ADG633/658/659**

DecDriver® LCD Display Driver **AD8382**

May

8-channel, 24-bit, **Sigma-Delta ADC** is optimized for fast channel switching **AD7739**

12-/14-bit, 80-Msps **Pipelined ADCs** operate on single 3-V supply **AD9236/45**

96-kHz, 24-bit, **Sigma Delta Codecs** **AD1835A/37A/38A/39A**

SigmaDSP™ Digital Audio Processor with on-board D/A Converters **AD1953**

AC'97 SoundMAX® Codec **AD1985**

1-Gsps **Direct Digital Synthesizer** generates frequency-agile sine waves to 450 MHz **AD9858**

IC provides **Power-Supply Supervisory/Sequencing** functions for communication systems **ADM1060**

10.709 Gbps **Laser-Diode Driver** chipset **ADN2843**

256-position **Digital Potentiometers** have SPI-/I^2C compatible interfaces **AD5160/5161/5245**

High-performance **Mixed-Signal DSP** Controller **ADSP-21990/91/92**

Polyphase **Energy Metering IC** has serial interface **ADE7754**

2-, 3-, 4-phase Synchronous Buck Controller **uses 5-bit VID code** **ADP3166**

8-/10-/16-bit, 2-port **Level-Translating Bus Switches** **ADG3245/46/47**

12-channel **Gamma Buffers** plus **VCOM Buffer** on single chip **ADD8701**

June

SOT-23 packaged 12-/10-/8-bit **Micropower ADCs** operate on single 1.6-V supply **AD7466/67/68**

10-bit, 65-/80-Msps **Pipelined ADC** operates on single 3-V supply **AD9215**

Low Power **Differential Amplifier** can supply 400 mA peak output current **AD8390**

24-bit, 192-kHz Multichannel **Digital Audio Playback System** **AD1833A**

Mixed-Signal Front-End (MxFE™) for broadband applications **AD9878**

7.0-GHz PLL **Frequency Synthesizer** **ADF4107**

1.65 V to 3.6 V **Level Translators** are available as buffers, muxes, and bypass switches **ADG3231/32/33**

Dual **Interface for Flat Panel Displays** **AD9887A**

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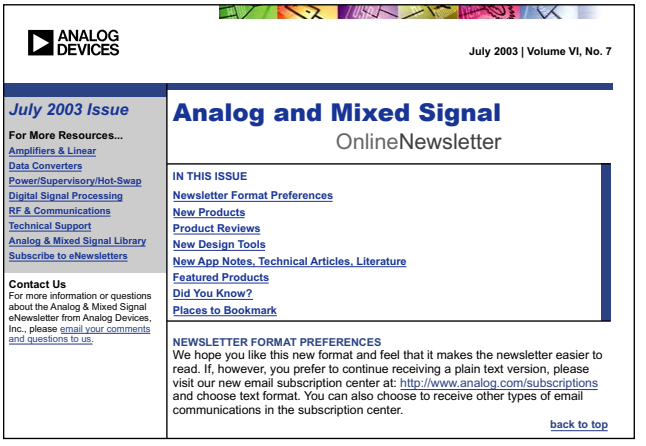
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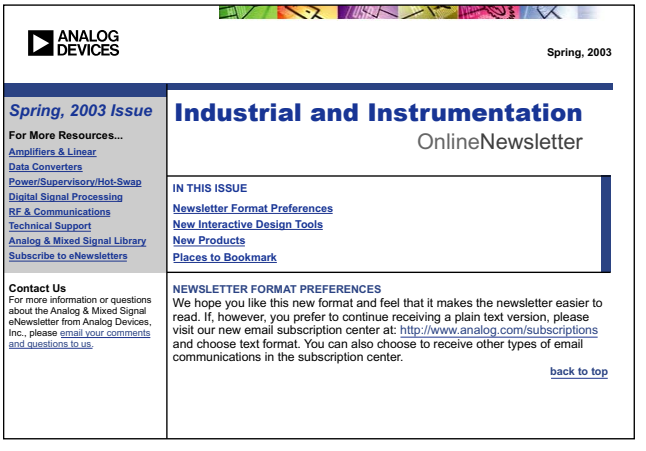
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