Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

DYNAMIC POWER MANAGEMENT OPTIMIZES PERFORMANCE vs. POWER OF BLACKFIN® DSPs (page 5)

Detecting Fast RF Bursts Using Log Amps (page 8)

Mirrors with Integrated Position-Sense Electronics for Optical Switching (page 3)

Complete contents on page 3

Volume 36 2002, Part 2

ANALOG DEVICES

Editor's Notes

We are pleased to note the introduction of a new Fellow at our 2002 General Technical Conference. Fellow, at Analog Devices, represents the highest level of achievement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art. Their creative technical contributions in product or process technology, or software, will have led to commercial success with a major impact on the company's net revenues and earnings.

Attributes include roles as mentor, consultant, entrepreneur, organizational bridge, teacher, and ambassador. Fellows must also be effective leaders and members of teams—and in perceiving customer needs. In the year 2002, one individual—Larry DeVito—was identified as having the rare combination of technical abilities, accomplishments, and personal qualities to qualify him to enhance our existing roster of Fellows: *Bob Adams* (1999), *Woody Beckford* (1997), *Derek Bowers* (1991), *Paul Brokaw* (1979), *Lew Counts* (1983), *Dennis Doyle* (2001), *Paul Ferguson* (2001), *Barrie Gilbert* (1979), *Roy Gosser* (1998), *Bill Hunt* (1998), *Josh Kablotsky* (2001), *Jody Lapham* (1988), *Chris Mangelsdorf* (1998), *Jack Memishian* (1980), *Doug Mercer* (1995), *Frank Murden* (1999), *Mohammad Nasser* (1993), *Wyn Palmer* (1991), *Carl Roberts* (1992), *Paul Ruggerio* (1994), *Brad Scharf* (1993), *Larry Singer* (2001), *David Smart* (2000), *Jake Steigerwald* (1999), *Mike Timko* (1982), *Bob Tsang* (1988), *Mike Tuthill* (1988), *Jim Wilson* (1993), and *Scott Wurcer* (1996).

–Dan Sheingold, Editor

New Fellow

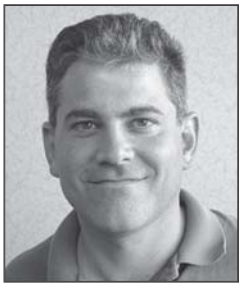
LARRY DEVITO

Larry DeVito joined Analog Devices in 1980. Over the decades, he has worked in areas of instrumentation, data-acquisition, transducer-interface, and integrated-sensor products. His designs include V/F converters, rms-to-dc converters, LVDT interfaces, and other magnetic-sensor products. His most recent work has been in the field of high-speed serial-data components, such as clock- and data-recovery ICs, synthesizers, and a transimpedance amplifier. He is Engineering Director of the company's fiber optics sensor-interface product line. Throughout his career at ADI, his efforts have inspired a series of product innovations; and his contributions continue to be at the crux of ADI's high-performance analog and fiber optics businesses.

Larry is a member of the program committee for the VLSI Circuits Symposium and the ISSCC. He holds nine patents, and three more are pending in the areas of high-performance analog circuits and fiber optics. He has written numerous papers and articles and has held advisory positions at MIT and Boston University.

An MIT graduate, he obtained the SB in 1975, and both the SM and EE in 1977. At MIT, he worked in the Crystal Physics Laboratory at the Center for Materials Science and Engineering, developing sputtered x-ray phosphors. He joined ADI after working for several years at the Sprague Electric Company as an IC design engineer. His hobbies include reading, gardening, and amateur radio.

AUTHORS *(continued on page 21)*



Rick Gentile (page 5) joined ADI in 2000 as a Senior DSP Applications Engineer; he currently leads the Blackfin® DSP Applications group. Prior to joining ADI, Rick was a member of the technical staff at MIT Lincoln Laboratory, where he designed several signal processors used in a wide range of radar sensors. He received a BS from the University of Massachusetts at Amherst and an MS from Northeastern University—both in Electrical and Computer Engineering. He enjoys sailing, windsurfing, and spending time with his daughters.

Alain Guery (page 11) is an Applications Engineer for A/D converters. He holds a Master's Degree from *l'Institut d'Electronique Fondamentale* (Paris) and has 15 years of design experience in data-acquisition systems used in most commercial aircraft engines, fiber optics, digital integrated circuits, and analog integrated circuits.

David Katz (page 5) is a Senior DSP Applications Engineer. He joined ADI in 2001 after working for several years at Motorola as a design engineer in cable modems and factory automation. David received both BS and MEng degrees in Electrical Engineering from Cornell University (1992). He enjoys spending his free time with his wife and son.

Charles (Chuck) Kitchin (page 11) is a hardware Applications Engineer at Analog Devices in Wilmington, Massachusetts. His main responsibilities include developing new applications circuits and writing technical publications. He has published over 70 technical articles, three books, and a large number of application notes. Chuck graduated with an ASET from Wentworth Institute in Boston; afterwards, he continued studying electrical engineering at the University of Lowell. His hobbies include astronomy, ham radio, and oil painting.

Analog Dialogue

www.analog.com/analogdialogue **dialogue.editor@analog.com**

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 36 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*on-line*, monthly or bimonthly at the above URL, and—less frequently—*in print*, as periodic retrospective collections of articles that have appeared on-line. In addition to technical articles, the on-line edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the Analog Dialogue site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus two special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com** and click on **<Contact ADI>** or type in this URL: **www.analog.com/request.html**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com]**.

Mirrors with Integrated Position-Sense Electronics for Optical-Switching Applications

by Trey Roessig [trey.roessig@analog.com] et al.*

For telecommunication systems to transition from 10-Gbit to 40-Gbit rates, signal paths using all-optical switches are becoming increasingly attractive. Analog Devices has developed an integrated optical microelectromechanical system (optical iMEMS) technology. It combines mirrors, high-voltage CMOS for electrostatic deflection, and low-voltage CMOS for on-chip capacitive position-sensing. This technology could drastically lower the cost of all-optical switching systems, ranging from 2 ×2 switches to large arrays. Described briefly here are the methodology and initial results of the position-sense functionality.

INTRODUCTION

All-optical switches do not need to convert the optical data to electrical signals and back. They increase the speed of the network by removing the important conversion bottleneck, and they are bandwidth- and protocol-independent.

The central component of many all-optical switches is a movable mirror. Although mirrors without position-sense capability are being developed, their assembly- and fiber-alignment costs are expected to result in relatively high prices. Position sensing, used in a feedback control loop that includes the high-voltage actuation circuitry and an external DSP, allows a factor-of-10 reduction in the mirror's natural settling time to a new position. This type of control loop will also provide more protection against shock and vibration than an open-loop system that simply actuates mirrors—but neither receives nor acts on position information.

We describe here the first mirrors to be developed with capacitive position-sensing integrated on-chip with the MEMS structure. The focus is on the methods and results of the capacitive sensing capability, which we consider an essential factor in reducing the cost of all-optical switches.

Capacitive Position Sensing

The use of capacitance variation to measure mirror position provides a number of advantages over other methods. It permits standard CMOS processing—rather than expensive custom processes—for devices that use the technique. Capacitive sensing is relatively stable over temperature, while other measurement methods, such as piezoresistive, can require complex connectivity to remove first-order temperature effects. Capacitive sensing also lends itself to on-chip circuit techniques that can add to this stability.

A way of accomplishing angular position measurement around one axis is to form a capacitive divider between the mirror itself and two sense electrodes beneath the structure, as shown in Figure 1. As the mirror rotates around an axis parallel to the dividing line between the two electrodes, one capacitance value increases and the other decreases. This differential capacitance can be used to measure the mirror rotation. In actual practice, of course, the electrodes are designed to sense multiple axes of rotation (see Figure 4).

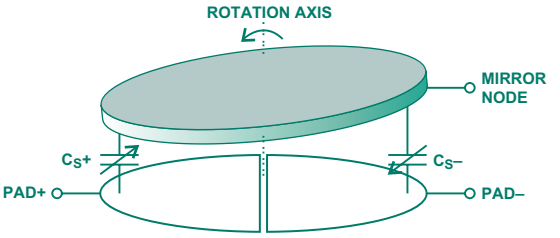


Figure 1. Capacitive bridge established by mirror structure.

A simplified version of a circuit to measure the differential capacitance is shown in Figure 2. Opposing voltage pulses are applied to each of the sense electrodes, and any differential capacitance will result in excess positive or negative charge on the mirror node itself. This charge is converted into a voltage by an on-chip amplifier. The voltage can provide a quantitative measurement of the mirror's angular position if the capacitive relationship is known.

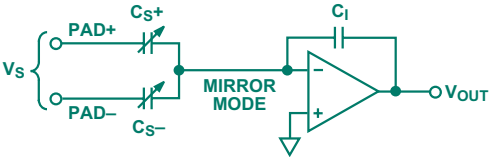


Figure 2. Capacitive detection circuit.

By integrating amplifier circuitry on the chip much greater position-measurement precision is possible than can be provided with off-chip detection. The principal reason is that parasitic capacitances and cross-coupling paths associated with bond wires can easily mask the tiny positional capacitances being measured. The much smaller parasitic capacitances associated with on-chip interconnections result in a dramatic increase in signal integrity.

Fabrication

Mirrors and position sense circuitry as described above have been successfully fabricated and tested at Analog Devices. Figure 3 shows a cross-section illustrating the proprietary optical iMEMS process used to fabricate these mirrors. A 3-layer process—using silicon-on-insulator (SOI) bonding—is used to fabricate a mirror, a silicon sacrificial layer, and a circuit device layer—all on the same substrate. These components combine to allow fine-featured MEMS structures and precision high- and low-voltage BiCMOS circuitry to coexist on the same substrate, making the capacitive mirror sensing feasible.

IN THIS ISSUE
Volume 36, Part 2, December 2002

Editor's Notes, New Fellow, Authors 2
Mirrors with Integrated Position-Sense Electronics for Optical-Switching Applications 3
Dynamic Power Management Optimizes Performances vs. Power in Embedded Applications of Blackfin® DSPs 5
Detecting Fast RF Bursts Using Log Amps 8
High-Speed Op Amp Drives a 16-bit, 1-MSPS Differential-Input A/D Converter 11
Single-Chip Digitally Controlled Data-Acquisition as Core of Reliable DWDM Communications Systems 15
Bus Switches for Speed, Safety, and Efficiency: What They Are, and What You Should Know about Them 18
Books, New Products 22-23
More Authors 21

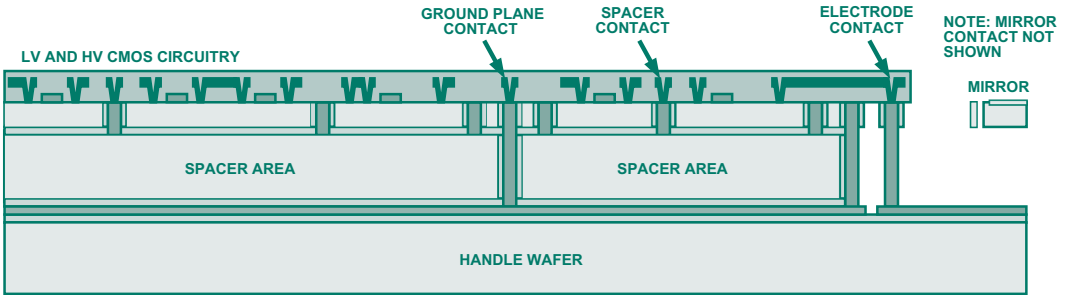


Figure 3. Analog Devices optical iMEMS process—optical mirror fabrication with integrated circuitry.

A scanning-electron-microscope (SEM) image of a fabricated mirror array is shown in Figure 4. This picture shows the 2-axis mirror, the position sense electronics (at bottom), and the gap underneath the mirror, which allows it to rotate. As shown it is rotated about the "Y" axis. Although not shown here, multiple mirrors can be fabricated on the same substrate, allowing for both high-port-count designs and the economies of scale typical of Analog Devices micromachined products.

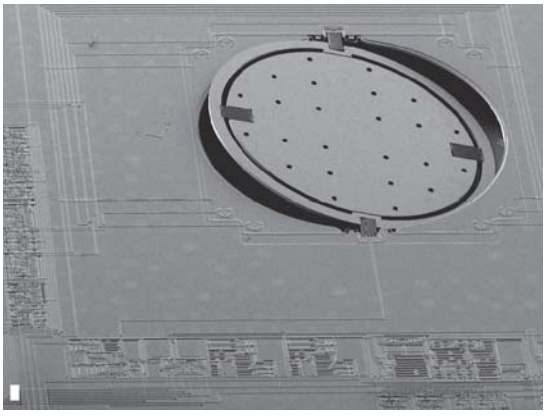


Figure 4. SEM of fabricated mirror with integrated circuitry.

Testing Results

Table 1 shows some target specifications and experimental results from the initial fabrication of these devices.

Table 1. Design targets and experimental results

Parameter	Target (Result if Different)
Mirror Diameter	800 μm
Maximum Angle	5 degrees
Natural Frequency	500 Hz (519 Hz)
Output Noise	2 μV/μHz (2.6 μV/μHz)

Figure 5 shows the relationship between the applied drive voltage and the output of the position-sense interface. A negative input voltage in this context refers to a voltage applied to the negative drive electrode. The classic $V \times |V|$ square-law behavior, typical of electrostatically driven structures, can easily be observed in the data.

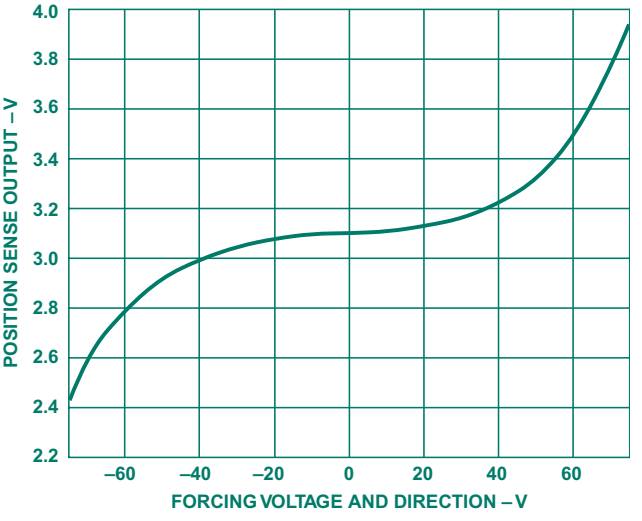


Figure 5. Position sense output for given input drive voltage.

CONCLUSIONS

The Analog Devices Micromachined Product Division has developed the first mirrors with on-chip capacitive position sensing. This technology promises products employing all-optical switches with improved insertion loss performance and capable of high-port-counts. These developments are the first steps toward greatly reducing the assembly costs of all-optical switches.

*ACKNOWLEDGEMENT

This project was a team effort at Analog Devices, Inc. The article is based on a paper submitted by the team and accepted for presentation at the European Conference on Optical Communication (ECOC). Members of the team, in addition to the above, were Ara Arakelian [ara.arakelian@analog.com], Tim Brosnihan [tim.brosnihan@analog.com], Bill Clark [bill.clark @analog.com], David Han [david.han@analog.com], Michael Judy [michael.judy@analog.com], Thor Juneau [thor.juneau @analog.com], Mark Lemkin [mark.lemkin@analog. com], Steve Sherman [steven.sherman@analog.com], and Jeff Swift [jeff.swift@analog.com]

Dynamic Power Management Optimizes Performance vs. Power in Embedded Applications of Blackfin® DSPs

by David Katz (david.katz@analog.com)
Rick Gentile (richard.gentile@analog.com)

The rapidly increasing consumer demand for products employing multimedia embedded processors calls for both high performance and low power consumption. But the increased computational complexity and faster clock rates necessary for high performance processing are hard to achieve using tactical power-saving design schemes. What is needed is a strategic way to manage power consumption to optimize performance versus power for the specific embedded application. Such an approach is achievable with the inherent *dynamic power management* capabilities of the Blackfin DSP family.

Blackfin DSPs are fixed-point, dual-16-bit-MAC/dual-40-bit-ALU digital signal processors. They are ideal for power-sensitive multimedia applications because they support a multi-tiered approach to power management that adjusts performance based on system needs. Let's take a look at some of the key power considerations in embedded systems and see how the Blackfin family uses dynamic power management to address them.

What are some typical strategies for saving power?

1. Changing Frequency and Voltage

Modern DSPs are normally designed in a process using CMOS FET switches, which are either fully *on* (and very lightly loaded) or fully *off* (except for leakage currents) during the steady state. The static power dissipation (quiescent power while the processor is idle) is typically much lower than the dynamic power dissipation caused by the charging and discharging of FET load capacitances at very high switching frequencies when the device is actively switching and voltages are slewing.

The charge (Q) stored in the device's equivalent load capacitance equals the capacitance multiplied by the voltage stored across it (which is the DSP's core supply voltage, V_{core}),

$$Q = CV_{core},$$

Since device current to charge this capacitance is defined as the rate of change of charge with respect to time, the dynamic current, I_{dyn}, is given by

$$I_{dyn} = dQ/dt = C(dV_{core}/dt)$$

The rate of capacitor voltage change with respect to time, dV_{core}/dt, is a measure of how fast the capacitor is being charged and discharged. For a given clock frequency, F, the fastest a complete charge or discharge can take place is one clock cycle. Therefore,

$$dV_{core}/dt = V_{core}(F)$$

$$I_{dyn} = C(dV_{core}/dt) = CV_{core}F$$

Finally, dynamic power dissipated is proportional to $V_{core} \times I_{dyn}$, or

$$P_{dyn} \propto CV_{core}^2F$$

Thus, it is apparent that dynamic power dissipation is proportional to the square of operating voltage and linearly proportional to operating frequency. Therefore, lowering F will decrease the dynamic power dissipation *linearly*, while reducing V_{core} will lower it *exponentially* (see Figure 1).

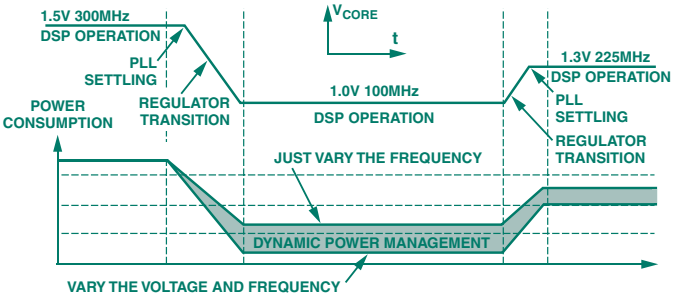


Figure 1. Effects of V and F changes on power consumption.

Consider the three different DSP functions combined in Figure 1, all with very different performance needs:

F0(x)	1.5 V	300 MHz
F1(y)	1.0 V	100 MHz
F2(z)	1.3 V	225 MHz

For instance, F0(x) might be a video-processing algorithm, F1(y) could be a monitoring mode (where the DSP is collecting data and doing minimal processing), and F2(z) might be a process to stream compressed video out of a serial port.

Changing only frequency (and not voltage) in a power-sensitive application is useful when the DSP has an extended period of monitoring activity. That is, if the DSP were waiting for an external trigger, it would not need to run at maximum frequency.

However, in some battery-powered applications, simply changing frequencies may not be enough to save power. For example, if an application is running three sections of code, reducing the operating frequency for any one of these sections means that particular section of code will take longer to execute. But if the DSP is running longer, the same amount of power will be expended when the three sections are complete. If, for example, the frequency is reduced by a factor of two, the code will take twice as long to execute, so no net power savings is realized.

On the other hand, considerable power savings can be achieved by reducing voltage as well as frequency. This savings in power consumption can be modeled by the following equation:

$$P_R/P_N = (F_{CR}/F_{CN})(V_{DDR}/V_{DDN})^2(T_{FR}/T_{FN})$$

where

- P_R/P_N is the ratio of reduced power to nominal power
- F_{CN} is the nominal core clock frequency
- F_{CR} is the reduced core clock frequency
- V_{DDN} is the nominal internal supply voltage
- V_{DDR} is the reduced internal supply voltage
- T_{FR} is the duration running at F_{CR}
- T_{FN} is the duration running at F_{CN}

For example, Figure 2 shows a scenario with the following characteristics:

- F_{CN} = 300 MHz
- F_{CR} = 100 MHz
- V_{DDN} = 1.5 V
- V_{DDR} = 1.0 V
- T_{FR} = 3
- T_{FN} = 1

Thus

$$(P_R/P_N) = (100/300)(1.0/1.5)^2 \times (3/1) = 0.44 \rightarrow 56\% \text{ savings!}$$

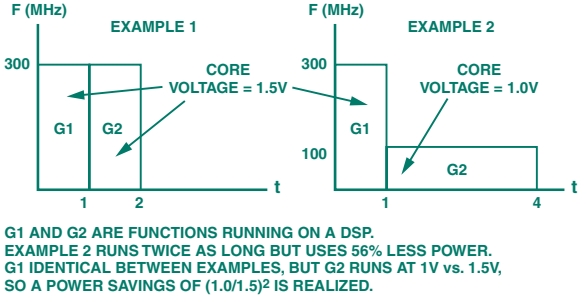


Figure 2. Power dissipation vs. frequency and time.

Since Blackfin DSPs not only have a programmable operating frequency, but also allow core voltage to be changed in concert with frequency changes, less power will be consumed when running a section of code at a lower frequency *and* a lower voltage, even if execution time is longer. The voltage-frequency transition is handled automatically on the ADSP-21532, while for the ADSP-21535, a simple sequence is followed. It is, of course, important to remember that developers must ensure the integrity of peripheral channels connected to external systems during any system clock frequency change.

A videophone application illustrates how the ability to vary both operating frequency *and* operating voltage can be exploited to greatly extend battery life. If, for example, the maximum performance (maximum core clock frequency) is only required during a video connection, the core frequency can be lowered to some preset value when using the phone for a voice-only transaction. For operating time-insensitive value-added features only (e.g., a personal organizer), the frequency can be further reduced. Each of these PLL frequency transitions can be accomplished in less than 40 microseconds on Blackfin DSPs.

IMPLEMENTATION

Blackfin clock generation unit

The *clock-generation unit*, which houses the phase-locked loop (PLL) and associated control circuitry, is an integral element of *dynamic power management* in Blackfin DSPs. The PLL is highly programmable, allowing the user to control the processor's performance characteristics and power dissipation dynamically.

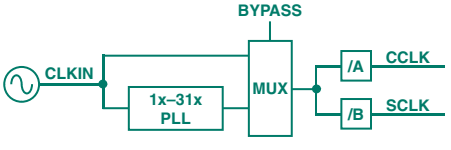


Figure 3. Functional block diagram of ADSP-21532 clock-generation unit.

Figure 3 shows a simplified block diagram of the ADSP-21532 clock generation unit. An input crystal or oscillator signal (10-to-33 MHz) is applied to the CLKIN pin. The PLL then multiplies this signal by a programmable factor of 1× to 31×. Then, separate A and B dividers independently generate core-clock (CCLK) and system/peripheral-clock (SCLK) frequencies. Control logic ensures that the system clock frequency will not exceed the core clock frequency.

The great advantage in this approach is that CCLK and SCLK can be changed "on-the-fly," with very little cycle overhead. Thus, designers need not think twice about changing clock frequencies in order to meet different performance requirements for different segments of their code. The resulting linear savings in dynamic power dissipation comes at no implementation cost, from the designer's perspective.

Another feature of the Clock Generation Unit is that it can be bypassed to allow the CLKIN signal to pass straight through to CCLK. This capability permits use of a very low frequency CCLK during inactive operation intervals, to further reduce overall power dissipation.

2. Flexible Power Management Modes

Many applications involve a set of operating modes that differ markedly with respect to processing needs. Consider the system of Figure 4, where a battery-powered sensor contains a DSP that acts as the central processor. One of the DSP peripherals might be used to sample parameters of the surrounding environment. In this "Mode A," which requires very low processing power, the DSP might be reading in sporadic packets of telemetry data. When it has read enough data to invoke a computational algorithm, the DSP would then enter "Mode B," a processing-intensive computational mode. It is likely that a "Mode C" also exists, to provide ultra-low power dissipation when no sensor information is expected and no processing is required.

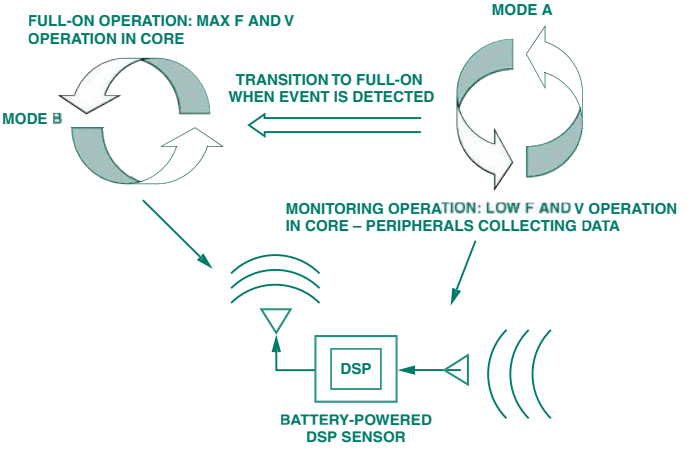


Figure 4. Sample DSP application with different operating modes.

Blackfin DSPs have four distinct operating modes (corresponding to four different power profiles) that provide selectable performance and power dissipation characteristics. Table 1 summarizes the operational characteristics of each mode.

Table 1. Operational Characteristics

Operating Mode	Core Clock	System Clock	Power Savings
Full-On	Enabled	Enabled	Minimum
Active (PLL bypassed)	Enabled	Enabled	Medium
Sleep	Disabled	Enabled	High
Deep-Sleep	Disabled	Disabled	Maximum

Full-on mode

Full-on is the Blackfin's maximum performance mode. In this execution state, the processor and all enabled peripherals run at full speed. The PLL is enabled, so CCLK runs at a multiple of CLKIN.

Active mode

In *Active* mode, the PLL is enabled but bypassed, so CCLK comes directly from CLKIN. Because CLKIN is sourced from an external oscillator input no greater than 33 MHz, this mode offers significant power savings. The system-clock (SCLK) frequency is also reduced, because it never exceeds CCLK. With the PLL bypassed in this mode, it is safe to change the PLL multiplier ratio; however, the changes do not take effect until the DSP is back in *Full-on* mode. In Active mode, not only can the PLL be bypassed—it can be disabled, for incremental power savings.

Sleep mode

The *Sleep* mode significantly reduces power dissipation by disabling CCLK, which idles the DSP core. However, SCLK remains enabled so that data transfer can still take place in L2 memory and peripherals. To exit from Sleep mode, the Blackfin provides a DSP core wake-up capability, which operates independently from the core's *event controller*.

Deep-sleep mode

The *Deep-sleep* mode maximizes power savings by disabling the PLL, CCLK, and SCLK. In this mode, the processor core and all peripherals except the *real-time clock* (RTC) are disabled. In Deep-sleep mode, the DEEP_SLEEP output pin is asserted, to permit external power-mode control. Deep-sleep mode can be exited only by an RTC *interrupt* or *hardware-reset* event. An RTC interrupt causes the processor to transition to *Active* mode; a hardware reset initiates the hardware-reset sequence.

3. Separate Power Domains

Blackfin DSPs support multiple power domains, including a dedicated *phase-locked-loop* (PLL) power domain, a *real-time clock* (RTC) that can be powered by a small, external coin-cell battery, and separate domains for the various peripherals. The core processor also has its own power domain. Using multiple power domains maximizes flexibility while maintaining direct connectivity with a wide variety of commercially available devices, such as SDRAM and SRAM memories. As shown in Figure 5, the separate power domains allow the Blackfin's core voltage to be varied without disrupting connections to external devices. This is a critical advantage, because—as noted above—the power consumed by a processor is proportional to the square of its operating voltage.

4. Using an Efficient Processor Architecture

Another often-overlooked means of reducing power consumption for a given application is to choose an *efficient processor architecture* for that application. Such features as specialized instructions and fast memory structures can reduce power consumption significantly by lessening overall algorithm execution time. Moreover, power-conscious applications make it imperative to structure algorithms efficiently, taking advantage of native architectural features, such as hardware loop buffers and instruction/data caches. This is important—complex algorithms often consume more power, since they use more resources. If an algorithm is optimized, it takes fewer instructions to execute. The sooner it completes all its steps, the sooner the core voltage and frequency can be reduced.

Power consumption can be further optimized in architectures that support selective disabling of unused functional blocks (e.g., on-chip memories, peripherals, clocks, etc.).

Blackfin DSPs provide additional power-control capability by allowing dynamic scheduling of clock inputs to each peripheral. This allows finer control of power dissipation. Also, internal clocks are routed only to enabled portions of the device. For example, on the ADSP-21535, the 256KB on-chip L2 memory consists of eight 32KB banks. These banks are only clocked when they are accessed, a feature that can result in significant power savings.

5. Profiling Tools

Providing yet another way to optimize power consumption, the Blackfin VisualDSP++ tool suite can profile applications to determine the exact processing requirements for each section of an algorithm. The tools allow a system designer, in real time, to quantify how much time is spent in any given code segment. Using this technique in battery-powered applications, the core and system frequencies, as well as the core voltage, can be modified to "match" the minimum values required to perform the task.

6. Intelligent Voltage Regulation

Beginning with the ADSP-21532, Blackfin DSPs provide on-chip core-voltage regulation. The first Blackfin DSP, the ADSP-21535, requires an external power management chip to allow dynamic control of the core voltage levels. The ADP3053 is a companion chip that supports power management for the ADSP-21535. The DSP will use up to 3 pins to control the power levels being provided by the ADP3053. The part allows 100-millivolt core-voltage increments, from 0.9 V to 1.5 V. In addition, the ADP3053 provides a low-noise PLL supply.

CONCLUSION

Designers using DSPs do not have to sacrifice power for performance. There are many alternatives to help them balance these often-conflicting demands. By viewing power management strategically, instead of tactically, significant savings can be achieved. The Blackfin DSP family provides an excellent platform for realizing low-power, high-performance embedded applications.

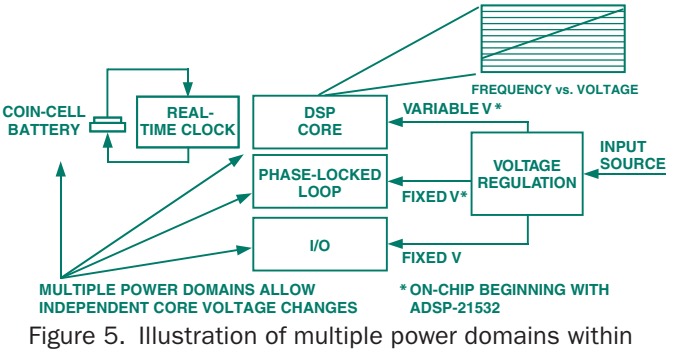


Figure 5. Illustration of multiple power domains within the Blackfin DSP.

Detecting Fast RF Bursts Using Log Amps

by Yuping Toh [yuping.toh@analog.com]

INTRODUCTION

Monolithic logarithmic amplifiers (*log amps*) can handle signals with dynamic ranges up to 100 dB. They are capable of responding to RF bursts that are as short in duration as a few tens of nanoseconds. However, when demodulating logarithmic amplifiers are used to detect fast RF bursts, strange tails sometimes appear at the output when the applied burst shuts off. An example of this was seen in a log amp tutorial article that appeared online in *Analog Dialogue* 33-3 (1999), and in print in Volume 33. This article explains a common cause of these tails and offers suggestions on how to eliminate them.

Understanding Demodulating Logarithmic Amplifiers

The first thing to understand about log amps is that, while they provide information about power, they actually respond to voltage. In communications technology, the term *log amp* generally refers to a device that outputs a voltage that is proportional to the logarithm of the envelope of the input signal, scaled to base-10. A power ratio of 100:1 corresponds to 20 decibels (dB)—or a voltage ratio of 10:1 into a given impedance.

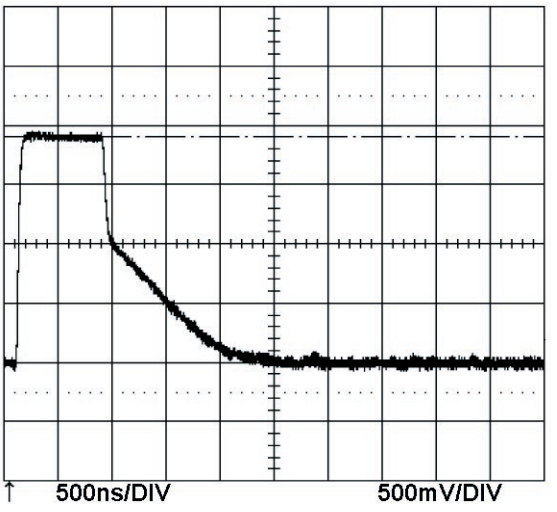
Another important factor relating to log amps and output tails: Log amps have high sensitivity to very small changes in amplitude at the low end of their operating range. Figure 1 shows the typical relationship between the input and output of a log amp. For every 10× increase in the peak-to-peak voltage at the input, the output increases by 500 mV. This means that, when inputs are in the single-digit mV range, a very small change in the input voltage will result in a significant change in the output voltage.

Using Logarithmic Amplifiers for RF Pulse Detection

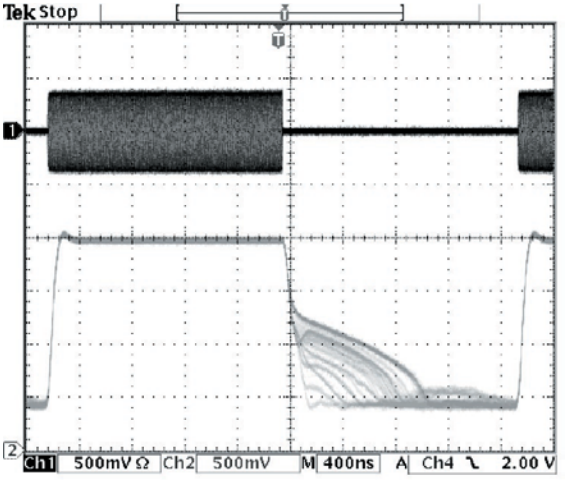
When an RF burst is the input to a demodulating log amp, the output will be a voltage pulse. This can be fed into a comparator to determine the presence or absence of the RF burst, or the amplitude of the RF burst can be determined by measuring the amplitude of the log amp output voltage.

Figure 2 shows examples of the strange *tails* that are sometimes seen at the end of otherwise fast and accurate log amp output-voltage pulses. These undesirable tails can cause false readings in radar and other systems where the shape of the detected pulse provides vital information about the target.

Figure 2a shows a stationary tail. Figure 2b shows a tail that is jittery, moving up and down the falling edge of the ideal rectangular pulse. Note that there are instances where the tail does not occur, but falls directly to the bottom without a kink in the response.



2a



2b

Figure 2. Tails at the output of a log amp in response to RF bursts.

Understanding the Tail

The tails in these two cases are caused by different mechanisms. The stationary tail in Figure 2a is caused by the poor quality of the RF burst applied to the input of the log amp. While not apparent on the modest voltage and time scales of an oscilloscope, the RF burst does not shut off instantaneously, but instead decays exponentially. Figure 3 shows an exaggerated picture of the input signal and the log amp response. Remember that log amps are highly sensitive to small changes in voltage at the low end of their dynamic range. Thus, the small, almost imperceptible, exponential decay of the RF burst causes a linear tail. The exponential decay is predictable and repeatable; it is due to the gating mechanism of the signal generator. This accounts for the stationary tail at the log amp output. The only solution to this form of tail is to obtain a signal generator that will shut off to zero more rapidly.

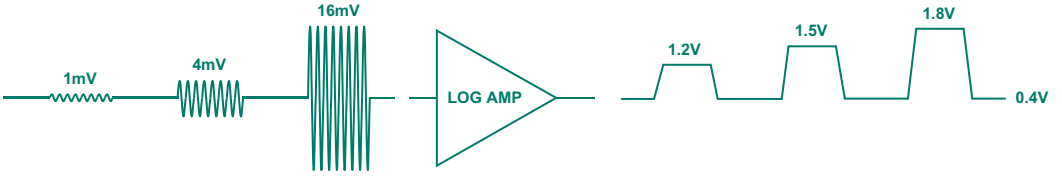


Figure 1. Input bursts and their associated log amp outputs.

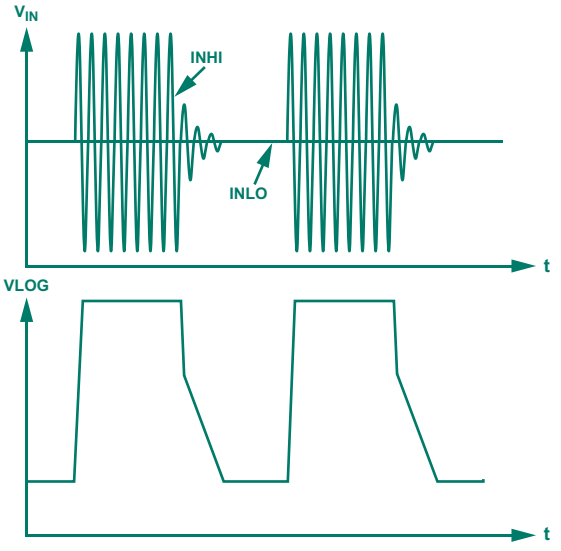


Figure 3. Slow signal settling—the cause of the stationary tail of Figure 2a.

The rest of this article will assume that a good-quality RF burst generator is used—and that the tail is jittery and not stationary.

Input Coupling

The type of jitter shown in Figure 2b is typically the result of improper input interfacing to the demodulating log amp. Most logarithmic amplifiers are designed to be driven differentially, but most RF signals are single-ended. There are several options for performing the single-ended to differential conversion necessary to inject the RF signal into the log amp, as shown in Figure 4. INHI and INLO are the log amp's differential input pins.

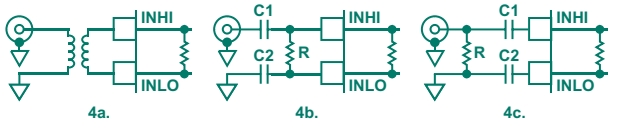


Figure 4. Three passive broadband single-ended to differential input interfaces for a logarithmic amplifier.

Figure 4a shows a *balun* (balance-unbalance-transformer) interface. This is the best method, as it generates a good-quality, truly differential signal at the inputs of the log amp. Use of a balun will eliminate the tails, provided that the size and added cost entailed are acceptable, given the design constraints.

Two popular alternatives involve RC networks. They occupy less board area than a balun and cost less, but they require care to avoid tails. An external shunt resistor is placed on either the device side (Figure 4b) or the input side (Figure 4c) of the capacitors to provide a controlled impedance at the device—usually 50 Ω.

Ideal Signals

Consider first the circuit in Figure 4b (we will return to the somewhat similar circuit of Figure 4c later on). This circuit does not convert the single-ended input signal to a differential signal. Instead, the ac component of the RF signal is allowed to pass through to INHI, while INLO sees a low-pass-filtered version of the signal. Ideally, the signal at INLO will have the same dc average as the signal at INHI. Both INHI and INLO are typically biased by the same internally generated reference voltage, as shown in Figure 5.

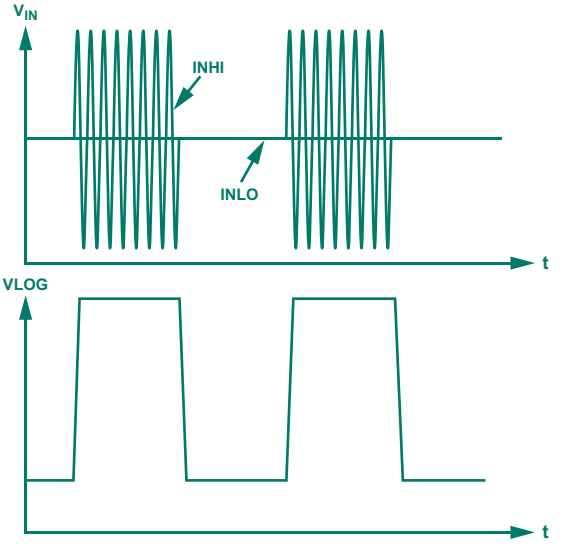


Figure 5. Ideal signals at INHI and INLO when using circuit shown in Figure 4b.

Imperfect Signals

The signals shown in Figure 5 are idealized. The real low-pass filter will attenuate the signal from INHI to INLO, but will not completely eliminate it, and there will be residual traces of the input signal at INLO. Figure 6 shows an exaggerated picture of the signals at INHI and INLO. It can be seen that the real signal at INLO is a highly attenuated version of INHI with a 90-degree phase lag.

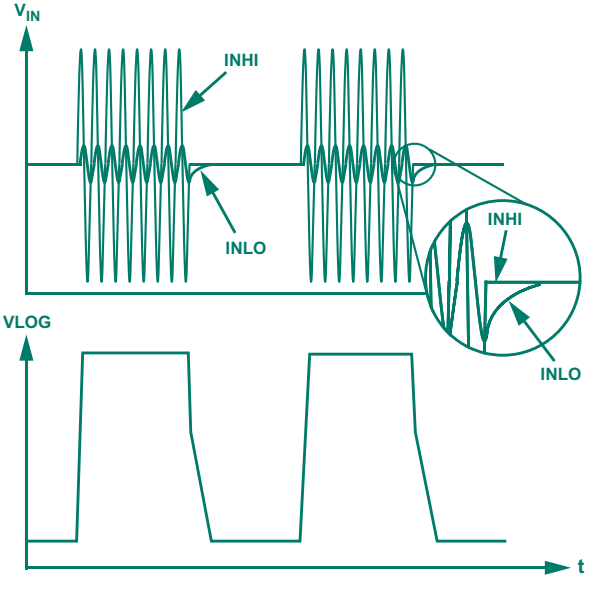


Figure 6. A closer look at signals at INHI and INLO when using circuit shown in Figure 4b.

Looking into the input port, the input signal sees a high-pass filter to INHI. This means that any changes occurring above the corner frequency formed by RC_1 will pass unattenuated to INHI. Thus, when the RF burst turns on suddenly from an off state, the voltage at INHI will track the input. The same will be true for when the RF burst turns off: the voltage at INHI will shut off immediately.

INLO, on the other hand, is a low-pass-filtered version of INHI; as a result, it will be an attenuated version of the voltage at INHI, phase-shifted by 90 degrees. When the RF burst is shut off, the voltage at INHI will settle immediately—but the voltage at INLO will not. It will instead undergo a single time-constant decay, with its time constant defined by RC_2. This is illustrated in the magnified section of Figure 6 (note that the scale of the INLO signal has been exaggerated for effect).

Source of the Tail

The tail is the result of the exponential decay of the signal at INLO. While INLO is decaying exponentially, INHI is off. The small differential input that the log amp sees between INHI and INLO is enough to result in a significant amount of output voltage. (Remember that the log amps are highly sensitive to small input amplitude changes.)

Further evidence that the tail is the result of exponential signal behavior at the input is given by the linear nature of the tails. When the log of an exponentially decaying voltage is generated, the result is a straight line with a negative slope. The jitter in the output occurs when the pulse rate and the RF frequency are not integer multiples of one other. Because of this, the RF signal is not always cut off at the same place in its period. The point in a period where the RF is shut off will establish the initial condition for the exponential decay. When the RF is shut off exactly as it crosses the zero-axis, INLO will be at a peak and the tail will start at its highest point. If the RF is shut off at a peak, then INLO will be zero and there will be no tail at all. Switching randomly between these two extremes will cause the jitter that is seen in the tail.

Cutting the Tail Off

The tail problem described above can be solved by making sure that the RC time constants formed by R, C_1, and C_2 are set appropriately. The critical time constant is that of the low-pass formed between R and C_2. The value of R is typically chosen to be about 50 Ω for matching purposes. For convenience, C_1 and C_2 are often chosen to be equal, though not always.

C_2 must be chosen to be small enough so that the exponential decay is faster than the response time of the log amp, typically specified as the 10% to 90% risetime of the log amp output to a step increase in the input power. This number establishes the maximum rate of change of the output voltage. As long as the exponential decay at INLO is faster than the maximum rate of change, the output will be limited by the log amp's own slew rate, and the tail will not appear. This analysis dictates that C_2 be as *small* as possible.

But if C_2 is made as small as possible, and C_1 is made equal, the corner frequency of the high-pass filter formed by R and C_1 will be pushed so far out that it might attenuate the desired RF signal as it travels from the input to INHI. To ensure that INHI is not attenuated going from the input to INHI, C_1 must be chosen so that the product of R and C_1 forms a corner frequency that is below the RF frequency. This dictates that C_1 should be *large*.

Within these bounds, C_1 and C_2 can be made equal, or they may be chosen to be different for optimum results.

Should the 50-Ω Resistor be on the Signal Side or the Device Side?

The analysis so far has centered on Figure 4b. The circuit in Figure 4c is similar, except that the input resistor is on the input side of the capacitors. Remember that the input impedances of the log amps are typically much higher than the 50 Ω of the termination resistor. If the 50-Ω resistor is placed on the device side of the capacitors C_1 and C_2, as in Figure 4b, the net impedance between INHI and INLO is about 50 Ω. But if the termination resistor is placed on the input side of C_1 and C_2 (Figure 4c), the impedance between INHI and INLO is the input impedance of the device.

The problem with having the termination resistor on the signal side is that the higher internal resistance of the device will require a much smaller value of C_2 to ensure elimination of the tails. Also, if the input resistance is not predictable, varying with the semiconductor manufacturing process, the choices for C_1 and C_2 may not always ensure tail-free operation.

Thus, placing the termination resistor on the device side of the capacitors is preferred.

Results

Figure 7 shows the result of choosing the proper capacitance values. The output shown in Figure 2b was taken with 10-nF input capacitors, while the output in Figure 7 was taken with 1-nF capacitors. A factor of 10 capacitance reduction has made a huge improvement in the output quality.

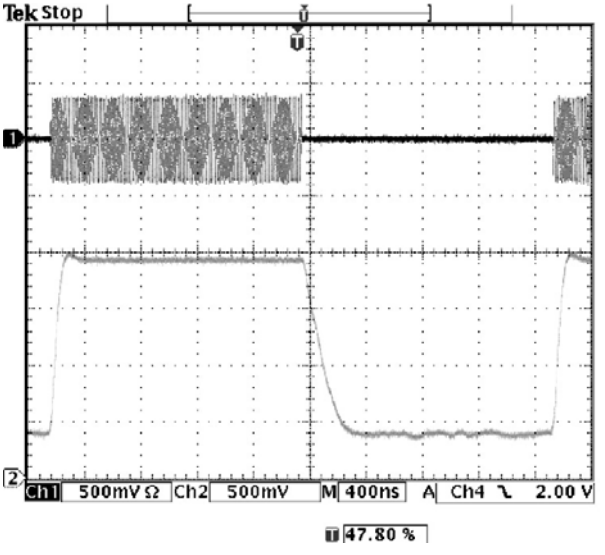


Figure 7. Tail-free output of a DLA after a change in capacitor values.

CONCLUSION

The performance of demodulating log amps need not be hampered by the presence of tails. They occur because of poor-quality signal sources or because of the improper selection of component values in the input interface. The most effective solution for the first form of tail is to obtain a better source of bursts. The second type of tail can be dealt with using proper interfacing circuits. Techniques include the use of baluns and passive RC circuits, as described here. Active solutions, such as single-ended to differential amplifiers are also available to the designer (but they were not covered here). Whatever method is chosen, it is important to keep in mind the issues discussed here.

FOR FURTHER INFORMATION

http://www.analog.com/technology/amplifiersLinear/logAmps/index.html

High Speed Op Amp Drives a 16-Bit, 1-MSPS Differential-Input A/D Converter

by Alain Guery [alain.guery@analog.com] and
Charles Kitchin [charles.kitchin@analog.com]

INTRODUCTION

Modern high resolution analog-to-digital converters (ADCs) usually require input buffer amplifiers (ADC *drivers*), because they often present a dc load of several hundred ohms or more—and a high frequency dynamic load—to the source that is driving them. If the source is a transducer or a typical low frequency preamplifier, significant errors may occur.

The ADC driver is a high performance fast-settling op amp with input impedance of (at least) several megohms and a low impedance output circuit that is capable of driving dynamic loads with minimal errors. In addition to buffering, the driver can also provide input scaling (gain) and low-pass filtering to reduce system noise. Some designs can also translate from single-ended sources to differential-input ADCs.

In order for the ADC driver to maintain system accuracy, its settling time, noise, and total harmonic distortion (THD) must be considerably better than that of the ADC itself. This is a significant challenge for the designer in systems employing fast 16- or 18-bit successive approximation (SAR-type) A/D converters.

Settling-time requirements

In order to use the full sampling rate of which an ADC is capable, the combined settling time for the op amp and ADC for a full-scale step input to within 1 LSB must be less than the ADC's specified sampling rate. This is especially critical in applications where the amplifier and ADC are acquiring diverse input values from several multiplexed sources. This window can be as short as 1 µs when using fast, high resolution ADCs, such as the 16-bit, 1-MSPS AD7677 (true differential input) and AD7671 (true bipolar input)—or about 1.25 µs with the 18-bit, 800-kSPS AD7674.

In the search for an amplifier to use as an ADC driver, it is unfortunate that—because of the extreme care required in measuring settling time—most op amp data sheets specify the settling time to only 0.1% or 0.01% of full scale, rather than the 0.0015% required for 16-bit accuracy—or the 0.0004% required for 18-bit accuracy. Thus, actually settling to within 1 LSB of 16 bits will normally require significantly more time than the data sheet specification. The AD8021 op amp, with a nominal settling time of 23 ns to 0.01%, allows the user to custom-compensate it (see Appendix) to achieve the maximum bandwidth, lowest noise, and minimum THD (total harmonic distortion) for a given closed-loop gain. This combination also allows it to meet stringent settling time specifications, even when operated at gains substantially higher than unity.

Noise requirements

The noise generated by an ADC driver amplifier needs to be kept as low as possible in order to avoid worsening the signal to noise ratio (SNR) and the transition noise performance of the 16-bit ADC. When using the AD7671, the op amp driver noise is first scaled down by the resistive divider inside the ADC. The noise is then filtered by the ADC's analog input circuitry.

The net SNR degradation (in dB) due to the amplifier will be:

$$SNR_{LOSS} = 20\log\left(\frac{N_{ADC}}{\sqrt{{N_{ADC}}^2 + \frac{\pi}{2} f_{-3dB}\left(\frac{2.5 N e_n}{FSR}\right)^2}}\right)$$

where:

N_{ADC} is the rms noise of the ADC in microvolts

f_{-3dB} is the –3-dB input bandwidth of the ADC in MHz (or the cutoff frequency of the ADC input filter, if used)

N is the noise gain of the amplifier (1 if in unity-gain buffer configuration).

e_N is the equivalent input noise voltage spectral density of the op amp in nV/√Hz.

FSR is the full-scale input span of the ADC (e.g., 5 V for a ±2.5-V range).

For example, assume that the 16-bit AD7671 is being driven by an AD8021 op amp. The ADC has 28-µV rms noise, 9.6-MHz bandwidth, and a 0-to-5-V input range. The op amp has an equivalent input noise of 2 nV/√Hz, and a noise gain of +1, when configured as a unity gain buffer, so the SNR of the ADC will be degraded by only 0.08 dB.

Distortion requirements

The input source usually needs a buffer amplifier with low output impedance for isolation from the ADC's input impedance. This buffer's output impedance affects the ac performance of the ADC, especially the level of *total harmonic distortion* (THD). A high source impedance increases THD, because the input impedance of an ADC with inputs swinging 2.5 V will usually have tangible nonlinear input capacitance.

The THD is degraded proportionally to the source impedance. The maximum allowable source impedance in series with the ADC's input depends on the amount of total harmonic distortion (THD) that can be tolerated. The ADC driver also needs to have very low inherent THD, well below that of the ADC (i.e., better than 16-bit accuracy). The combined THD level of the AD7671/AD8021 is typically –100 dB at both 20 kHz and 250 kHz. Figure 1 is a typical plot of THD and the major distortion components as a function of input level for this pair, with the ADC driven from 0 V to 2.5 V.

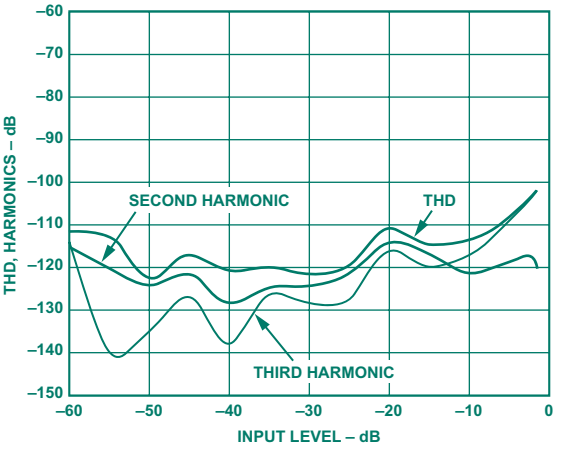
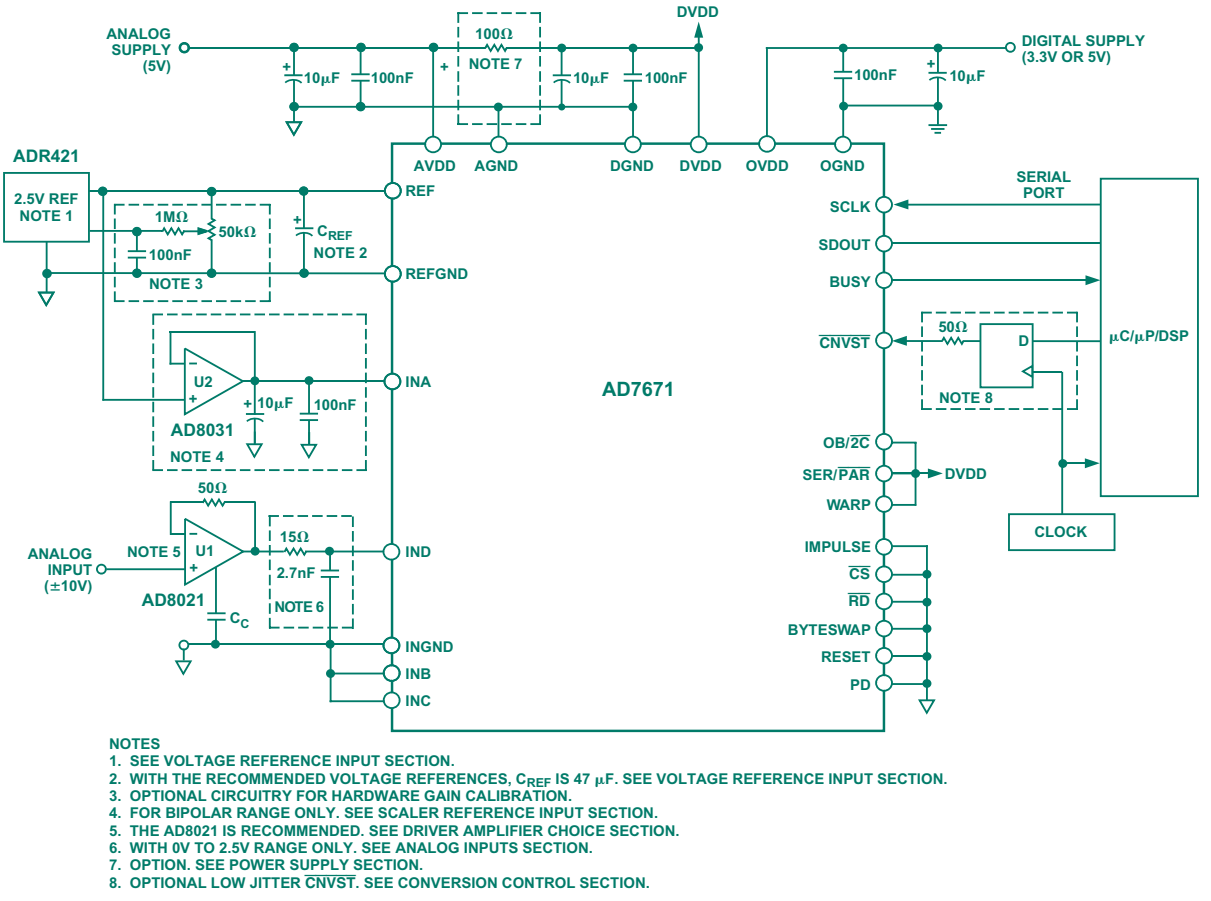


Figure 1. THD, second and third harmonics vs. input level for AD7671/AD8021 ADC/driver combination.



NOTES
1. SEE VOLTAGE REFERENCE INPUT SECTION.
2. WITH THE RECOMMENDED VOLTAGE REFERENCES, C_{REF} IS 47 µF. SEE VOLTAGE REFERENCE INPUT SECTION.
3. OPTIONAL CIRCUITRY FOR HARDWARE GAIN CALIBRATION.
4. FOR BIPOLAR RANGE ONLY. SEE SCALER REFERENCE INPUT SECTION.
5. THE AD8021 IS RECOMMENDED. SEE DRIVER AMPLIFIER CHOICE SECTION.
6. WITH 0V TO 2.5V RANGE ONLY. SEE ANALOG INPUTS SECTION.
7. OPTION. SEE POWER SUPPLY SECTION.
8. OPTIONAL LOW JITTER $\overline{\text{CNVST}}$. SEE CONVERSION CONTROL SECTION.

Figure 2. A single-ended-input 16-bit data acquisition system. References in Notes are to sections of the AD7671 data sheet.

A *single-ended* 16-bit ADC driver circuit

Figure 2 shows a complete 16-bit data-acquisition system consisting of an AD7671 ADC and an AD8021 op amp, used as a driver amplifier, U1. The input signal is buffered by U1, which is operated as a low noise unity-gain follower; its high input impedance allows a multiplexer or a passive filter to be used ahead of the op amp.

A 50-ohm feedback resistor is used to prevent the AD8021 from ringing. An optional low pass filter, consisting of a 15-ohm resistor and 2.7-nF capacitor, lowers the noise bandwidth of the op amp and also serves as an anti-aliasing filter.

The reference voltage source is a low-temperature-coefficient ADR421. If desired, the reference voltage can be hardware adjusted with the optional circuit described in Note 3 in Figure 2. Because this ADC is based on charge redistribution, its reference input should be properly bypassed to minimize current spikes. The AD7671 uses three sets of power supply pins: an analog +5-V supply (AVDD), a digital +5-V core supply (DVDD), and a digital input/output interface supply (OVDD). The OVDD supply allows direct interface with any logic voltages between 2.7 V and 5.25 V. The number of supplies can be reduced by powering the digital core (DVDD) from the analog supply, using a simple RC low-pass filter as shown.

Figures 3 and 4 illustrate the dynamic performance of the system. The FFT plot in Figure 3 shows the output spectrum of the ADC for a 45-kHz input waveform. Figure 4 shows the THD and the second and third harmonic distortion products of the ADC, as well as the *spurious-free dynamic range* (SFDR), over frequency. SFDR is defined as the difference, in decibels, between the rms amplitude of the input signal and its peak spurious output level.

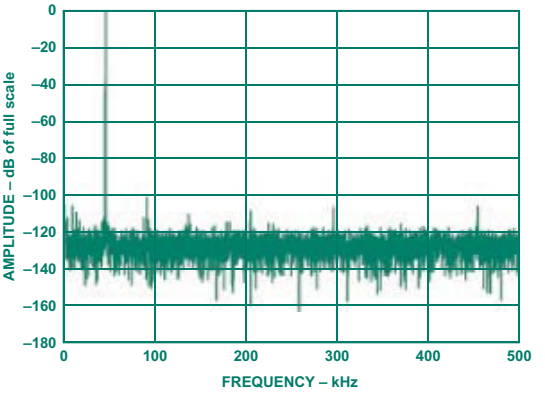


Figure 3. FFT plot of AD7671/AD8021 combination.

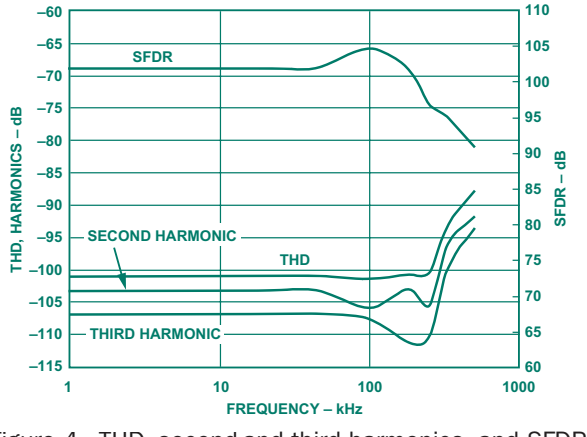


Figure 4. THD, second and third harmonics, and SFDR vs. frequency. SFDR scale is at right.

A *differential* 16-bit ADC driver circuit

The AD7677 is a 16-bit ADC that accepts and processes differential input voltages. Its reference, interface, and power-supply connections are all essentially the same as for the single-ended ADC, as shown in Figure 2. The use of a true-differential input signal will always result in the lowest possible system noise and therefore provide the highest resolution. However, when the input signal is differential, it is essential to use a very low noise op amp input buffer, such as the AD8021, to provide common-mode noise rejection.

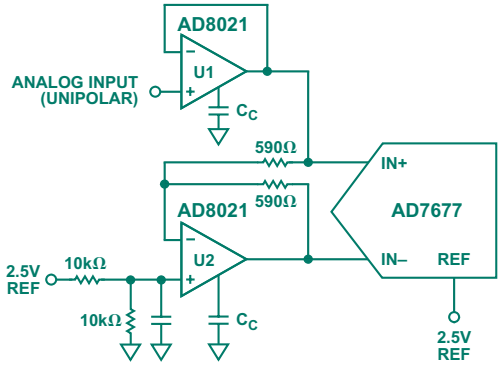


Figure 5. A single-ended to differential-input ADC driver circuit.

The circuit of Figure 5 allows the use of a single-ended transducer with this differential-input ADC. It uses two AD8021 op amps. U1 functions as a unity gain buffer. The output of U1 drives the IN+ input of the AD7677 ADC. (A similar circuit can be used to drive the 18-bit AD7674 ADC, which is pin compatible with the AD7677.) The output of U1 also drives the inverting input of the second op amp, U2, which inverts the signal and drives the IN- input pin of the ADC. U2 is operated at a noise gain of 2, a gain low enough to minimize noise without sacrificing THD performance. The offset reference is applied to the noninverting input of U2 through a 2:1 voltage divider. With a 0 to 2.5-V source, this circuit provides a ±2.5-V differential input swing (U1: 0 to +2.5 V and U2: +2.5 V to 0). The mid-scale common-mode offset voltage is 1.25 V. Figure 6 shows the AD7677's typical common-mode rejection (CMR = 20 logCMRR) as a function of frequency.

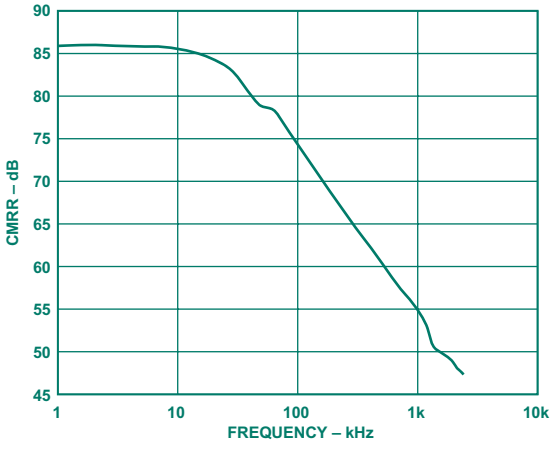


Figure 6. Typical CMR vs. frequency—AD7677/AD8021 combination.

During the acquisition phase, the AD7677 ADC looks like a one-pole RC filter for ac input signals; it consists of internal analog input resistors, R+ and R–, nominally 168 ohms, and an internal capacitance, C_S. The resistors, R+ and R–, consist of some series resistance plus the on resistance of the switches. The ADC's sampling capacitor, C_S, is typically 60 pF. This filter, with a typical –3-dB cutoff frequency of 15.8 MHz, reduces undesirable aliasing effect and reduces high frequency noise coming from the external input circuitry.

Because the input impedance of the AD7677 is very high, the AD7677 can be driven directly by a low impedance source without gain error. This allows further filtering, using (for example) an external one-pole passive RC filter between the outputs of the amplifiers and the input of the ADC. This further improves reduces the noise reaching the ADC's analog input circuit.

Layout, decoupling, and grounding: Guidelines for high resolution data acquisition

Most high performance ADCs, such as the AD7671, AD7677, and AD7674, have very good immunity to noise on the power supplies. However, the printed circuit board (PCB) that houses the ADC should be designed so that the analog and digital sections are separated, each confined to different areas of the board. Digital and analog ground planes should also be separated, with only one common connection point—preferably underneath the PC board, and located as close as possible to the ADC. Crossover of digital and analog signal wiring should be avoided.

If the ADC is in a system containing multiple analog and digital ground connections, these should still have only a single connection point, using a "star ground"—again located as closely as possible to the ADC. Also, avoid running any digital lines under the ADC, as these may couple noise onto the IC. Instead, run the analog ground plane under the ADC.

High speed clock signals and other waveforms with fast edges should be connected to other circuitry using shielded lines. Close traces on the PC board should run at right angles to each other. The power supply lines should use as large a trace as possible, to provide a low inductance path. Power-supply decoupling capacitors, typically 100 nF ceramic, should bypass the IC, wired as closely as possible to its power supply and ground pins. Additionally, 10-μF bypass capacitors should be used, to further reduce low frequency ripple. The location of the *reference-voltage* decoupling capacitor is also important. It should be close to the ADC and connected with short, large traces to minimize any parasitic inductance.

The ADC's ground pins also require attention to detail. ADCs such as the AD7671 and AD7677 each have five different ground pins: INGND, REFGND, AGND, DGND, and OGND. Each is used to sense an individual input or reference line. INGND (analog input ground) is used to sense the analog input signal. REFGND (reference input analog ground) senses the reference voltage; it should be a low impedance return to the reference, because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane, depending on the configuration. The OGND (input/output interface digital power ground) is connected to the digital system ground.

APPENDIX

About custom-compensated op amps

Almost all op amps produced today use internal frequency compensation. This usually consists of an internal compensation capacitor, which provides negative voltage feedback. It is, in effect, part of a single-pole low-pass filter, which causes the op amp's open-loop gain to roll off at a rate of 20 dB (10×) per decade as frequency increases. Since most op amps are designed to operate

over a wide range of closed-loop gains, including full feedback, this internal capacitor needs to be made large enough so that the amplifier is always stable. Because of this conservative design for stability at unity-gain operation (or for the op amp's minimum specified gain)—and the inverse gain-bandwidth relationship—the capacitance limits the bandwidth excessively if the amplifier is to be operated at higher gains.

For example, if the usual internally-compensated op amp has a –3-dB bandwidth of 200 MHz operating at unity gain, its bandwidth at a gain +10 will only be about 20 MHz. However, if this same op amp had used a much smaller compensation capacitor, it could have provided full bandwidth at this higher gain, but it would be unstable and oscillate if operated at lower gains. So, this need to maintain stability at low gains sacrifices both bandwidth and slew rate at higher gains. Although so-called "current-feedback" op amps do tend to maintain their bandwidth over a wide range of gains, they typically will have far higher noise levels than a voltage-feedback amplifier. They also have unbalanced input impedances (the plus input is, in effect, a transistor base circuit; and the minus input is an emitter).

The AD8021 is a "custom-compensated" op amp that solves this gain vs. bandwidth performance dilemma. It uses a small internal compensation capacitance of about 1.5 pF to provide stability at gains of 10 or greater. It also features a *compensation pin* to allow the user to add the optimum external capacitance for any desired gain or load condition.

The ability to custom compensate this op amp provides an unbeatable performance combination of wide bandwidth, high slew rate, and low noise. The tradeoff between bandwidth and the ability to drive capacitive loads may also be optimized for a particular application.

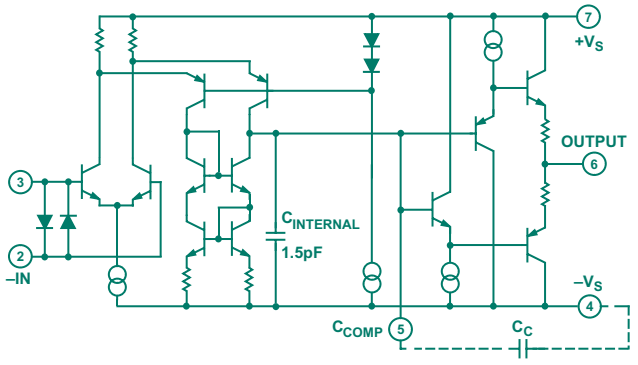


Figure 7. AD8021 simplified schematic.

Figure 7 shows a simplified schematic of the AD8021. The input stage is an NPN differential pair operating at 1.6-mA total collector current. This current level provides high input-stage transconductance with low input noise (2.1 nV/$\sqrt{\text{Hz}}$ @50 kHz). The input stage drives a folded cascode and a current mirror to provide the usual differential to single-ended conversion. The external compensation capacitor is connected between a high impedance node, at Pin 5, and the negative supply line. The output stage has a current gain of 5,000, which maintains the high impedance at Pin 5, even when the amplifier is driving heavy loads. Two internal diode-clamps protect the inputs (Pins 2 and 3) from large input transient voltages, which might otherwise cause an emitter-base breakdown—and increase input offset voltage and input bias current.

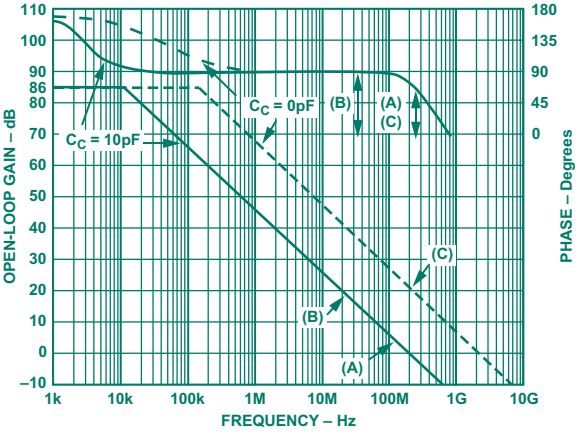


Figure 8. AD8021 open-loop gain and phase vs. frequency.

Table 1 lists recommended values of resistance and compensation capacitance, and corresponding dynamic performance, for several common closed-loop gain values. Note that the value of the compensation capacitor depends on the circuit noise gain, i.e., its net gain for signals applied to the + input.

As with any high speed op amp, printed circuit board layout is critically important. The use of a hand-wired prototyping board or through-hole components will most likely cause the AD8021 to oscillate, because of excess lead inductance. For this reason, the use of a low cost evaluation board (part number AD8021AR-EVAL) and surface-mount components is highly recommended. The NP0 ceramic chip-capacitors (0805 size) specified in Table 1 are available from Digi-Key Corporation, part numbers PCC020CNCT-ND (2 pF), PCC070CNCT-ND (7 pF), PCC100CNCT-ND (10 pF).

Table 1. Recommended Component Values.
See Test Circuit 2. CF = CL = 0, RL = 1 kΩ, RIN = 49.9 Ω

Noise Gain	RS (Ω)	RF (Ω)	RG (Ω)	C_{COMP} (pF)	Slew Rate (V/s)	–3 dB SS BW (MHz)	Output Noise (AD8021 only) (nV/$\sqrt{\text{Hz}}$)	Output Noise (AD8021+R's) (nV/$\sqrt{\text{Hz}}$)
1	75	75	NA	10	120	490	2.1	2.8
2	49.9	499	499	7	150	205	4.3	8.2
5	49.9	1 k	249	2	300	185	10.7	15.5
10	49.9	1 k	110	0	420	150	21.2	27.9
20	49.9	1 k	52.3	0	200	42	42.2	52.7
100	49.9	1 k	10	0	34	6	211.1	264.1

Single-Chip Digitally Controlled Data-Acquisition as Core of Reliable DWDM Communication Systems

by Mark Malaeb [mark.malaeb@analog.com]

The recent lifting of government regulations on the communications industry has fueled an explosion of new ideas and inventions, especially in the optical space. Many players, from startups to Fortune 500 companies, participated in the 1998 to 2000 growth period in an attempt to implement these ideas. Today, although the industry is going through a painful period and many of the startups are gone, the need for implementing these ideas and inventions is still alive and well.

Optical fiber is the transport medium that has emerged to accommodate the expected long-term growth. In order to make the most of the wide bandwidth, which is the principal advantage of fiber transport, a method called *wave-division multiplexing* (WDM)—and later, *dense* WDM (DWDM)—was implemented. This method of transmission allows the transport of multiple wavelengths (one wavelength—or color—per laser) through a single fiber, but imposes stringent requirements on lasers.

One major requirement is that the laser temperature be held constant so that its wavelength will not drift and interfere with other lasers. This usually involves a *thermoelectric-cooler* (TEC) controller (addressed later in this article). Controlling the laser power level and its modulation mechanism over time and temperature is another system requirement. This job is handled by the *laser-diode driver* (LDD). For long-haul applications, optical amplifiers are needed for signal reconditioning and retransmitting. *Erbium-doped fiber amplifiers* (EDFAs) and Raman amplifier types predominate. They recondition the signal without having to convert it from optical to electrical, and then back to optical—which was the widely used method (and only option) in the past. The amplification is now done solely in the optical domain. However, to control their parameters, optical amplifiers, need high-end *A/D and D/A converters* (ADCs and DACs), logarithmic amplifiers (log amps), and *transimpedance amplifiers* (TIAs), plus a controller.

Optical Communication Systems

Most optical communication systems (Figure 1) use ADCs and DACs in the control loops used for the *thermoelectric cooler* (TEC), laser diode driver (LDD), and *avalanche-photodiode* (APD) monitoring and biasing circuitry. Dedicated control loops are used for driving the pump laser and reading its power level; adjusting the *extinction ratio* and *average power* in the transmit laser diode; and maintaining the laser diode at a stable temperature in WDM and DWDM systems. Loop signals are digitally processed by a *microcontroller.* Containing all these tasks in its portfolio, the ADuC832, a member of the MicroConverter® family—an integrated data-acquisition chip, combined with a CPU core and standard peripherals—is a strong candidate to serve as the heart of such control systems.

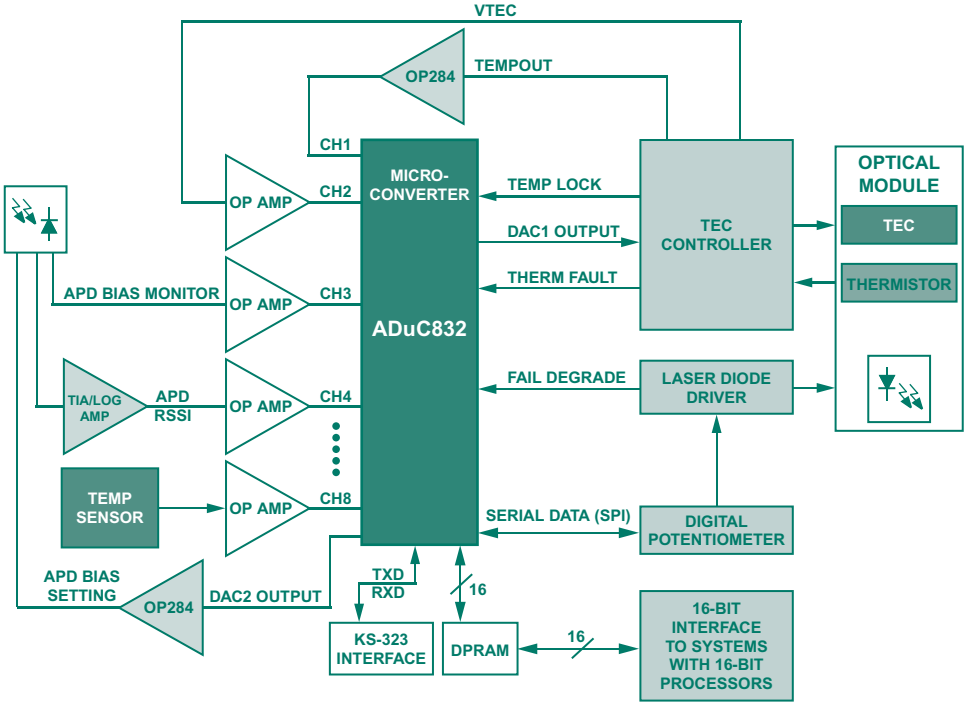


Figure 1. Overall system block diagram.

The ADuC832 (Figure 2) includes: an 8-channel, 12-bit, 5-µs self-calibrating ADC; a 2-channel, 12-bit DAC with rail-to-rail outputs; an industry-standard 8052 microcontroller; 62 Kbytes of Flash program-RAM, and a host of peripheral functions. All of these features, plus a temperature monitor, programmable PLL clock, voltage reference, synchronous and asynchronous serial ports—and more—are integrated into a space-saving 56-lead *chip-scale package* (CSP), allowing the entire control system to fit within the housing of an optical module.

We describe here the possible practical implementation of the various portions of an optical communication system, as shown in Figure 1, including a thermoelectric-cooler controller, laser-diode drivers (LDDs), photodetector-diode biasing, received optical signal-strength indicator (RSSI), and temperature sensors.

Complete, fully tested software modules are available for each of these applications. These modules are written and commented especially for analog/optical designers who are not software savvy and never want to be. This will help cut design time and overall time to market for both experienced and novice programmers.

TEC Controller

To ensure wavelength stability, the thermoelectric-cooler (TEC) controller is designed to maintain a laser diode or optical module at a specific temperature, with precision typically to within 0.01°C. This device relies on a negative-temperature-coefficient (NTC) thermistor to sense the temperature of the object attached to the TEC. The target temperature is set with an analog input voltage—either from a DAC, as shown in Figure 3, or with an external resistor divider. A positive or negative current is applied to the TEC, either heating or cooling the object as required. An internal proportional-integral-derivative (PID) compensation amplifier stabilizes the temperature. An external PID network can be adjusted to optimize the settling time.

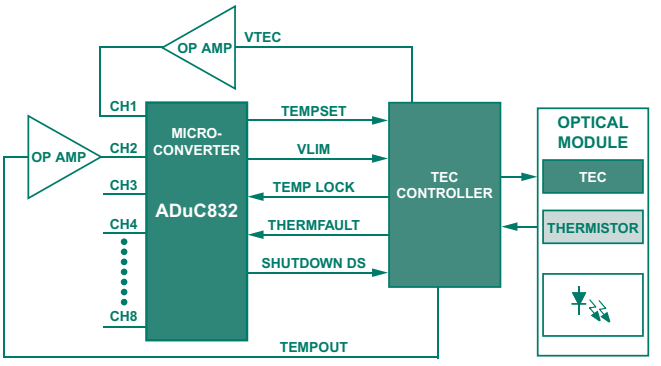


Figure 3. The MicroConverter sets the TEC target temperature and monitors its performance.

One of the 12-bit DACs, connected to the TEMPSET pin, sets the target temperature. The voltage corresponds to a specific target temperature (typically 25 mV/°C for most laser diode applications). The TEC, through its PID loop, maintains the target temperature to within 0.01°C (naturally, this value is dependent on the thermistor quality and suitable care). To protect the thermoelectric cooler from overvoltage, a maximum voltage is specified at the VLIM pin. This voltage is supplied and set by the second 12-bit DAC (typical range 0-to-1.5 V) or by a simple resistance-divider network. The VTEC pin is connected to one of the eight ADC channels, allowing the actual voltage across the TEC to be monitored. The TEMPOUT pin is connected to the second ADC channel, allowing the TEC temperature to be dynamically monitored (typical range 0-3 V). An op amp (OP184, OP162, etc.) is used ahead of each of the ADC inputs for signal scaling, buffering and filtering, if needed. Two digital inputs are used: TEMPLOCK indicates that the desired TEC temperature has been reached; THERMFAULT is used to

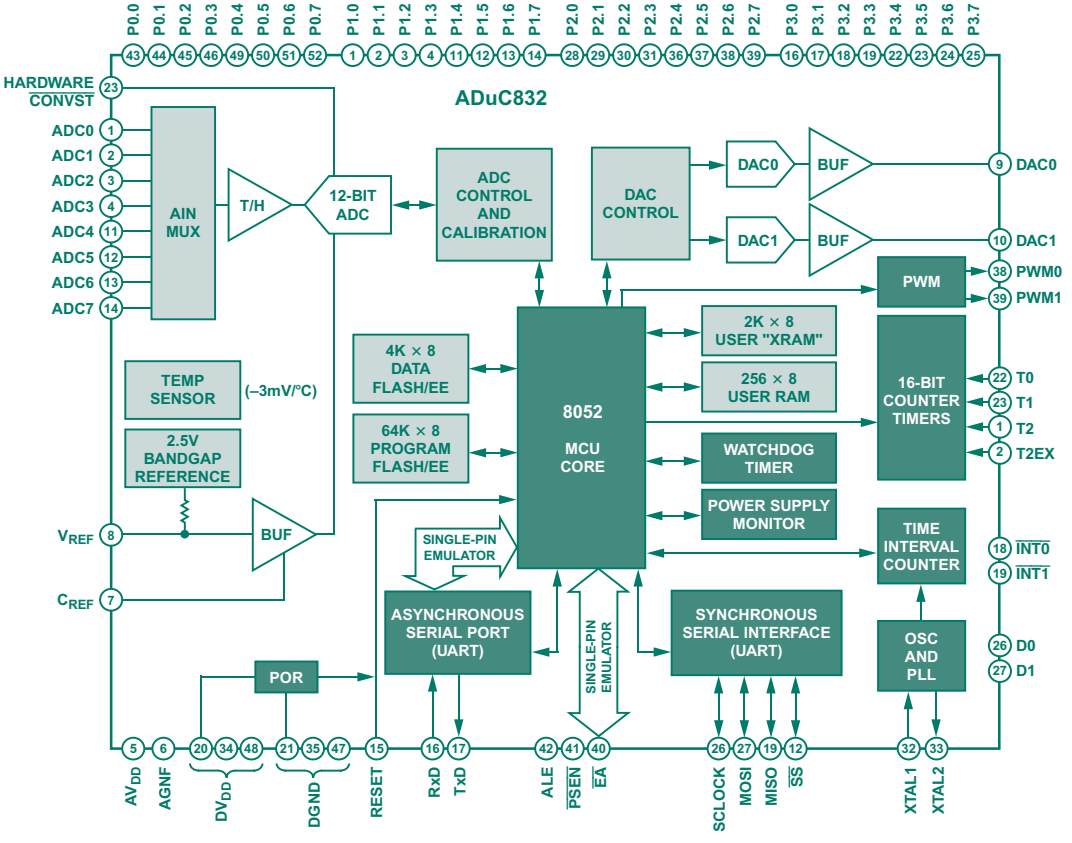


Figure 2. MicroConverter block diagram.

indicate a thermistor malfunction. One digital output is connected to the SD pin, allowing the device to be put into a low-current shutdown mode.

Laser Diode Driver

As part of the system, a laser-diode driver (LDD), the ADN2841, is used to control both average power and extinction ratio of the laser diode using a dual-loop control scheme. The extinction ratio is controlled as a function of modulation current, while the average power is controlled by the bias current. This dual loop configuration compensates for the variation in laser diode slope efficiency due to temperature, aging and diode-to-diode production tolerances, and enhances the designer's ability to source laser diodes from multiple manufacturers.

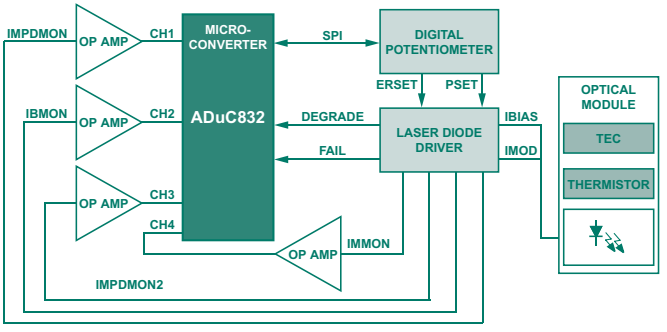


Figure 4. The MicroConverter sets the average power and extinction ratio of the laser diode, and monitors alarms.

The MicroConverter is used for both control and monitoring. Figure 4 shows that the extinction ratio (at the ERSET pin) and the average power (at the PSET pin) are set using an ADN2850 dual 10-bit digital pot. This pot is controlled through the *serial peripheral interface* (SPI) port. The monitor photodiode currents, IMPDMON and IMPDMON2, flow to ground through 1.5-kΩ resistors to provide voltages proportional to the monitor currents. The diode's modulation and bias currents, IMMON and IBMON, flow to ground in the same way. The voltages developed across these resistors are connected to the ADC channels, making them available in a digital format. The ADN2841 has active high monitoring alarms to identify degraded-diode and failed diode conditions. These two digital outputs are connected to two general-purpose I/O pins.

APD Monitoring and Biasing

Avalanche photodiodes are known for their extreme sensitivity and high internal gain. These characteristics make them ideal for optical receiver applications that require optimum sensitivity. Unfortunately, such high gains necessitate bias voltages ranging from 40 to 60 volts. The designer must also deal with the fact that the APD gain function is temperature dependent. The gain can be held constant by adjusting the APD bias voltage as the temperature changes. Figure 5 shows how an ideal solution to this problem can be implemented with a DAC, a switching regulator, and an adjustable voltage booster circuit.

The gain can be held constant by increasing the APD bias voltage as the temperature increases, as specified by the APD manufacturer. This change is typically expressed in %/°C, and ranges from 0.15%/°C to 0.30%/°C.

The ADP3031 switching regulator can provide output voltages of up to 12 volts. Several ADP3031 boost stages can be cascaded to achieve the desired final voltage.

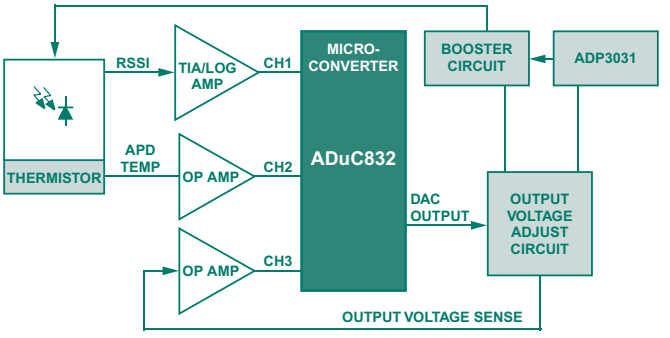


Figure 5. The ADuC832 controls the APD biasing and gain, and reads the received signal strength indicator.

A DAC is used in the range of 0-to-2 V to vary the voltage across the diode with temperature. The actual voltage across the diode can be monitored with the A/D, thus providing complete closed-loop control. With the diode gain maintained at its target, the received optical signal strength can then be accurately monitored with a transimpedance amplifier (TIA) or a log amp plus another channel of the ADC. Calibration coefficients can be conveniently stored in Flash data memory, enabling adjustments to be made as needed.

The 16-Bit Interface

This interface is accomplished using general-purpose I/O ports 0 and 2, plus an external latch. It serves two main functions: as a memory interface for the ADC when it is run in direct memory access (DMA) mode; and as a general-purpose 16-bit peripheral interface through the use of a dual-port RAM or other type of memory. Figure 6 shows the details of such a configuration.

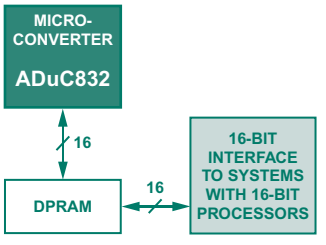


Figure 6. The MicroConverter and its 16-bit interface for data exchange.

The ADC runs at a maximum update rate of one conversion per 5 µs. At this rate, the microcontroller has 5 µs to read the ADC result and store it in memory for further processing. It has to be done within this time interval or the next sample will be lost—especially time-consuming when using an interrupt routine for the ADC. Thus, in applications where the MicroConverter cannot service a very fast interrupt rate, DMA mode should be used. In DMA mode, ADC results are written directly to external memory.

Like any standard 8051-compatible controller, this 16-bit interface can be used to exchange data with systems running a 16-bit processor. The dual port memory helps prevent bus altercation and contention—and provides a somewhat independent interface system. Because "real estate" (circuit-board area) is critical in most optical modules, integration of ADCs, DACs, Flash memory, and an 8052 MCU in a 56-lead CSP package provides the designer with a compact and powerful solution for optical communication systems.

Bus Switches for Speed, Safety, and Efficiency: What They Are and What You Should Know about Them

by Eva Murphy [eva.murphy@analog.com] and
Catherine Redmond [catherine.redmond@analog.com]

Bus switches—often called *digital switches*—are products designed for connecting to high speed digital buses. Characterized by sub-nanosecond propagation delay and fast switching—and introducing no additional noise or dc power dissipation—they are ideally suited for voltage translation, hot swapping, hot plug, bus or capacitance isolation, and many other applications. In addition, their design makes them useful in many analog applications. The key features that make them suitable for so many different applications include low *on*-resistance, low capacitance, and low propagation delay. This discussion will consider the architecture and characteristics of bus switches—and explain many of their uses.

What is a bus switch?

The basic element of a bus switch is an N-Channel FET whose condition is controlled by CMOS logic. As a *bilateral* switch, either the *source* terminal (A) or the *drain* terminal (B) can be the signal input (Figure 1). When disabled, the gate is held at zero volts and there is an open circuit between the source and the drain.

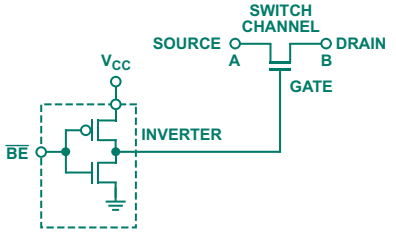


Figure 1. Bus switch channel.

When the switch is enabled ($\overline{BE}$ at 0), its gate is driven to V_{CC}. If V_{GS} (or V_{GD})—i.e., $V_{CC} - V_{IN}$, is greater than the transistor threshold voltage (usually about 1 V) the channel will switch to the low-resistance *on* condition (a few ohms). However, as V_{GS} approaches the threshold voltage, the device approaches its saturation region and becomes highly resistive; Figure 2 shows a typical plot of *on*-resistance versus input voltage as a function of V_{CC} (ADG3257). When in saturation, the output voltage will be limited to $V_{CC} - V_{TH}$.

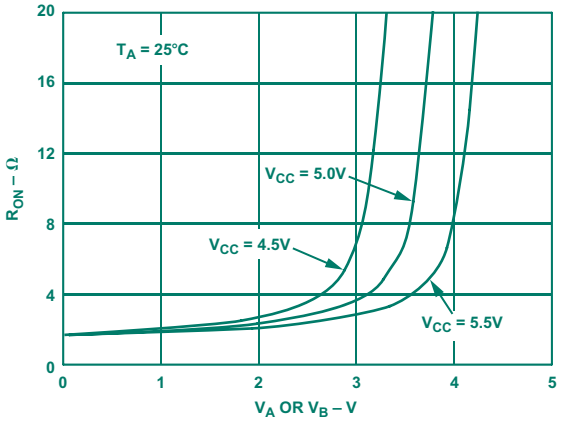


Figure 2. On-resistance of ADG3257 bus switch vs. input voltage (V_A or V_B).

Figure 3 is a plot of output voltage versus input voltage for a typical bus switch with inputs and supply voltages in the 5-V range. When V_{GS} becomes less than about 1 V, the switch channel begins to saturate and the voltage clamps to $V_{CC} - V_{TH}$. So, in this example, for V_{CC} = 5 V, the output follows the input up to about 4 V. Beyond this input voltage, V_{OUT} is held at $V_{CC} - V_{TH}$. This clamping tendency turns out to be a very useful feature of a bus switch; its advantages and use will be discussed in more detail later.

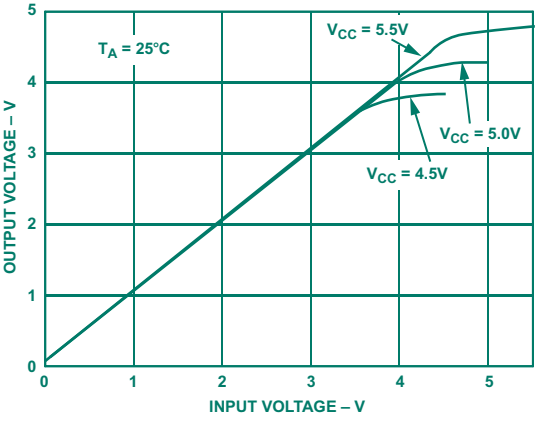


Figure 3. V_{OUT} vs. V_{IN} for the ADG3257 bus switch with V_{CC} in the 5-V range.

Key features affecting applications of bus switch devices are: *on-resistance*, *capacitance* associated with the channel, and *propagation delay. On*-resistance of such devices is usually very low—typically a few ohms. The capacitance, which needs to be kept as low as possible, is typically less than 10 pF in the *on* condition. Both capacitance and *on*-resistance parameters affect the propagation delay through the switch channel.

Practically all of the propagation delay of a bus switch in the *on* condition, driven by a low impedance voltage source, comes from the RC delay of the R_{ON} of the switch and the load capacitance—typically it is in the sub-nanosecond region and is much smaller than the rise/fall times of the driving signals. In a system, propagation delay of the digital switch is determined by the circuit impedance on the driving side of the switch and its interaction with the load on the driven side.

Where would we use a bus switch?

Bus switches are used to increase speed and reduce noise by isolating functions that do not need to drive the bus—or be driven by it—at one moment, but may need to be connected later. Additionally, bus switches can be used in PC *docking stations*, PC-*card* or *power management* applications to break current paths and prevent circuit leakage. By nature, bus switches dissipate very low quiescent power—bus switch members of the ADG324x/ADG325x families, when not switching, typically consume 1 nA (1 μA max)—making them excellent for use in low-power applications such as *notebook* PCs. Bus isolation also makes these devices suitable for *hot swapping* and *hot plugging*, where they can help prevent undesired behavior when additional cards or modules are plugged in. Bus switches are also useful in applications that require systems operating at two different supply voltages to be connected. Each of these applications will be described in more detail below.

Using a digital bus switch for *bus isolation*

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus-bridging devices that allow the number of available loads to be increased without exceeding the specs. Ideally, any load on a bus that is not currently in use should be disconnected to reduce overall capacitive loading and avoid exceeding the bus capacitance specification.

Bus switches are designed specifically for this purpose: to isolate functions that do not need to drive or be driven at this moment but may need to be connected later, thus minimizing the total capacitive load connected at any given moment.

If a bus switch is placed between each load on the bus and the bus itself, then the load is isolated from the bus when the switch is disabled. Because the bus switch can pass significant amounts of current *in either direction* when enabled, without adding significant propagation delay for signals that pass through it, it is a viable solution to the bus isolation problem. Figure 4 shows a generalized situation, and Figure 5 shows a specific solution to a memory bank drive problem with a quad 2:1-multiplexer bus switch.

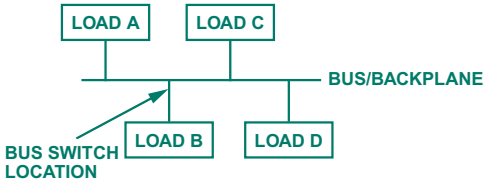


Figure 4. A bus switch can isolate Load B from the rest of the bus.

Multiplexing

Problems faced by a designer of a system with a large number of common bus signals include noise in the system due to simultaneous switching of the address and data bus signals—and large delays in the system caused by capacitive loading of the bus.

Figure 5a shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. Now, if a bus switch is used (the ADG3257 quad 2:1 multiplexer/demultiplexer in this example) as shown in Figure 5b, then the output load on the memory address and data bits is halved. This isolation can provide a near-doubling of the speed at which the selected bank's data can flow, because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also markedly reduced.

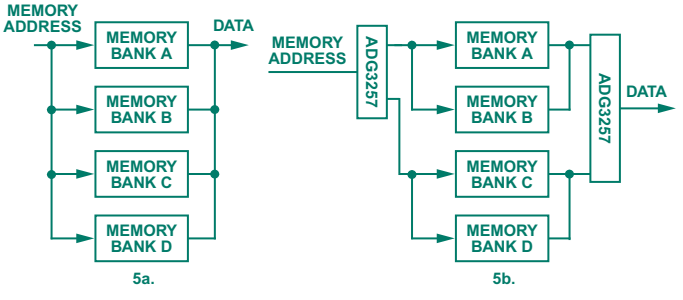


Figure 5. Reducing memory bank loading.

a. The address and data lines are heavily loaded when all memory banks are permanently connected to the bus.
b. When the ADG3257 is used to switch between different memory bank pairs, access time and noise are both reduced.

Voltage-level translation

When interfacing between two devices operating at different supply voltages, digital signals coming from the higher voltage device need to be safely interfaced to the lower voltage device. In order not to exceed *maximum* ratings specified for the device operating at the lower voltage level, the voltage output coming from the higher voltage device must be reduced. This can be readily accomplished by inserting a bus switch in series with the signal in question (Figure 6).

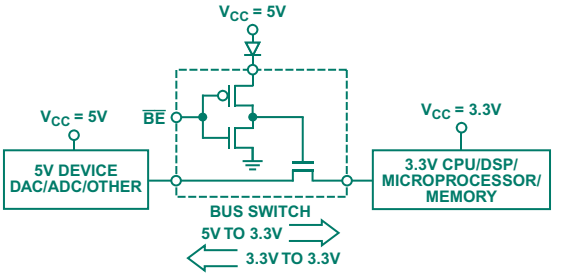


Figure 6. Using the ADG3257 to switch and level translate between a 3.3-V controller and 5-V data converter.

As discussed above, if the V_{GS} voltage is reduced to less than 1 V, the switch channel begins to saturate and the output voltage clamps to $V_{CC} - V_{TH}$. That is, the output follows the input up to the vicinity of this voltage and, for higher input voltages, V_{OUT} is held at $V_{CC} - V_{TH}$. Figure 7 shows an output-input plot of the same switch as in Figure 3, but focused on V_{CC} in the 3.3-V region. This behavior makes bus switch devices suitable for interfacing applications calling for level translation.

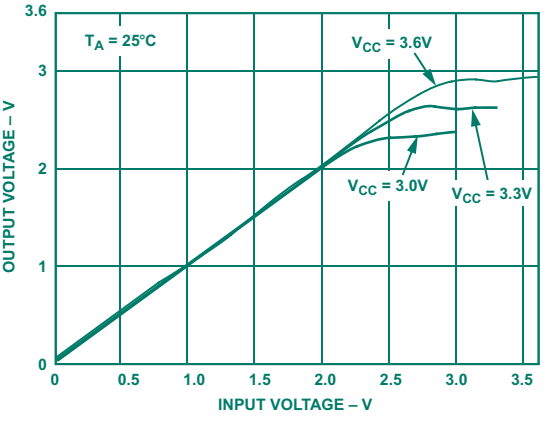


Figure 7. V_{OUT} vs. V_{IN} for the ADG3257 bus switch with V_{CC} in the 3-V range.

In the example of Figure 6, the user may wish to apply a 3.3-V DSP or microcontroller as a control device in an application for which reasonable analog performance requires that the ADC or DAC or other device operate from, say, a 5-V supply. Unless the microcontroller has inputs that can tolerate the 5-V device's output levels, the circuits will not be able to communicate properly. With the bus switch of Figures 3 and 7 connected between the devices, as a voltage translator, bidirectional communication is possible without risk of damaging the lower-supply device. The combination of the diode, connected in series with the 5-V supply, and the bus switch's clamp voltage provides a drop fairly close to the required 5-V-to-3.3-V (left to right) without impeding 3.3-V communication (right to left).

Similarly, the device could be used to level-translate between 3.3-V and 2.5-V systems. A LVTTL VOH level for a 2.5-V output is 2 V, while the LVTTL VIH level required by the 2.5-V device is 1.7 V, so a 5-V bus switch operating at a lower supply voltage can easily meet these requirements.

Because a bus switch is a simple FET, the signal path is bidirectional; i.e., the inputs and outputs are interchangeable. However, *information* cannot always be communicated bidirectionally; it is dependent on supply. Table 1 shows that translations between 5 V↔3.3 V and 3.3 V↔2.5 V may be used to communicate bidirectionally between devices operating from different supplies, but the other two options (2.5V→1.8V, 3.3V→1.8V) cannot be employed for both directions. For further details, see the ADG3247 data sheet.

Table 1. Bus Switch Devices and Their Level-Translation Capabilities.

Part No.	Function	Level Translation			
		5↔3.3	3.3↔2.5	2.5→1.8	3.3→1.8[1]
ADG3245	8-Bit Bus Switch	X	✓	✓	✓
ADG3246	10-Bit Bus Switch	X	✓	✓	✓
ADG3247	16-(2x8) Bit Bus Switch	X	✓	✓	✓
ADG3257	Quad 2-1 (4 Bit, 1 of 2)	✓[2]	✓	X	X

[1]SEL pin tied to logic low. For more information on SEL pin, see ADG3245/6/7 data sheets.

[2]Requires external diode.

As explained earlier, the threshold voltage, V_{TH}, is approximately 1 V, so with 2.5-V supply, the maximum output of the bus switch will be 1.5 V, which is insufficient to meet the 1.7-V V_{IH} input requirement of a 2.5-V device (Figure 8). Similarly, when translating between 3.3 V and 1.8 V, the maximum output of the bus switch will be 1.5 V, so again the voltage level is not sufficiently high for a 3.3-V device to recognize it as *logic high*. Therefore, the signal path can be relied on only for unidirectional communication in these cases.

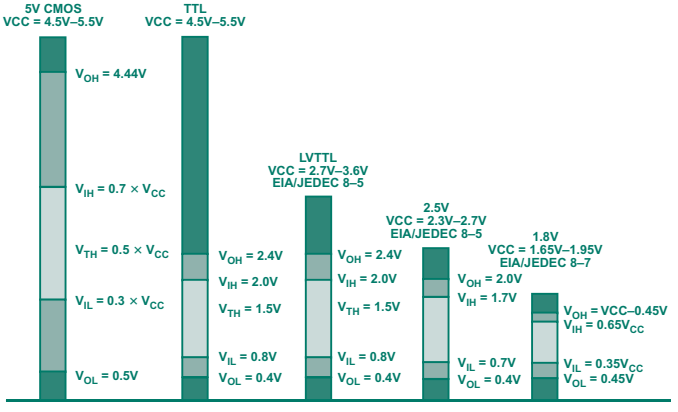


Figure 8. Logic levels compared for different supply voltages.

How many "bits"?

In the terminology of bus switches, *bits* refers to the number of channels associated with the device. For example, a 16-bit device (ADG3247) has 16 individual channels. Bus switches can be made available in a variety of bit widths. Current offerings are 8-, 10-, 16-bit and quad 2-1 (4-bit, 2-port) devices (ADG3245, ADG3246, ADG3247, ADG3257, respectively), with more in the offing.

Can a bus switch be used to switch analog signals?

A bus switch channel is a simple N-channel *field-effect transistor* (FET); standard analog switch designs include a P channel in parallel in order to make rail-to-rail analog switching possible. The design of the bus switch provides lower *on*-resistance, smaller *on* and *off* channel capacitance, and thus improved frequency performance, compared to its analog counterpart. Smaller associated capacitances benefit device performance by reducing charge injection (Figure 9) to significantly lower values than are found in the standard analog switch.

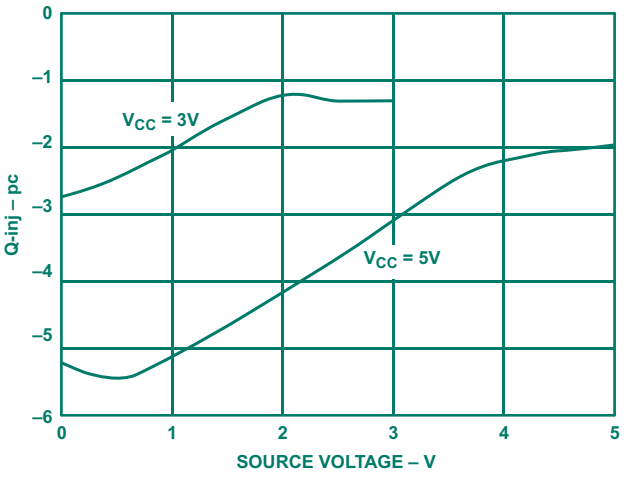


Figure 9. Charge injection for a typical bus switch (ADG3257).

Thus, bus switches need not be confined to bus switching applications or used solely for switching digital signals. They can also find many uses in switching analog signals, within the limitations of $V_{CC} - V_{TH}$ (which, in many cases, is not an important issue).

How are bus switches useful in hot swap applications?

Hot swapping is adding and/or removing plug-in circuitry in a system with the power *on*. Examples of applications that require the ability to hot swap are docking stations for laptops and line cards for telecommunications switches. During a hot swap event, the connectors on the back plane are "live"; the add-on card must be able to cope with this condition. If the bus can be isolated prior to insertion, one has more control over the hot-swap event. Isolation can be achieved using a digital switch, ideally positioned on the add-on card between the connector and the device (Figure 10). However, it is important that the ground pin of the add-on card must connect to the ground pin of the back plane before any other signal or power pins, and it must be the last to disconnect when a card is removed.

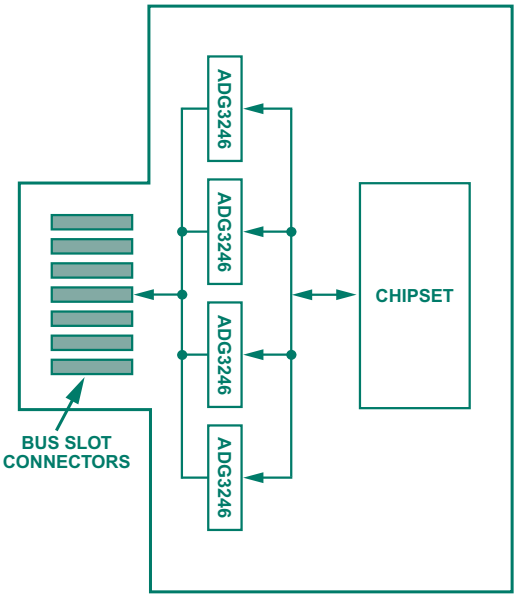


Figure 10. Hot swapping with the ADG3246 bus switch.

And how about hot plug?

Critical systems, such as ADSL (Asynchronous Digital Subscriber Line), manufacturing controls, servers, and airline reservations must not be shut down. If new hardware, such as a plug-in modem, needs to be added to the system, it has to be done while the system is up and running. This process of adding hardware during mandatory continuous operation is known as *hot plug*. To ensure smooth execution of the process, a digital switch can be wired between the connector and the internal bus (Figure 11). During the hot-plug event, the switch is turned off to provide isolation of the specific circuit location.

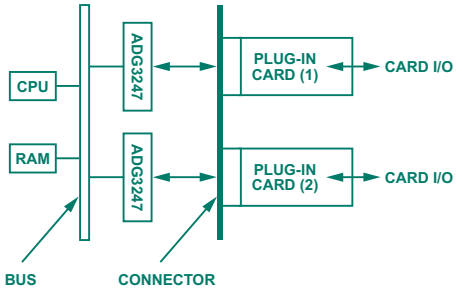


Figure 11. Using the ADG3247 in a hot-plug application.

The benefits of a flow-through pinout architecture

A useful feature of many of these digital switches from Analog Devices is the logical "flow-through" pin arrangement, in which each input and its corresponding output are on opposite sides of the chip without crossovers or interruptions of the pattern (Figure 12). This makes routing of the input and output signals much easier to deal with in printed circuit board layouts. In addition, propagation delays can be more readily matched with a flow-through pin arrangement.

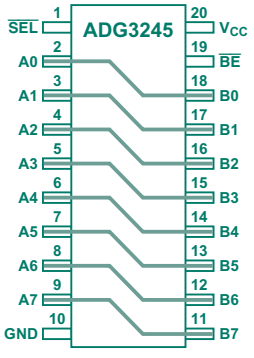


Figure 12. Flow-through pin arrangement.

CONCLUSION

Bus switch devices are extremely versatile; they may be used in many different applications in today's high performance systems. In this brief introduction, we have shown how bus switches are utilized in areas such as bus isolation, voltage translation, analog signal switching, and hot-insertion applications. We have also made it evident that they are suitable for many other applications. We have introduced key specifications of bus switches, discussed their operation, and sought to answer some frequently asked questions about them.

ACKNOWLEDGEMENTS

We wish to thank the Bus Switch Team of Analog Devices for their valuable contributions.

REFERENCES

ADG3245, ADG3246, ADG3247, and ADG3257 data sheets

EIA/JEDEC for power supply voltages and interface standards

Compact PCI Hot Swap Specification R1.0

PCI Hot-Plug Specification R1.0

AUTHORS *(continued from page 2)*

Mark Malaeb (page 15), a Field Applications Engineer at Analog Devices, was graduated from the University of Arizona with a Master's degree in EE. His experience includes industrial automation, embedded controls, and RF design; and he has a broad knowledge of optical networking and telephony. He joined ADI in September 2001.

Eva Murphy (page 18) is an Applications Engineer at ADI's facility in Limerick, Ireland. She provides applications support for general-purpose digital-to-analog converters (DACs), switches/multiplexers, and direct-digital-synthesis (DDS) products. Joining Analog Devices in 2000, Eva holds a BEng from Cork Institute of Technology. Her interests include reading, traveling, and walking.

Catherine Redmond (page 18), a Senior Applications Engineer at ADI's facility in Limerick, Ireland, provides applications support for general-purpose digital-to-analog converters (DACs) and switch/multiplexer products. With a BEng from Cork Institute of Technology, Catherine joined Analog Devices in 1997. Her interests include traveling to warmer climates, outdoor activities, and listening to music.

Trey Roessig (page 3) received the PhD degree in Mechanical Engineering from the University of California, Berkeley, in 1998, majoring in dynamic systems and minoring in circuit design. In 1997, he co-founded Integrated Micro Instruments, Inc., which was acquired by Analog Devices in 2000. He is currently with ADI's Power Management division.

Yuping Toh (page 8), a native of Singapore, received BSEE (1999) and MSEE (2002) degrees from Worcester Polytechnic Institute, where he earned memberships in Tau Beta Pi and Eta Kappa Nu. In June 2001, Yuping joined Analog Devices as an Applications Engineer in the RF group. He is the co-author of a paper recently published in *the IEEE Journal of Solid State Circuits*, "Single-Ended to Differential Converter for Multiple-Stage Single-Ended Ring Oscillators."

BOOKS

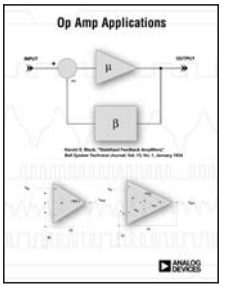
OP AMP APPLICATIONS

Edited by Walter G. Jung

He's done it again! Walt Jung, author of several generations of *IC Op-Amp Cookbook*, going back to 1974, has just completed an all-new op amp book. Together with Walt Kester and ADI's staff of Field Applications Engineers, he has assembled what may well be the ultimate op amp book, ***Op Amp Applications***.[1] This 970-page volume is brimming with application circuits, handy design tips, historical perspectives, and in-depth looks at the latest techniques to simplify designs and improve their performance.

But this is more than just the last word on applications. In a brief but fascinating History section, he outlines the early development of the feedback amplifier, starting with H. S. Black's invention of seventy years ago—and provides priceless insights into the application needs, technological developments, and creative personalities that drove the many generations of op amp designs.

Following the history chapter, the book has seven sections with self-explanatory titles:



- **Op amp basics:** Topologies, structures, specifications, precision op amps, high-speed op amps
- **Specialty amplifiers:** Instrumentation, programmable gain, isolation
- **Using op amps with data converters:** ADC/DAC specifications, driving ADC inputs, driving ADC/DAC reference inputs, buffering DAC outputs
- **Sensor signal conditioning:** Bridge circuits, strain, force, pressure, and flow measurements, high-impedance sensors, temperature sensors
- **Analog filters:** Transfer functions, time-domain responses, standard responses, frequency transformations, filter realizations, practical implementation problems, design examples
- **Signal amplifiers:** Audio, buffers/driving capacitive loads, video, communications, amplifier ideas, composite amplifiers
- **Hardware and housekeeping techniques:** Passive components; PCB design issues; power-supply systems; protection; thermal considerations; EMI/RFI; simulation, breadboarding, and prototyping.

There are three indexes: a comprehensive subject index, an Analog Devices parts index, and a standard-device parts index. The book is in an 8.5 × 11-inch softcover format. Its price is $40.00. For copies, get in touch with Analog Devices Customer Service and request OP-AMP-APPLIC-BOOK. In North America, call toll-free 1-800-262-5643.

Walt Jung, who recently retired from ADI's Central Applications Group, is a well-known long-time electronics and audio experimenter and a prolific writer. A member of the IEEE and a Fellow of the Audio Engineering Society, he was inducted into *Electronic Design's* Hall of Fame in 2002. His books include three editions of the *IC Op-Amp Cookbook*, plus the *IC Timer Cookbook*, and the *IC Converter Cookbook*. A perennial resident of Maryland, he worked for a number of years as a design engineer, and for many years as a consultant and writer before joining ADI's Applications team in 1991.

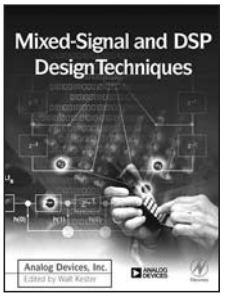
[1]Jung, Walter G., Op Amp Applications, Norwood, MA: Analog Devices, Inc., 2002. ISBN 0-916550-26-5.

[2]Kester, Walt, ed. Mixed-Signal and DSP Design Techniques, Boston, MA: Newnes, an Imprint of Elsevier Science, 2003. ISBN 0-7506-7611-6.

MIXED-SIGNAL AND DSP DESIGN TECHNIQUES

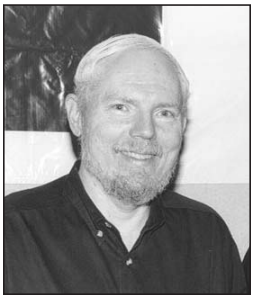
A set of ADI Seminar Notes, edited by Walt Kester, has been available in printed book form from ADI and free on our Website, *www.analog.com* (At left, under Technical Library, choose Technical Library Home; in the Master List, click on Seminar Materials for a list of free links to seminar books). It is now available in a new edition, with updated information—particularly in the digital signal-processing (DSP) area—published by Newnes (*http://www.bh.com/newnes*),[2] as the first volume in a new series.

Packed with design information from engineers with years of experience, and backed up by many references, this volume covers the details of both analog and digital signal-processing (DSP), as well as the requisite analog-digital interfacing. Chapter headings include:



- **Introduction:** About real-world signals and signal processing, with a practical example
- **Sampled data systems:** Discrete time sampling, static transfer functions and dc errors, ac errors in data converters, D/A converter dynamic performance
- **ADCs for DSP applications:** Successive-approximation, sigma-delta, flash, subranging (pipelined), bit-per-stage
- **DACs for DSP applications:** DAC structures, low-distortion architectures, logic, interpolating, sigma-delta, direct digital synthesis (DDS)
- **Fast Fourier transform (FFT):** Discrete Fourier transform (DFT), fast Fourier transform, FFT hardware and benchmarks, DSP requirements for real-time FFT, spectral leakage and windowing
- **Digital filters:** Finite impulse response (FIR), implementations in DSPs, circular buffering, FIR designing, infinite impulse response (IIR), design techniques for IIR, multirate, adaptive
- **DSP hardware:** Microcontrollers, microprocessors, and DSPs; DSP requirements; ADSP-21xx 16-bit fixed-point core; fixed-point vs. floating-point; SHARC DSPs; ADSP-2116x single-instruction, multiple-data (SIMD) core; TigerSHARC, static superscalar; DSP evaluation and CROSSCORE™ tools
- **Interfacing to DSPs:** Parallel interfacing, reading from memory-mapped peripheral ADCs; writing to memory-mapped DACs; serial interfacing; I/O ports, analog front ends, and codecs; high-speed interfacing; DSP system interface
- **DSP applications:** High performance modems for POTS; RAS modems; ADSL; digital cellular; GSM, SoftFone, Othello; analog cellular base stations; digital base stations; motor control, codecs and DSPs in voiceband and audio; sigma-delta ADC with programmable digital filter; applications summary
- **Hardware design techniques:** Low-voltage interfaces, grounding in mixed-signal systems, digital isolation techniques, power-supply noise reduction and filtering, dealing with high-speed logic.

Priced at $59.99, it is available at technical book stores everywhere, including on-line.



Walt Kester is a Corporate Staff Applications Engineer. During more than 30 years at ADI, he has designed, developed, and given applications support for high-speed ADCs, DACs, sample-hold amplifiers, op amps, and multiplexers. Besides writing many papers and articles, he prepared and edited the *Notes* for High-speed, Mixed-signal, Advanced linear design, and other seminars. Walt has a BSEE from North Carolina State and an MSEE from Duke. He enjoys carpentry and travel.

NEW PRODUCT BRIEFS VOLUME 36, PART 2

Volume 36-04

12-bit, 1-Msps differential-input sampling **ADC** with 20-MHz bandwidth **AD7450**
12-bit, 170-/210-Msps sampling **ADC** with LVDS outputs **AD9430**
Dual 12-bit, 105-/125-Msps IF sampling **ADC** **AD10201/26**
Dual low-cost 80-MHz *FastFET*™ **Op Amp** **AD8034**
High-performance, 145-MHz *FastFET* **Op Amp** **AD8065**
High-speed **Op Amp** has ultralow distortion **AD8007**
Octal 16-V, rail-to-rail, unity-gain **Buffer Amplifier** **AD8570**
Dual precision, low-noise, low-bias-current *FastFET* **Op Amp** **AD8620**
AC'97 SoundMAX® **Codec** **AD1981A**
Melody® 32 **Audio Processor** **ADSST-Melody-32**
Dual fractional-N RF- and integer-N IF **Frequency Synthesizer** **ADF4252**
Dual 1024-position nonvolatile **Programmable Resistors** for laser diode drivers **ADN2850**
CDMA **Power Management System**..... **ADP3510**
12-/14-bit serial input, ±10-volt, voltage output **DACs** . **AD5530/AD5531**
Quad 64-position **Digital Potentiometers** with nonvolatile memory **AD5233**
Single/dual 256-position 15-V **Digital Potentiometers** **AD5260/62**
Dual 1024-position **Digital Potentiometers** with nonvolatile memory **AD5235**
Energy Metering ICs **ADE7751/55**
MicroConverter with 12-bit ADC and embedded Flash MCU in TSSOP package **ADuC814**
1-MHz, 750-mA **Buck Regulator** **ADP3088**
5-bit programmable 2-phase **Synchronous Buck Controller** . **ADP3167**
Synchronous Buck Controller with dual linear regulator controllers **ADP3171**
Dual **MOSFET Driver** with bootstrapping **ADP3415**
CDMA **Power Management System** **ADP3510**
0.5-ohm 1.8 V to 5.5 V **SPDT Switch/2:1 Mux** **ADG819/20**
0.4-ohm 1.8 V to 5.5 V **SPST Switches** **ADG801/02**
Quad high-speed 2:1 mux/demux **Bus Switch** **ADG3257**
Complete **Thermal System Management Controller** **ADM1026**
6-channel **DecDriver™ Decimating LCD Panel Driver** **AD8381**
Professional NTSC/PAL **Video Decoder** with 10-bit CCIR656 output **ADV7185**
Video Encoders with six 12-bit DACs for standard definition, progressive scan and HDTV **ADV7300A/01A**
Video Encoders with six 11-bit DACs for standard definition, progressive scan and HDTV **ADV7302A/03A**
14-bit, 30-Msps **CCD Signal Processor** **AD9824**

Volume 36-05

12-/10-/8-bit, 1-Msps low-power **ADCs** in 6-lead SC-70 packages **AD7476A/77A/78A**
12-/14-bit, 3-Msps successive-approximation **ADCs** **AD7482/84**
Dual low-noise, low-distortion, high-speed current-feedback **Op Amp** **AD8008**
Low-cost 80-MHz *FastFET* **Op Amp** **AD8033**
Low-noise, precision JFET-input **Op Amp** **AD8510**
1.8-V, low-power, rail-to-rail **Op Amp** for battery-powered applications **AD8515**
Single/dual/quad low-noise precision rail-to-rail **Op Amps** **AD8605/06/08**
SigmaDSP™ Digital Audio Processor with on-board D/A Converters **AD1954**
Dual 12-/14-/16-bit, 160-Msps, 2×/4×/8× interpolating .. **AD9773/75/77**
TxDAC+® D/A Converters
Low-power **MxFE™** digitizes 10-MHz to 300-MHz IF Signals **AD9874**
Dual 3-GHz fractional-N RF- and 1.1-GHz integer-N IF **Frequency Synthesizers** **ADF4217L/18L/19L**
2.7-V **Serial-Port Transceivers** with 15-kV ESD protection and Green-Idle™ **ADM3310E/15E**
Multirate 155-Mbps to 2.7-Gbps **Clock- and Data-Recovery** IC with limiting amplifier .. **ADN2819**
Average Power Controller for continuous-wave lasers **ADN2830**
Thermoelectric Cooler Controller **ADN8830**
Octal 8-/10-/12-bit low-power voltage-output **DACs** **AD5308/18/28**
DashDSP™ for motor control has analog front-end and FLASH memory **ADMCF340**
32-bit **SHARC® Digital Signal Processor** **ADSP-21161N**
Energy Metering IC with on-chip oscillator measures instantaneous and average power **ADE7757**
2-phase **Core-voltage Controller** for Intel® mobile Pentium® III processors **ADP3203**
Xstream® 34 × 34, 3.2 Gbps **Digital Crosspoint Switch** **AD8152**
Low-leakage, low-charge-injection ±5-V **CMOS Switches** **ADG611/12/13**
32-channel, 4-ohm **Analog Multiplexers** **ADG725/26/31/32**
Low-resistance, low-voltage dual SPST **CMOS Switches** **ADG821/22/23**
dBCOOL™ System Monitor and Fan Controller **ADM1027**
–48-V **Hot Swap Controller** **ADM1070**
600-MHz triple 2:1 **Multiplexers** **AD8186/87**
10-/12-bit, 20-/30-Msps **CCD Signal Processors** with Precision Timing™ generator **AD9891/95**
Programmable **Grayscale Generator** for TFT LCD panels ... **ADD8502**
14-bit 108-MHz precision **Video Encoders** with Noise-Shaped Video (*NSV*™) **ADV7304A/05A**

Volume 36-06

14-bit, 1-Msps successive-approximation **ADC** has serial input **AD7485**
Dual 2-channel 16-bit, 500-ksps successive-approximation **ADC** **AD7654**
4-channel, 8-/10-/12-bit, 1-Msps **ADCs** with sequencer .. **AD7904/14/24**
5-V upstream cable **Line Driver** **AD8328**
Analog I/O port includes 16-bit, 1-Msps ADC and 14-bit, 1-µs DAC **AD15700**
Stereo 24-bit, 96-kHz multibit sigma-delta **ADC** for digital audio **AD1871**
Stereo 24-bit, 192-kHz multibit sigma-delta **DAC** with SACD playback **AD1955**
AC'97 **SoundMAX® Codec** **AD1981B**
16-bit fixed-point DSP-based **Audio Processor** ..... **SST-Melody-DAP**
32-bit floating-point **Audio Processor** ..... **SST-Melody-SHARC**
80-Msps 2-channel W-CDMA **Receive Signal Processor** (RSP).... **AD6634**
Mixed-Signal Front-End (MxFE™) for set-top boxes or cable modems **AD9879**
Mixed-Signal Front-End (MxFE) for broadband modems **AD9975**
Dual 2.4-GHz fractional-N RF- and 1.0-GHz integer-N IF **Frequency Synthesizer** **ADF4212L**
5-V differential PROFIBUS **Line Driver/Receiver** **ADM1486**
Clock- and Data-Recovery IC with limiting amplifier for OC-48/OC-48 FEC **ADN2811**
256-position single-/dual-channel **Digital Potentiometers** **AD5280/82**
TigerSHARC® high-performance 32-bit floating-point **DSP Microcomputer** **ADSP-TS101S**
1.200-V ultralow-power, low-noise **Voltage Reference** rejects power-supply variations **ADR280**
Precision, low-drift, 4.096-V/5.000-V **Voltage References** with *shutdown* **ADR392/95**
Complete 12-bit, 40-Msps **Imaging Signal Processor** **AD9821**
Low-cost dual **Interface for Flat-panel Displays** **AD9882**
Triple 330-MHz, 8-bit **Video DAC** **ADV7125**
Chip scale PAL/NTSC **Video Encoder** with advanced power management **ADV7174/79**
Video-rate Codec can sample up to five channels simultaneously **ADV7202**