Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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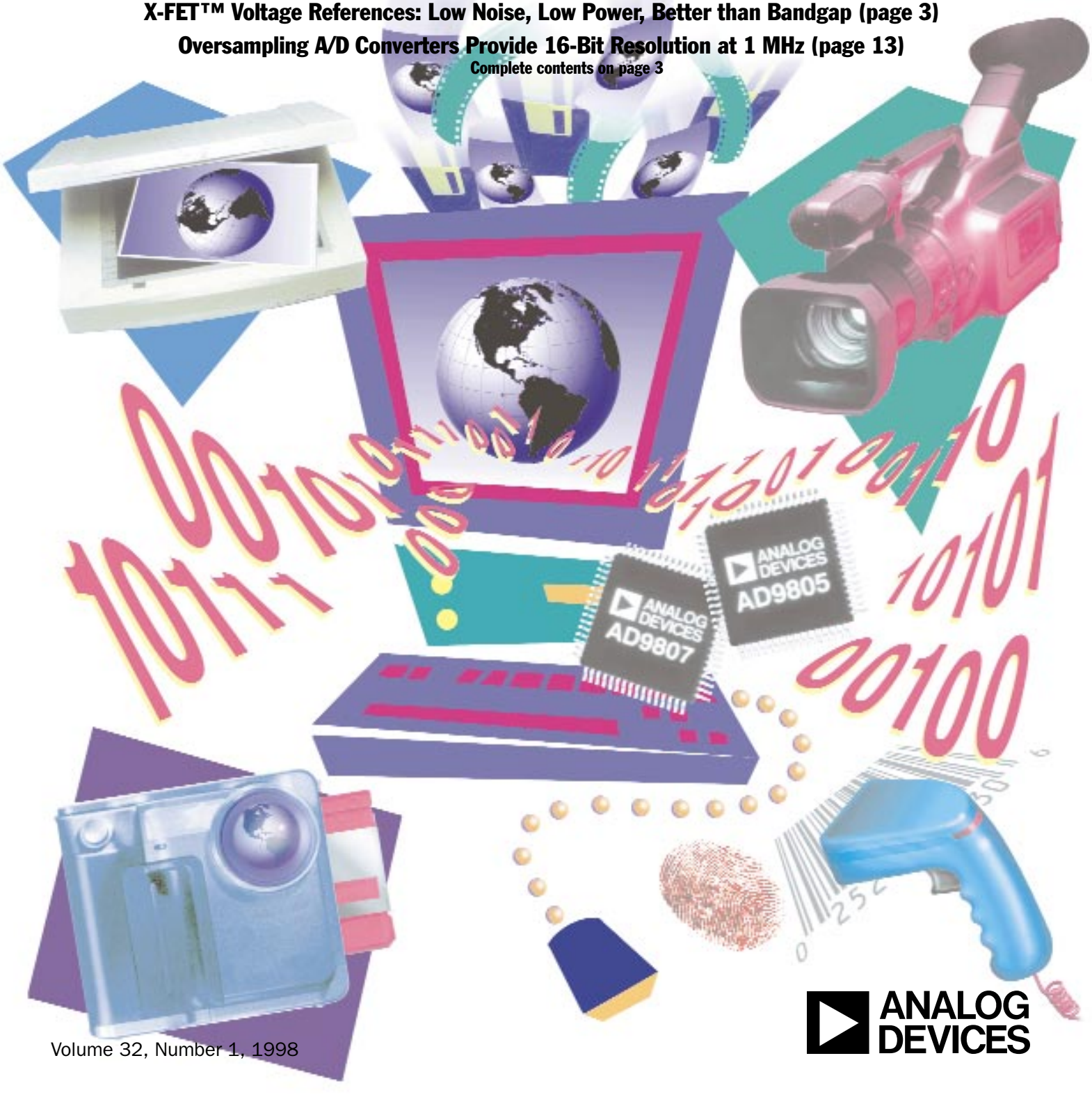

Volume 32, Number 1, 1998

ANALOG DEVICES

Editor's Notes

NEW FELLOWS

We are pleased to note the introduction of 3 new Fellows at our 1998 General Technical Conference: Roy Gosser, Bill Hunt, and Chris Mangelsdorf. *Fellow*, at Analog Devices, represents the highest level of achievement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their creative technical contributions in product or process technology will have led to commercial success with a major impact on the company's net revenues.

Attributes include roles as mentor, consultant, entrepreneur, organizational bridge, teacher, and ambassador. Fellows must also be effective leaders and members of teams and in perceiving customer needs. This trio's technical abilities, accomplishments, and personal qualities well-qualify them to join Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980) Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Doug Mercer (1995), Mohammad Nasser (1993), Wyn Palmer (1991), Carl Roberts (1992), Paul Ruggerio (1994), Brad Scharf (1993), Mike Timko (1982), Mike Tuthill (1988), Jim Wilson (1993), and Scott Wurcer (1996) as Fellows.

ROY GOSSER

Royal A. Gosser is an innovator whose design track record is highlighted by products labeled "First", "Fastest", and "Greatest SFDR". A perennial contributor of new ideas, Roy has designed products that include various A/D converters, op amps, and track and holds. Recent well-known products include the AD9042A/D converter (co-designed with Frank Murden), the AD8011 op amp, and the AD8320 cable line driver. He holds 4 patents.

Equally as important as creative circuit design, a key to IC device performance is the manufacturing process. Roy has supplied ideas and other inputs to assist our process engineers in designing the Analog Devices XFCB (eXtra-Fast Complementary Bipolar) process, one that makes possible the manufacture of some of the world's highest-performance analog ICs in silicon.

Roy joined Analog Devices Computer Labs Division, in Greensboro, NC, in 1982 as an IC design engineer, meeting the challenge to build better interstage amplifiers for A/D converter cards. After a 4-year interlude as Manager of Product Test Engineering, he returned to the design of integrated circuits—and hasn't looked back! Before joining ADI, he had worked in R/D at Litronix (now Siemens), as a design engineer at Hewlett Packard (Palo Alto), and then at Harris Semiconductor. His training included 4 years with Naval Air as an electronic technician, followed by a BSEE from San Jose (CA) University and an MSEE from National Technological University (NTU).

BILL HUNT

Since 1983 Bill has been Design Engineering Manager at ADI's site in Limerick, Ireland. During this time Bill has continually contributed designs and leadership to many core developments, in D/A and A/D converters of all types, including sigma-delta. He has been chief proponent and architect of devices in the servo section of hard-disk drives (HDD). He led the design of baseband audio converters for digital wireless telephony and products for basestations and wired telephony. He also developed a line of DDS products.

He has shown a great ability to understand customer system problems and to develop solutions in terms of new directions for semiconductor technology. He has been active in developing computer-aided design techniques, providing inputs to process-technology developments and measurement techniques.

Bill graduated with a BSEE in 1967 and worked his way through the development engineering ranks of Telectron Ltd, a telecommunications equipment manufacturing company, before joining Analog Devices in 1979 as a Design Engineer. During this period, he gained insight into the emerging infrastructure of the telecom industry and their inherent dependence on early adoption of semiconductor technology as a competitive advantage.

CHRIS MANGELSDORF

Dr. Christopher W. Mangelsdorf designed the AD770 8-bit, 200-MSPS A/D converter, and went on to lead a team that designed the industry's first CMOS 10-bit, 15-MSPS ADC and the first high-resolution integrated CCD signal processing chip for digital cameras. These have served as core designs for many other CMOS high-performance products. For the last 2 years, Chris has managed the product design center that serves our customers in Japan.

Chris represents ADI on the Bipolar Circuits and ISSCC conference committees; he has chaired panels and presented papers at these and other conferences. He has published >10 technical papers and has 13 patents (5 shared). He serves as a link to college campuses and as a mentor to young team members.

He received a BS in Physics from Davidson College (NC) in 1977, and went on to earn a Master's degree, then a Ph.D., in Electrical Engineering at MIT, where he held the Analog Devices Fellowship. He has been associated with Analog Devices since summer employment in 1980. He enjoys board sports, i.e., windsurfing, surfing, and snowboarding.

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Analog Dialogue

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XFET™ References

Low noise, lower voltage than Zeners, Micropower, better than bandgaps

by Roya Nasraty

In order for an analog signal to represent (or be represented by) a digital number, a reference, usually voltage, is necessary to translate the scale. Thus, an A/D converter produces a digital number proportional to the ratio of an analog signal to a reference voltage; and a D/A converter produces an output that is a fraction of the full-scale voltage or current, established by a reference. If the reference signal develops an error of +1%, it will cause a proportional system error: the analog output of a DAC will increase by 1%, and the digital output of an ADC will decrease by 1%.

In systems where absolute measurements are required, system accuracy is highly dependent on the accuracy of the reference. In high-resolution data-acquisition systems, especially those that must operate over a wide temperature range, high-stability references are a must. The accuracy of any converter is limited by the temperature sensitivity and long term drift of its voltage reference. If the voltage reference is allowed to contribute an error equivalent to only 1/2 of a least-significant bit (1 LSB = 2^{-n} of full scale), it may be surprising to see just how good the reference must be, even for small temperature excursions. And when temperature changes are large, the reference design is a major problem.

For instance, an autocalibrated true 16-bit A/D converter has an LSB of 15.2 parts per million (ppm) of full scale. For the ADC to have an absolute accuracy of 16 bits, the voltage-reference error over the entire operating temperature range must be less than or equal to 1/2 LSB, or 7.6 ppm. If the reference drift is 1 ppm/°C, then (neglecting all other error sources) the total temperature swing must not exceed 7.6°C to maintain true 16-bit accuracy. Anther sources of error, often overlooked, is reference *noise*; keeping it low (typically less than 1/4 LSB) is critical for high accuracy. Nonlinearity of the reference's temperature coefficient and large thermal hysteresis are other sources of error that can significantly affect overall system accuracy.

TYPES OF REFERENCES

Zener* diodes: Widely used for many years is the temperature-compensated Zener diode, produced by the reverse breakdown of the base-emitter junction at the surface of the device. Zeners have constant voltage drop, especially when used in a circuit that can provide a constant current derived from a higher supply voltage. Zeners are available in a wide range of voltage options: from about 6 V to 200 V, tolerances of 1.0% to 20%, and power dissipation from a fraction of a watt to 40 or 50 W. However they have many shortcomings. They often require additional circuitry to obtain low output impedance, the voltage tolerance of low-cost devices is generally poor; they are noisy and very sensitive to changes in current and temperature, and they are susceptible to change with time.

The *buried*, or *subsurface* Zener is the preferred reference source for accurate IC devices. In a subsurface Zener reference, the reverse breakdown area is covered by a protective diffusion to keep it well below the impurities, mechanical stresses and crystal imperfections found at the surface. Since these effects contribute to noise and long term instability, the buried breakdown diode is less noisy and more stable than surface Zeners. However, it requires a power supply of at least 6 V and must draw several hundred microamperes to keep the noise to a practical level.

*Note: Reference diodes can use two types of breakdown phenomena, Zener and avalanche. Most reference diodes employ the higher-voltage avalanche mode, but all have come to be called "Zener" diodes.

Bandgaps: Another popular design technique for voltage references uses the bandgap principle: the V_{be} of any silicon transistor has a negative tempco of about 2 mV/°C, which can be extrapolated to approximately 1.2 V at absolute zero (the bandgap voltage of silicon). The difference in base-emitter voltage between matched transistors operating at differing current densities will be proportional to absolute temperature (PTAT). This voltage, added to a V_{be} with its negative temperature coefficient, will achieve the constant bandgap voltage. This temperature-invariant voltage can be used as a "low-voltage Zener diode" in a shunt connection (AD1580). More often, it is amplified and buffered to produce a standard voltage value, such as 2.5 or 5 V. The bandgap voltage reference has attained a high degree of refinement since its introduction and is widely used; yet it lacks the precision demanded by many of today's electronic systems. Practical bandgap references are not noted for good noise performance, exhibit considerable temperature hysteresis, and have long-term stability dependent on the absolute value of at least one on-chip resistor.

A new principle—the XFET™: With the proliferation of systems using 5-V supplies and the growing need for operation at and below 3 volts, designers of ICs and systems need high-performance voltage references that can operate from supply rails well below the >6 V needed for buried-Zener diodes. Such a device must combine low-power operation with low noise and low drift. Also desirable are linear temperature coefficient, good long-term stability and low thermal hysteresis. To meet these needs, a new reference architecture has been created to provide this much-desired voltage reference. The technique, dubbed XFET™ (eXtra implanted FET), yields a low-noise reference that requires low supply current and provides improved temperature coefficient linearity with low thermal hysteresis.

The core of the XFET reference consists of two junction field-effect transistors, one of which has an extra channel implant to raise its pinch-off voltage. With both JFETs running at the same drain current, the difference in pinch-off voltage is amplified and used to form a highly stable voltage reference. The intrinsic reference voltage is about 500 mV, with a negative temperature coefficient of about 120 ppm/K. This slope is essentially locked in

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to the dielectric constant of silicon and is closely compensated for by adding a correction term generated in the same manner as the proportional-to-absolute temperature (PTAT) term used to compensate bandgap references. However, the intrinsic temperature coefficient of the XFET is some thirty times lower than that of a bandgap. As a result, much less correction is needed. This tends to result in much less noise, since most of the noise of a bandgap reference comes from the temperature-compensation circuitry. The temperature correction term is provided by a current, I_{PTAT}, which is positive and proportional to absolute temperature (Figure 1).

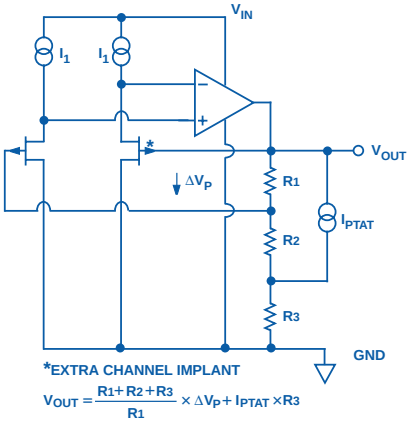

Figure 1. Simplified schematic diagram of ADR29x reference.

The ADR29x series* are the first of a growing family of references based on the XFET architecture. They operate from supply rails from 2.7 to 15 V and draw just 12 µA. Output voltage options include 2.048 V (ADR290), 2.5 V (ADR291), 4.096 V (ADR292), and 5 V (ADR293).

Fruits of the new technology: The XFET circuit topology has significant advantages over most bandgap and Zener references. When operating at the same current, peak-to-peak noise voltage from a XFET reference at frequencies between 0.1 and 10 Hz is typically 3 times less than that for a bandgap (see comparison between the REF192 and ADR291). Alternatively, a bandgap reference needs to run at typically 20 times the supply current of an XFET reference in order to provide equivalent peak-to-peak noise performance (ADR291 vs. AD680). The XFET reference has a very flat or linear temperature coefficient over the extended industrial operating temperature range. The best bandgap and Zener voltage references typically have non-linear temperature coefficients at the temperature extremes. These nonlinearities are not consistent from part to part, so a simple ROM/software look-up table cannot be used for temperature coefficient correction. Temperature coefficient linearity is a very important specification for DVM applications. Another major advantage of the XFET is its excellent long term stability. Its drift is less than one-fifth that of a bandgap reference and comparable to that of Zener references (see Table).

Despite the low quiescent current, the ADR29x family are capable of delivering 5 mA to the load from a low-dropout PNP output stage; and there is no requirement for an output decoupling capacitor. Thermal hysteresis with the XFET design is much better than with bandgaps. Production devices exhibit approximately 200 µV of recoverable and non-cumulative shift when subjected to a 100-kelvin thermal shock vs. a 500 to 1000-µV shift in comparable bandgaps. The overall performance advantage offered by ADI's proprietary XFET architecture in portable systems requiring precision, stability, and low power is unmatched by existing bandgap or Zener references.

Application—current source: The ADR29x Series are useful for many low-power, low-voltage precision reference applications, including negative references and "beefed-up" precision regulators using external low-quiescent rail-to-rail amplifiers with Kelvin feedback connections. The low and insensitive quiescent current (about 12 ± 2 µA over temperature) permits the ADR29x family members to serve as precision current sources, operating from low supply voltage.

Figure 2 shows a basic connection for a floating current source with a grounded load. The precision regulated output voltage causes a current of (V_{OUT}/R_{SET}), to flow through R_{SET}, which is the sum of a fixed and an adjustable external resistance. This current, ≤5 mA, adds to the quiescent current to form the load current through R_L. Thus, predictable currents from 12 µA to 5 mA can be programmed to flow through the load.

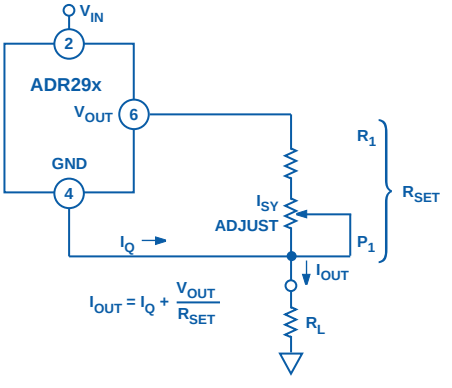

Figure 2. Precision current source.

*For data, consult our Web site, **www.analog.com** (Product Center), AnalogFax line **800-446-6212** (with **Faxcode 2110**), or use the reply card. **Circle 1**

Table 1. Comparison of Zener, Bandgap, and XFET References

Parameter	**ADR291**	**AD586**	**AD680**	**REF192**
Reference Topology	XFET	Buried Zener	Bandgap	Bandgap
Supply Voltage (V)	+3.0	+15.0	+5.0	+3.3
Voltage Output (V)	2.5	5	2.5	2.5
Initial Accuracy (mV)* max	±2	±2	±5	±2
Temperature Coefficient (ppm/°C)* max	8 (–25 to +85)	2 (0 to +70)	20 (–40 to +85)	5 (–40 to +85)
Noise Voltage 0.1–10 Hz (µV p-p)	8	4	10	25
Quiescent Current (µA) max, 25°C	12	3000	250	45
Line Regulation (ppm/V)*, max	100	100	40	4
Load Regulation (ppm/mA)* max	100	100	100	10
Operating Temperature Range (°C)	–40 to +125	–40 to +85	–40 to +85	–40 to +85

*Top Grade

1.5-W Loudspeaker Amplifier Delivers Sound Performance

by Troy Murphy

The SSM2211* speaker amplifier, from the Analog Devices audio amplifier group, is an operational power amplifier designed to deliver up to 1.5 W of power into a 4-Ω speaker when powered by a +5-V single supply. Its current drive, sound quality, and heat dissipation are substantially improved over earlier integrated speaker amplifiers. Its SO-8 package uses a patented Thermal Coastline® technique for significantly improved heat dissipation in a small space. This allows the device to deliver power at elevated ambient temperatures.

The pushpull-output SSM2211 consists of an input amplifier (Figure 1), that can be configured for gain like a standard op amp, and a unity-gain inverting amplifier—with appropriate biasing—producing a differential output voltage across a floating "bridge-tied" load (BTL) with maximum swing approaching twice the supply voltage (hence four times the single-ended power output into a resistive load). Both amplifiers have high-current output stages (to within 400 mV of the rails at full power). A reference voltage is available to bias the two amplifiers for single-supply use, and the device can be put into a low-current shutdown mode, drawing typically less than 10 nA; this makes it very suitable for battery-powered applications, such as portable PC audio and mobile radios.

At maximum output power, the total harmonic distortion (THD) is only 0.1%, a significant improvement over IC speaker amplifiers currently on the market.

Design objectives There are two major challenges in designing a power amplifier to be housed in a small-outline (SOIC) package. One is to deliver the maximum power efficiently from a single supply voltage. The other is to dissipate the heat the device generates at high output power levels without excessive temperature rise.

To drive a load connected from the single-ended output of an amplifier to ground, the maximum sine-wave power available is simply $V_P^2/(2R)$, where V_P is the peak voltage. In the ideal case (rail-to-rail), V_P would be half the supply voltage, and max output would be $V_s^2/(8R)$. With the amplifier biased halfway in a single-supply application, a capacitor must be used to couple a speaker to a single-ended output to block direct current from the speaker. Because the typical resistance of a speaker can be 8 Ω or less, the capacitance must be at least several hundred microfarads to minimize attenuation at low frequencies. The capacitor adds cost to the system design and takes up precious board space. The efficiency of this arrangement is low.

By connecting a speaker across both outputs in a pushpull, or bridge-tied load (BTL) configuration, the need for a coupling capacitor is eliminated, because both output terminals are biased to the same dc voltage. The BTL configuration also doubles the voltage swing across the output. Because the output power is proportional to the square of the voltage, this allows four times as much power to be delivered to the speaker, a loudness increase of 12 dB. In addition, efficiency can be greater.

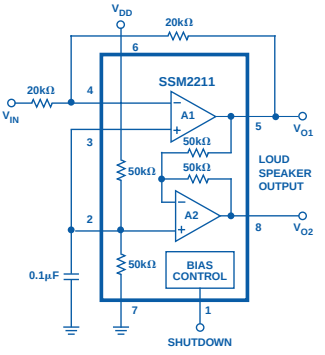

Figure 1. SSM2211 Simplified Schematic.

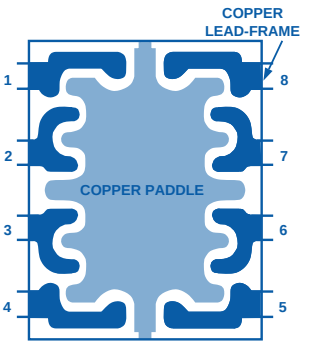

Figure 2. Thermal Coastline.

The maximum power dissipation of the SSM2211 is a function of the supply voltage and the resistance of the speaker it is driving. It can be found by the formula:

$$P_{DISS,\max} = \frac{2V_{DD}^{\ 2}}{\pi^2 R_L}$$

where V_{DD} is the supply voltage and R_L is the speaker resistance.

With a +5-V supply and an 8-Ω speaker, the maximum power dissipation of the device is 633 mW. This can result in a significant heat increase in a standard SO-8 package. To improve the heat dissipation from the package, the SSM2211 uses a modified package for lowered thermal resistance. This proprietary package, developed by Analog Devices, uses an internal modification called a Thermal Coastline® to improve the thermal resistance in a SOIC package by more than 30%.

The modification, done inside the package, is invisible to the user. In a standard package, the die sits on a rectangular paddle with the bonding pads coming out to the die. In a package with a Thermal Coastline, the area of the paddle is increased; the bonding pads are extended and curve around the paddle, as shown in Figure 2. This provides a path with increased thermal conductivity for heat to flow from the die into the package case, thereby lowering the thermal resistance from the die to the ambient surroundings.

For a standard SOIC package, typical junction-to-ambient-temperature thermal resistance (θ_{JA}) is 158°C/W. In a Thermal Coastline SOIC package, θ_{JA} is 98°C/W. Thus, a die in a Thermal Coastline package will not get as hot as a die in a standard package with the same power dissipation.

As a result of this packaging, the SSM2211 can deliver 1 W into an 8-Ω load at temperatures up to +85°C. This is a significant improvement over IC power amplifiers in conventional small-outline packages, which can only deliver this magnitude of output power at temperatures less than +44°C.

Analog Devices Thermal Coastline technology is not limited to small outline packages; it can be applied to practically any package type. Besides high-power audio, these new thermally efficient packages have useful applications in power management and temperature sensing devices. You can expect to see more small packages of this sort with greater power output on increasing numbers of new products from Analog Devices.

*For data, consult our Web site, **www.analog.com** (Product Center), AnalogFax line **800-446-6212** (with **Faxcode 1979**), or use the reply card. **Circle 2**

Integrated Solutions for CCD Signal Processing

by Erik Barnes

The *charge-coupled device* (CCD) is the image sensor of choice for most consumer imaging systems. The CCD's output signal requires a unique, largely analog, signal-processing chain. At first, processing was implemented with standard linear components: op-amps, A/D and D/A converters, analog multipliers, and analog switches. As time passed, advances in semiconductor design and technology have made it possible to combine these in a more fully integrated approach to CCD signal processing. Today, all of the signal processing steps required—from the output of the CCD through the digital output of the A/D converter—can be accomplished with a single integrated circuit. Integrated solutions for CCD imaging applications from Analog Devices retain the performance of traditional designs but provide substantial savings in cost, power, and size.

Processing the CCD Signal

To understand what the integrated signal processing components have to offer, consider the typical CCD output waveform shown in Figure 1. The output stage of the CCD converts the charge of each pixel (picture element) to a voltage via the sense capacitor, C_S. At the start of each pixel period, the voltage on C_S is reset to the reference level, causing a *reset feedthrough* glitch to occur. The amount of light sensed by each pixel is measured by the difference between the reference and data voltage levels. Accurately recovering and digitizing the CCD signal requires several operations, including *correlated double sampling* and *dc restoration* (clamping), gain, offset, and A/D conversion. Correlated double sampling (CDS) serves two important purposes: it calculates the difference between the reference and data levels of the CCD signal, and it reduces some of the noise components in the CCD signal. Conceptually, the CDS is a differential-in-time amplifier: it takes separate samples of the input signal and outputs the difference between them. Figure 2 shows a simple implementation of CDS using two sample-and-hold Amplifiers (SHAs) and a difference amplifier, one of many possible topologies.

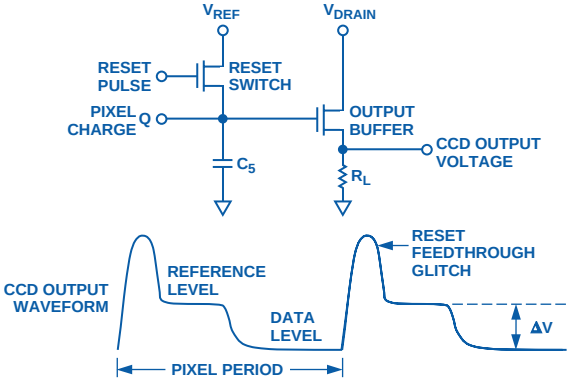

Figure 1. CCD output stage.

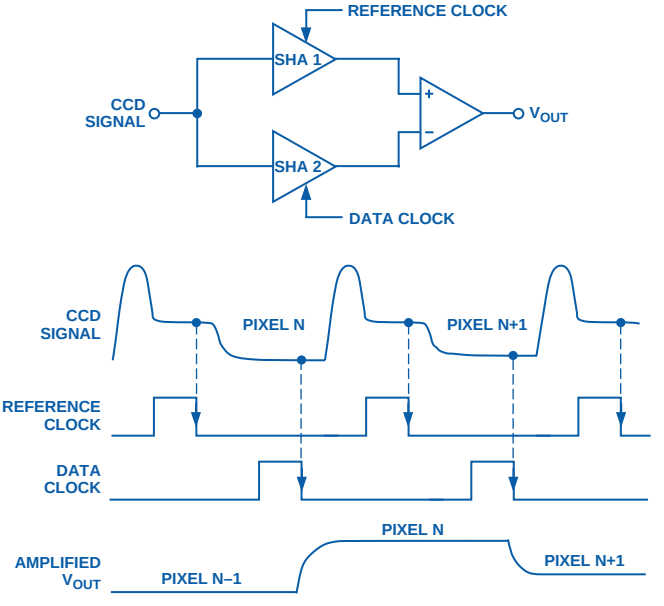

Figure 2. Correlated double sampling. SHA1 samples the reference level, SHA2 the data level. The difference amplifier subtracts the samples, for a measure of the light intensity, reducing common-mode noise.

By taking two samples of the CCD signal and subtracting them, any noise source that is correlated to the two samples will be removed. A slowly varying noise source that is not correlated will be reduced in magnitude. Noise introduced in the output stage of

Part Number	**AD9807**	**AD9816**	**AD9805**	**AD9803†**	**AD9802**	**AD9801**
Number of Channels	3	3	3	1	1	1
Resolution, bits	12	12	10	10	10	10
Sampling Rate, MHz	6	6	6	21	18	18
Diff. nonlinearity, LSBs	0.75 max	1.0 max	0.5 max	0.5 typ	0.5 typ	0.5 typ
No Missing Codes	Guaranteed	Guaranteed	Guaranteed	Guaranteed	Guaranteed	Guaranteed
Output Noise, rms (LSBs)	0.3	0.5	0.1	0.85	0.85	0.85
Internal voltage reference	Yes	Yes	Yes	Yes	Yes	Yes
Supply Voltage, V	+5	+5	+5	+3	+3	+3
Price, USD (1000s)	$25	$9.50	$9.50	†	$5.95	$8.50
Faxcode, *Circle	**2021, 3**	**2475, 67**	**2021, 3**	†	**2195, 4**	**2118, 5**

*For data, consult our Web site, **www.analog.com** (Product Center), AnalogFax line **800-446-6212** (with **Faxcode**), or circle a 1-digit number on the reply card.
†Unreleased product, samples available.

the CCD shown in Figure 1 consists primarily of kT/C noise from the charge-sensing node, and $1/f$ and white noise from the output amplifier. The kT/C noise from the reset switch's ON-resistance is sampled on the Sense node, where it remains until the next pixel. It will be present during both the reference and data levels, so it is correlated within one pixel period and will be removed by the CDS. The CDS will also attenuate the $1/f$ noise from the output amplifier, because the frequency response of the CDS falls off with decreasing frequency. Low frequency noise introduced prior to the CDS from power supplies and by temperature drifts will also be attenuated by the CDS. But wideband noise introduced by the CCD will not be reduced by the CDS.

A typical CCD signal has a dc offset of anywhere from 3 to 9 volts or more. DC offsets of this magnitude are generally not compatible with CMOS signal processing ICs, because most scanner and high end camera systems use 5-V supplies for the signal processors, while camcorders and digital cameras use supplies as low as 2.7 volts. On-chip ac-coupling using an input "dc-restoring" clamp accomplishes the necessary dc level shift, with the addition of an external coupling capacitor.

The CCD's dark current causes a difference between the reference and data levels of the CCD signal, typically ranging from 10 to 80 mV. If left uncorrected, this offset will reduce system dynamic range, particularly after gain is applied. Analog signal processing corrects the average level of the offset, retaining dynamic range. With the major part of the offset thus removed in the analog domain, the digital image processing circuitry can perform fine offset adjustment on a pixel-to-pixel basis to correct for dark-current variations.

A programmable-gain amplifier (PGA) is needed to match the CCD signal's maximum amplitude with the full-scale voltage of the A/D converter. Different CCDs for scanner and digital camera applications can have peak spans ranging from 100 mV up to 3 or 4 volts. Most CMOS A/D converters have full-scale voltage spans of 1 to 5 volts. If the CCD signal only spans 25% of the ADC's full-scale range, 2 bits of dynamic range will be lost. The PGA will amplify the CCD signal to the appropriate amplitude, allowing the ADC's full dynamic range to be used.

The A/D converter converts the conditioned analog signal into a digital representation, which is then processed by external application-specific digital circuitry. The speed and resolution required by the A/D converter are based on the pixel rate and resolution of the application. A CCD with a maximum dynamic range of 55–60 dB would require a 10-bit ADC, while one with a dynamic range of 65–70 dB would require a 12-bit ADC. Additional resolution may be needed to allow headroom for the digital image processing. For example, digital upscaling by 6 dB reduces the dynamic range of the ADC by one bit, because only half of the A/D converter's input voltage range can be used.

Integrated Solutions from ADI

Analog Devices offers several *analog front-end* (AFE) integrated circuits for the scanner, digital still camera, and camcorder markets; they comprise all of the signal processing steps described above. Advances in process technology and circuit topologies have made this level of integration possible in foundry CMOS without sacrificing performance. Not long ago more-costly and power-hungry BiCMOS or bipolar technology would have been required. By combining successful ADC architectures with high-performance CMOS analog circuitry, it is possible to design complete low-cost CCD signal-processing ICs.

For *scanner* applications, the AD9807 and AD9805 (see Table) were introduced in late 1996. These devices feature three input channels for processing color linear CCDs, with input clamping, CDS, offset control, PGA, and a 12- or 10-bit ADC. Additional operating modes allow direct connection with *contact image sensors* (CIS), another type of image sensor that is gaining popularity. The latest product in this series is the AD9816 (Figure 3). This second-generation product functions like the AD9807, but it is housed in a smaller package and costs less.

For *digital still camera* (DSC) designs, the AD9801 was introduced in early 1997. Though it includes the same basic functions as the AD9807 family, it is tailored for use with area CCD arrays. A single-channel, 18-MHz architecture is used, with a 30-dB programmable gain amplifier, black level clamp loop, and 10-bit ADC. The input range is smaller, to accommodate the lower output voltages of area CCDs, and the programmable gain range is wider

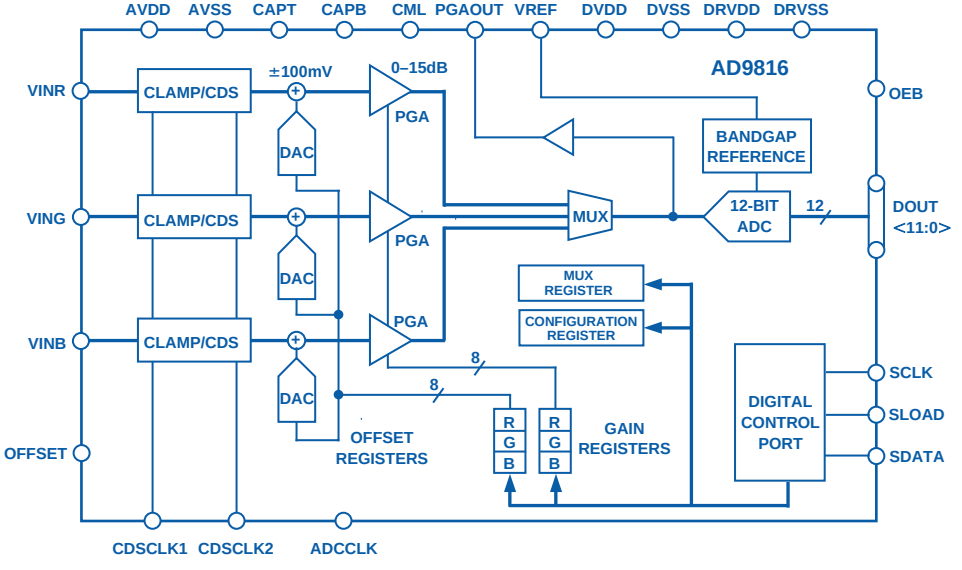

Figure 3. The AD9816 features 3-channel simultaneous sampling, individual per-channel gain and offset adjustment, internal voltage reference, and a 6-MHz, 12-bit A/D converter. The on-board registers are programmed using a 3-wire serial interface.

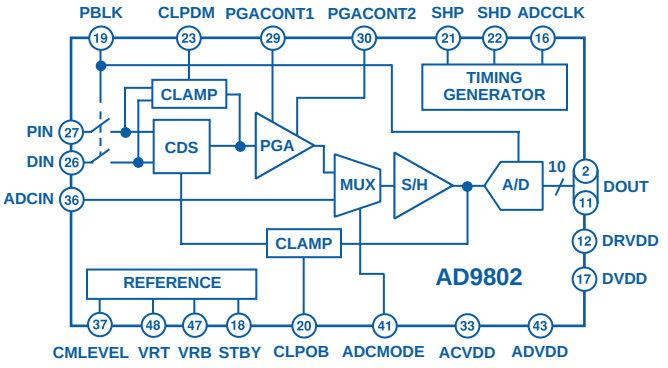

Figure 4. Functional block diagram of the AD9802 CCD signal processor.

in order to be compatible with the broad range of lighting conditions in which a camera is used (scanners operate under more uniform lighting conditions). Battery operation demands lower power, so the AD9801 operates from a single 3-volt supply.

The AD9802, introduced in the fall of 1997, is intended to be used for both DSC and camcorder designs. Shown in Figure 4, the AD9802 has the features of the AD9801, and also includes a multiplexed direct input to the 10-bit ADC. A direct ADC input is required in camcorder applications, to digitize analog video signals from a tape or external VCR. The AD9803, now being sampled (at this writing), adds a serial digital interface for programming the internal registers—and features a higher sampling rate.

Performance Considerations

Two important characteristics of especial interest in imaging applications are noise and nonlinearity.

Noise in the AFE consists of wideband noise from all of the analog circuitry, wideband noise from the ADC, and quantization noise from the ADC. Stand-alone A/D converters usually specify a signal-to-noise ratio (SNR) or signal-to-noise-and-distortion (SINAD), but these types of measurements are not entirely useful in imaging applications. Converter SINAD is tested with a sine-wave input, and includes the effects of distortion of the analog signal, converter distortion due to integral and differential nonlinearity (INL and DNL), quantization noise, and thermal noise. In some cases, to reduce the contribution of thermal noise, multiple data records are averaged.

The distortion numbers are not of interest in imaging applications because CCD signals are not sinusoidal in nature, and the front-end of the ADC samples the CCD signal only during a relatively slow-moving portion of the waveform. Instead of using a traditional converter SNR measurement, CCD system designers consider the contributions from wideband noise, quantization noise, and DNL errors. Wideband noise can be measured using a "grounded-input histogram" test, in which the inputs to the device are grounded, and a histogram is taken of the output data. The standard deviation of the histogram will give the rms noise level of the device (not including the ADC quantization noise). A low-noise AFE can have a thermal noise level comparable to or less than the rms quantization noise of its on-board ADC.

AFE noise is important because of its impact on the system's dynamic range. Dynamic range is determined by comparing the maximum signal that can be processed to the minimum signal level that can be resolved in the system. Noise from the CCD and from the AFE (which includes the analog signal processing and A/D converter) will contribute to overall system noise level. The CCD random noise is usually specified by the CCD manufacturer as "noise floor" or "random noise" in mV or electrons rms; the kT/C and 1/f noise contributions will be reduced by the CDS. Fixed pattern noise due to variations in the dark current of each pixel can be very objectionable in images and should be included in the noise calculation if it is not reduced through calibration techniques. Noise will also be introduced by the amplifier used to buffer the CCD's output signal, though this can be minimized by amplifier choice and circuit techniques. The noise contribution from the AFE can be found on the product's data sheet, or measured using the grounded input histogram test. The ADC's resolution will determine the quantization noise level, which is calculated by dividing the weight of one LSB by $\sqrt{12}$. Adding all the noise sources in a given bandwidth (referred to the same point in the signal chain) by root-sum-of-squares gives:

$$n_{TOTAL} = \sqrt{n_{CCD}^{\ 2} + n_{FPN}^{\ 2} + n_{AFE}^{\ 2} + n_{ADC}^{\ 2}}$$

This equation can be used in approximating the achievable dynamic range, to see if the AFE being considered is a good match for the CCD. If the largest noise source is three times the next largest, it will be dominant. Understanding which noise sources are dominant will help in the selection of an appropriate AFE.

The AFE's linearity will also affect system performance. The nonlinearities of a real ADC can cause artifacts in the digitized image. Differential nonlinearity (DNL) is very important, because the human visual system is good at detecting edges or discontinuities in an image. DNL is the variation in code width for the ADC, with poor DNL causing uneven gradations or "steps" in adjacent luminosity levels. A true 10-bit system demands DNL of better than 1 LSB at the 10-bit level (0.5 LSB is preferable) to avoid degradation of image quality. DNL that is poor enough to cause missing codes can cause image artifacts in the digital processing. Integral nonlinearity (INL) is also important, but a given amount is less perceptible than a comparable amount of DNL. The human visual system is less adept at distinguishing gradual nonlinearity which is spread out over the entire grey-scale range. However, large INL can contribute to errors in the color processing algorithms of a particular system, resulting in color-related artifacts in the image.

Although the integrated approach does not have the advantage of allowing each separate processing stage to be evaluated, the AFE can be thoroughly evaluated under the operating conditions of a specific application. Evaluation boards, conveniently available for the AD980x family, simplify this step of the design.

Integration road map: Increased scope of on-chip integration for decreased size and cost is becoming a way of life in systems-on-a chip development. Now that good analog performance is possible with standard CMOS processes, it should become feasible to integrate some or all of the back-end digital processing of the imaging system onto a single chip to meet the needs of a specific application. Indeed, Analog Devices is currently producing an ASIC to meet the needs of a major scanner manufacturer for a chip that successfully integrates the AFE, digital image processing, SRAM, timing generation, CPU, and SCSI/EPP interfaces on a single chip. At this level of complexity, power and ground management on the chip is critical to minimize coupling of digital noise into the analog circuitry. Because of the large driver currents required, the solution to the problem of including the SCSI interface on-chip has been an especially challenging exercise.

DSP 101 Part 4:

Programming Considerations for Real-time I/O

by Noam Levine and David Skolnick

So far, this series has introduced the following topics:

- Part 1 (vol. 31-1): DSP architecture and DSP advantages over traditionally analog circuitry
- Part 2 (vol. 31-2): digital filtering concepts and DSP filtering algorithms
- Part 3 (vol. 31-3): implementation of a finite-impulse- response (FIR) filter algorithm and an overview of a demonstration hardware platform, the ADSP-2181 EZ-Kit Lite™.

Now, we look more closely at DSP programming concerns that are unique to real-time systems. This article focuses on how to develop algorithms for DSP systems with a variety of I/O interfaces.

What does "real-time" mean? In an analog system, every task is performed in "real time" with continuous signals and processing. In a digital signal-processing (DSP) system, signals are represented with sets of samples, i.e., values at discrete points in time. Thus the time for processing a given number of samples in a DSP system can have an arbitrary interpretation in "real time", depending on the sampling rate. The first article in this series introduces the concept of sampling and the Nyquist criterion—that in real-time applications, the sampling frequency must be at least twice the frequency of the highest frequency component of interest in the (analog) signal (Nyquist rate). The time between samples is referred to as the sampling interval. To consider a system as operating in "real time," all processing of a given set of data (one or more samples, depending on the algorithm) must be completed before new data arrives.

This definition of real time implies that, for a processor operating at a given clock rate, the speed and quantity of the input data determines how much processing can be applied to the data without falling behind the data stream. The idea of having a limited amount of time with which to handle data may seem odd to analog designers because this concept does not have a parallel in analog systems. In analog systems, signals are processed continuously. The only penalty in a slow system is limited frequency response. By comparison, digital systems process parts of the signal, enough for very accurate approximations, but only within a limited block of time. Figure 1 shows a comparison. Real-time DSP can be limited by the amount of data or type of processing that can be completed within the algorithm's time budget. For example, a given DSP processor handling data values sampled at, say, 48-kHz (audio signals), has less time to process those data values, including execution of all necessary tasks, than one sampling 8-kHz voice-band data.

In the filter example described earlier in this series, the input sampling rate is 8 kHz. For the DSP in the example to keep up with real-time data, all processing has to be done within a time budget of 1/(8 kHz), or 125 µs. On a 33-MHz digital signal-processor (30 ns per cycle), the time budget provides 125 µs/30 ns, or 4166 instruction cycles, to complete processing and any other required tasks.

Since there is a finite amount of time that can be budgeted to perform any given algorithm, managing time is a central part of DSP system software design. Time management strategy determines how the processor gets notified about events, influences data handling, and shapes processor communications.

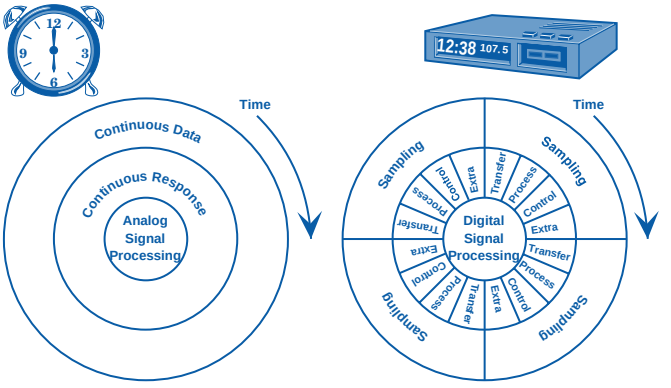

Figure 1. Comparison of analog and digital signal processing. a. Analog: A response value corresponds to each data value at all instants of time. b. Digital: For each sample, the data must be transferred in and processed, an event marks the end of processing (control), and extra time may be necessary for other tasks within the cycle after the designated process occurs.

Event Notification: Interrupts: One can program a DSP to process data using one of several strategies for handling the "event," the arrival of data. A status bit or flag pin could be read periodically to determine whether new data is available. But—"polling" wastes processor cycles. The data may arrive just after the last poll, but it can't make its presence known until the next poll. This makes it difficult to develop real-time systems.

The second strategy is for the data to *interrupt* the processor on arrival. Using interrupts to notify the processor is efficient, though not as easy to program; clock cycles can be wasted during the wait for an interrupt. Nevertheless, event-driven interrupt programming being well-suited to processing real-world signals promptly, most DSPs are designed to deal efficiently with them. In fact, they are designed to respond very quickly to interrupts. The ADSP-2181's response time to an interrupt is about three processor cycles; i.e., within 75 ns the DSP has stopped doing what it was doing and is handling the interrupt event (*vector*).

In many DSP-based systems, the interrupt rates, based on the input data sampling rate, are often totally unrelated to the DSP's clock rate. In the FIR example seen earlier in this series, the processor is interrupted at 125-µs intervals to receive new data.

Interrupt Handling and Interrupt Vectors: Because interrupt processing is such a vital element in DSP systems, processors typically have built-in hardware mechanisms to handle interrupts efficiently. Hard-wired mechanisms are more efficacious than software alone because a DSP's interrupt service routines (ISRs) may have to meet all of the following demands:

- Fast context switching—switch from working on one task and its data (a *context*) to another context without the time loss and complication associated with writing programs to save register contents and chip status information.
- Nested-interrupt handling—handle multiple interrupts of different priorities "simultaneously." The DSP handles one interrupt at a time, but an interrupt of higher priority can take precedence over the handling of a lower-priority interrupt.

- Continue to accept data/record status—while the DSP services an interrupt, events keep on occurring in the real world and data keeps on arriving. To keep up with the "real-world," the DSP must record these events and accept the data—then process them when it has finished servicing the interrupt.

On Analog Devices DSPs, fast context switching is accomplished using two sets of data registers. Only one set is active at a time, containing all the data in process during that context. When servicing an interrupt, the computer can switch from the active to the alternate set without having to temporarily save the data in memory. This facilitates rapid switching between tasks.

To handle multiple interrupts, Analog Devices DSPs record their state for each one. Processor state information is kept on a set of status "stacks" located in the DSP's Program Sequencer. A "stack" consists of a set of hardware registers. Current status information is "pushed" onto the stack when an event occurs. This stack mechanism also allows interrupts to be *nested*; one with higher priority can interrupt one with lower priority.

Two hardware features, interrupt latch and automated I/O, let Analog Devices DSPs stay abreast of the "real world" while processing an interrupt. The latch keeps the DSP from missing important events while servicing an interrupt. The other feature, comprising various forms of automated I/O (including serial ports, DMA, autobuffering, etc.) lets external devices pump data into the DSP's memory without requiring intervention from the DSP. So no data is missed while the DSP is "busy."

When an interrupt request is generated, by an external source or an internal resource, the DSP processor automatically stores its current state of operation, and prepares to execute the interrupt routine. Interrupt routines are dispatched from an interrupt vector table. An interrupt vector table is an area in Program Memory with instruction addresses assigned to particular DSP interrupt functions. For example, in the table below, a Transmit (Tx) interrupt at serial port 1 (SPORT1) of an ADSP-2181 processor will cause the next instruction to be executed at program memory (PM) location 0x0020, followed by the contents of the next three locations, through 0x0023 (the *interrupt routine*). As the 12 items in the table indicate, an ADSP-2181 can handle interrupts from 11 locations (external hardware, DMA ports, and the serial ports) and the processor Reset. The table lists the programmed instructions assigned to each interrupt vector source in memory locations 0x0000 to 0x002F for an FIR filter program.

```
Jump start; nop; nop; nop; /* PM(0x0000-03): Reset vector */
rti; nop; nop; nop;        /* PM(0x0004-07): IRQ2 vector */
rti; nop; nop; nop;        /* PM(0x0008-0B): IRQL1 vector */
rti; nop; nop; nop;        /* PM(0x000C-0F): IRQL0 vector */
ar = dm(stat_flag); ar = pass ar; if eq_rti; jump next_cmd;
                           /* PM(0x0010-13): SPORT0 Tx vector */
jump input_samples; nop; nop; nop;
                           /* PM(0x0014-17): SPORT0 Rx vector */
jump irqe; nop; nop; nop;  /* PM(0x0018-1B): IRQE vector */
rti; nop; nop; nop;        /* PM(0x001C-1F): BDMA vector */
rti; nop; nop; nop;        /* PM(0x0020-23): SPORT1 Tx vector */
rti; nop; nop; nop;        /* PM(0x0024-27): SPORT1 Rx vector */
rti; nop; nop; nop;        /* PM(0x0028-2B): Timer vector */
rti; nop; nop; nop;        /* PM(0x002C-2F): Powerdown vector */
```

Each interrupt vector has four instruction locations. Typically, these instructions will cause the processor to jump to another area of memory in order to process the data, as is shown in the Reset (at 0x0000), SPORT0 Rx (0x0014), and IRQE (0x0018) interrupt vectors. If there are just a few steps—such as reading a value, checking status, or loading memory—that can be done within the four available instruction locations, they are programmed directly, as shown in the SPORT0 Tx vector (0x0010-13). Any unused interrupt vectors call for return from interrupt (rti), with three nop (no operation) instructions.

The nop instructions serve as place holders—instruction space used to ensure that the correct interrupt action lines up with the hardware-specified interrupt vector. The rti instruction at the beginning of each unused vector location is both placeholder and safety valve. If an unused interrupt is mistakenly unmasked or inadvertently triggered, "rti" causes a return to normal execution.

Data I/O

In DSP systems, interrupts are typically generated by the arrival of data or the requirement to provide new output data. Interrupts may occur with each sample, or they may occur after a frame of data has been collected. The differences greatly influence how the DSP algorithm deals with data.

For algorithms that operate on a sample-by-sample basis, DSP software may be required to handle each incoming and outgoing data value. Each DSP serial port incorporates two data I/O registers, a *receive* register (Rx), and a *transmit* register (Tx). When a serial word is received, the port will typically generate a Receive interrupt. The processor stops what it is doing, begins executing code at the interrupt vector location, reads the incoming value from the Rx register into a processor data register, and either operates on that data value or returns to its background task. In the table above, the computer jumps to a program segment, "input_samples", performs whatever instructions are programmed in that segment, and returns from the interrupt, either directly or via a return to the interrupt vector.

To transmit data, the serial port can generate a Transmit interrupt, indicating that new data can be written to the SPORT Tx register. The DSP can then begin code execution at the SPORT Tx interrupt vector and typically transfer a value from a data register to the SPORT Tx register. If data input and output are controlled by the same sampling clock, only one interrupt is necessary. For example, if a program segment is initiated by Receive interrupt timing, new data would be read during the interrupt routine; then either the previously computed result, which is being held in a register, would be transmitted, or a new result would be computed and immediately transmitted—as the final step of the interrupt routine.

All of these mechanisms help a DSP to approach the ability to emulate what an analog system does naturally—continuously process data in real time—but with digital precision and flexibility. In addition, in an efficiently programmed digital system, spare processor cycles left between processing data sets can be used to handle other tasks.

Programming Considerations

In a "real-time" system, processing speed is of the essence. By using SPORT autobuffering, no time is lost to data I/O. Instead, the data management goal is to make sure that the selected address points to the new data.

In the FIR filter example (*Analog Dialogue* 31-3, page 15), a SPORT Receive interrupt request is generated when the input autobuffer is full, meaning that the DSP has received three data words: status, left channel data, and right channel data. Since this simplified application uses single-channel data, only the data value that resides at location rx_buf+1 is used by the algorithm.

Filter Algorithm Expansion In other applications, the data handling can be more involved. For example, if the FIR filter of the example were expanded to a two-channel implementation, the core DSP algorithm code would not have to change. The code relating to data handling, however, would have to be modified to account for a second data stream and a second set of coefficients.

In the filter code, two new buffers in memory would be required to handle both the additional data stream and the additional set of coefficients. The core filter loop may be isolated as a separate "callable" function. This technique lets the same code be used, regardless of the input data values. Benefits of this programming style include readable code, re-usable algorithms, and reduced code size. If a modular approach is not taken, the filter loop would have to be repeated, using additional DSP memory space.

The SPORT Receive interrupt routine would then consist of the setting of pointer and calling the filter. The revised filter routine is shown in the following listing:

```
Filter: cntr = taps - 1;
mr = 0, mx0 = dm(i2,m1), my0 = pm(i5,m5);
                          /* clear accumulator, get first data
                          and coefficient value */
do filt_loop until ce;    /* set-up zero-overhead loop */
filt_loop: mr = mr + mx0*my0(ss), mx0 = dm(i2,m1),
my0 = pm(i5,m5);          /* MAC and two data fetches */
mr = mr + mx0 * my0 (rnd); /* final multiply, round to 16-bit
                          result */
if mv sat mr;             /* check for overflow*/
rts;                      /* return */
```

It's important to note that the only modifications to the core filter loop were the addition of a label, "Filter:" at the beginning of the routine, and the addition of an "rts" (return from subroutine) instruction at the end. These additions change filter code from a stand-alone routine into a subroutine that can be called from other routines. No longer a single-purpose routine, it has become a re-usable, callable subroutine.

With the core filter set up as a callable subroutine, the two-channel data handling requirements can now be addressed. To simplify some of the programming issues, this example assumes that both the left and right channels use the same filter coefficients.

In the third installment of this series, the entire filter application assembly code was displayed. At the top of the code listing, all of the required memory buffers were declared. To expand the filter application to handle two channels of data, the required new variables and buffers need to be declared. For the incoming data, the buffer declaration,

```
.var/dm/circ_filt_data[taps]; /* input data buffer */
```

would need to be replaced with two buffers, declared as

```
.var/dm/circ_filt1_data[taps]; /* left channel input data buffer */
.var/dm/circ_filt2_data[taps]; /* right channel input data buffer */
```

Because both channels are to have the same filter coefficients applied to them, the data buffers are of equal length.

The filter loop subroutine expects certain data and coefficient values to be accessed using particular address registers. Specifically, address register I2 must point to the oldest data sample, and I5 must point to the proper coefficient value prior to the filter routine being called.

Because the filters for both the left and right channel will be sharing the same memory pointers, there has to be a mechanism for differentiating the two data streams. For the data pointer, I2, two new variables need to be defined, "filter1_ptr" and "filter2_ptr." These locations in memory are going to be used to store address values appropriate for each data stream. The circular buffering capability of the ADSP-2181 is used to ensure that the data pointer is always in the correct place in the buffer whenever the filter is executed. Because the subroutine is now dealing with two buffers, the pointer locations need to be saved when processing for each channel is completed.

To set up the pointers, two variables in data memory need to be declared as follows:

```
.var/dm filter1_ptr;   /* data pointer for left channel data */
.var/dm filter2_ptr;   /* data pointer for right channel data */
```

These variable then need to be initialized with the starting address of each of the data buffers;

```
.init filter1_ptr: ^filt1_data; /* initialize starting point,
                                left channel */
.init filter2_ptr: ^filt2_data; /* initialize starting point,
                                right channel */
```

The DSP assembler software recognizes the symbol "^" to mean "address of." The DSP linker software fills in the appropriate address value. In this way, the pointer variables in the executable program are initialized with the starting addresses of the appropriate memory buffers.

The following listing shows how the FIR Filter interrupt routine uses these new memory elements. The original Filter subroutine from the 3rd installment has been modified to provide two separate channels of filtering. Instead of launching directly into the filter calculation, the routine must first load the appropriate data pointer. The filter routine is then called, and the resulting output is placed in the correct location for transmission.

```
/* ---------------------  FIR Filter ----------------------*/

input_samples:
   ena sec_reg;           /* use shadow register bank */

/* set up for filter 1 */
i2 = dm(filter1_ptr);     /* set data pointer for filter 1 */
ax0 = dm(rx_buf + 1);     /* read left channel data */
dm(i2,m1) = ax0;          /* write new data into delay line,
                          pointer now pointing to oldest data */

call filter;              /* perform the first filter for left
                          channel data */

dm(tx_buf+1) = mr1;       /* write left-channel output data */
dm(filter1_ptr) = i2;     /* save updated filter1 data pointer */

/* set up for filter 2 */
i2 = dm(filter2_ptr);     /* set data pointer for filter 2 */
ax0 = dm(rx_buf + 2);     /* read right channel data */
dm(i2,m1) = ax0;          /* write new data into delay line,
                          pointer now pointing to oldest data */

call filter;              /* perform the filter again for the
                          right channel data */

dm(tx_buf+2) = mr1;       /* write right channel output data */
dm(filter2_ptr) = i2;     /* save updated filter2 data pointer */

rti;                      /* return from interrupt */
```

Because the core filter algorithm no longer handles data I/O, this subroutine can be expanded to more channels of filtering by merely adding more pointer variables and declaring more buffer space (as long as sufficient memory exists!) Similarly, different coefficients can be used for the two filters by setting up variables that contain coefficient-buffer pointer information. In either case, the filter algorithm does not need to be altered. By using this style of modular programming, the user can build up a library of callable

DSP functions. Differences for particular systems can thus be reduced to data-handling issues rather than the development of new algorithms. While this programming style does not necessarily allow the algorithm to perform its task more quickly, the system designer has more flexibility in establishing how data flows through the system.

Real-Time Interface Issues: So far, we have examined how real-time programming in embedded systems relies on rapid interrupt response, efficient data handling, and fast program execution. In addition, the flow of data into and out of the processor also influences how well the system will work in a real-time embedded environment.

The primary data flows into and out of a digital signal processor can be both parallel and serial. Parallel transfers are typically at least as wide as the native data word of the processor's architecture (16 bits for an ADSP-2100 Family processor, 32 bits for the SHARC®). Parallel transfers occur via the external memory bus or external host interface bus of the processor. Serial data transfers require considerably fewer interconnections; they are frequently used to communicate with data converters.

Serial Interface: Ease of hardware interfacing is an important element of efficient DSP system implementation. The ADSP-2181 EZ-Kit Lite system uses an AD1847 serial codec (COder/DECoder). Serial codecs permit data transfers via a serial port (SPORT) on the DSP. This serial port is not an RS-232 PC-style asynchronous serial port; it is a 5-wire synchronous interface that passes bit-clock, Receive-data, Transmit-data, and frame-synchronization signals. Major benefits of serial interfaces are low pin count and ease of hardware hookup. The AD1847 requires only 4 signals to interface to the DSP: serial clock, Receive data, Transmit data, and Receive frame-synchronization signal. The serial data stream is time-division multiplexed (TDM), meaning that the same physical line can carry more than one type of information in serial order. In the case of the AD1847 application on EZ-Kit Lite, initiated in the last issue, the serial line carries both left- and right-channel audio information, along with codec control and status information. As noted earlier, the processor has various means for handling this data. SPORT Interrupts are generated automatically by the serial port hardware for either Receive or Transmit data and for either a single word or a block of words (Figure 2).

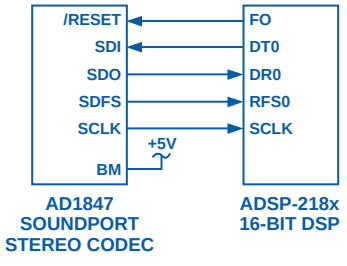

Figure 2. Serial interfacing between digital signal processor and I/O device.

Parallel Interface: Even with a serial bit clock running as fast as the DSP processor, a serial interface trades data transfer speed for simplicity of wiring, transferring a data word at a fraction of the DSP processor speed. For system performance that requires higher data rates, a parallel interface can be used. When interfacing in parallel, the DSP exercises its external data and address busses to read or write data to a peripheral device. On the ADSP-2181, the buses can interface with up to 16 bits of data.

Parallel data transfer is always faster than serial transfers. The DSP can perform an external access every processor cycle, but this requires really fast parallel peripherals that can keep up with it, such as fast SRAM chips. Parallel data transfers with other entities usually occur at less than one per processor cycle.

Interrupt handling is different for the serial and parallel interfaces. Since the external data bus of the DSP processor is a general-purpose entity handling all sorts of data, it does not have dedicated signal lines for interrupt generation and control; however, other DSP resources are available. On the ADSP-2181, several external hardware interrupt lines, such as the one for I/O memory select, are available for triggering by an external device, such as an A/D converter or codec. Such an interface is shown in Figure 3, involving a parallel device and the ADSP-2181 DSP.

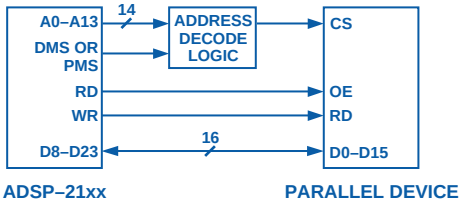

Figure 3. Parallel I/O interfacing for a DSP.

When responding to the interrupt for parallel data, the processor reads the appropriate source and typically places that data value in memory, by executing instructions similar to those shown here:

```
irq2_svc: ax0 = IO(ad_converter); dm(i2,m1) = ax0; rti;
```

"ad_converter" is a previously defined address in I/O space.

REVIEW AND PREVIEW

The goal of this article has been to detail the programming concerns that DSP developers face when handling I/O and other events in real-time systems. Issues introduced include real-time data (samples and frames), interrupts and interrupt-handling, automated I/O, and generalizing routines to make callable subroutines. This brief article could not do justice to the many levels of detail associated with each of these topics. Further information is available in the references below. Future topics in this series will continue to build on this application. The next article will add more features to our growing example program and describe software validation (i.e., debugging) techniques.

REFERENCES

ADSP-2100 Family Assembler Tools & Simulator Manual. Consult your local Analog Devices Sales Office.

ADSP-2100 Family User's Manual. Analog Devices. Free.

Many valuable publications can be found in the Design Support area of our Web site under Product Documentation. A useful bookmark is:

http://www.analog.com/support/product_documentation/dsp_prdoc.html

Oversampling ADCs for 16-Bit Resolution

2.5-MHz AD9260 (>1-MHz inputs)
1.2-MHz AD7723 (≤460-kHz input)

Analog Devices has introduced two new CMOS high-speed 16-bit oversampling A/D converters for handling wideband signals with wide dynamic range in applications where low power, small footprint, and low-cost monolithic solutions are essential.

The **AD9260**, using a 20-MSPS clock in an 8× oversampling mode (Figure 1), can output 16-bit signals at a 2.5-MHz word rate, providing a 1.01-MHz signal passband with 0.004-dB ripple and 100-dB SFDR (spurious-free dynamic range). The **AD7723**, with a 19.2-MHz clock, and using 16× oversampling, can provide 16-bit performance for 460-kHz inputs, at a 1.2-MHz output word rate. In less-demanding applications, to conserve battery capacity, the AD9260's power requirement can be reduced from 585 mW to 150 mW; and the AD7723's 500-mW can be halved. The AD7723 also has a 200-µW standby mode. The table provides a few additional points of comparison.

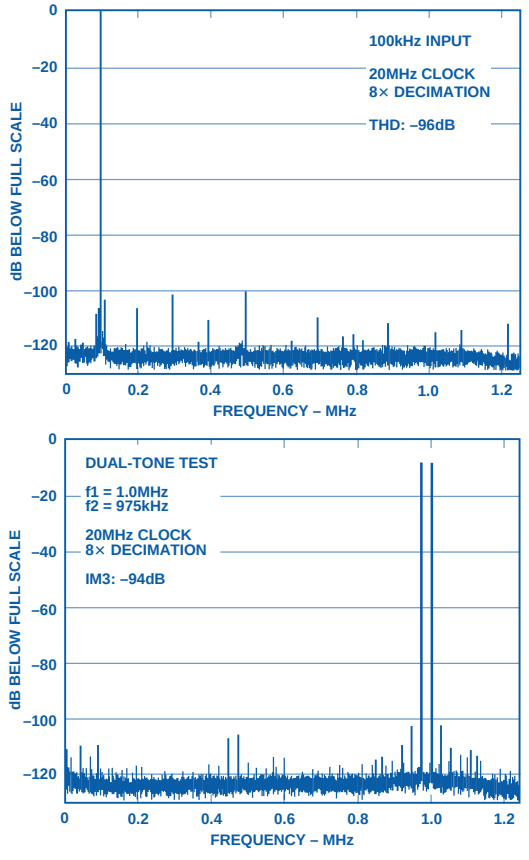

Figure 1. AD9260 SFDR: single (100-dB) and dual-tone (95-dB) performance.

Both devices have internal references; the AD7723 provides 2.5 V, and the AD9260's reference has both 1.0 and 2.5-V modes. They are housed in 44-pin QFP packages, the AD9260 in MQFP, and the AD7723 in PQFP. Both will operate with +5-V analog and digital supplies, but the AD9260's digital supplies are specified in +3 V operation for power economy and minimum noise. Evaluation boards are available for each type.

Characteristic	**AD9260**	**AD7723**
Resolution, bits	16	16
Sample rate, MSPS	20	19.2
Output data rate, MSPS @ OSR	2.5 @ 8×	1.2 @ 16×
Oversampling ratio selection	1×, 2×, 4×, 8×	16×, 32×
Filtering characteristic	LP	LP, BP
Power dissipation, mW (max)	630	500
Dissipation reduction, mW	to 150	50%, 200 µW
Internal reference, V	1,2.5	2.5
SFDR, dB (low-frequency signals)	100	90
SNR, dB, 1.2 MHz thruput	88.5 typ	83 min
44-pin package	MQFP	PQFP
Faxcode,* **or circle** (reply card)	2155, **6**	2103, **7**
Price, USD (1000s)	$39.90	$23

Typical applications: 16-bit performance at wide bandwidths and high sampling rates is especially useful in communications equipment. A key example is in echo cancellation in modems for full-duplex communications, where the same channel is shared for simultaneously transmitted and received signals (Figure 2). In such equipment, a strong transmitted signal (and its echoes) and a weak received signal may be in close proximity in time or frequency. In order to sort them out using DSP techniques, the signal must first be converted to digital without losing small components in noise and without generating spurious components (spurs) by distorting large components. This calls for a wide-dynamic-range device that has high SFDR with low distortion (both harmonic and intermodulation) and low quantization noise.

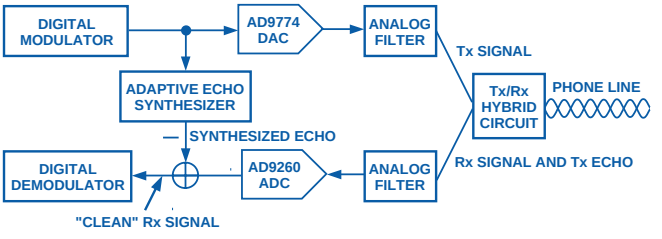

Figure 2. Full-duplex digital error-cancelling modem.

The AD9260 has been successfully evaluated for wire-line and wireless communication applications, such as wideband cellular base stations, echo cancelling ADSL modems, single-pair HDSL modems, navigational systems, and broadband CDMA base stations. The high speed, dynamic range, low power, high-level integration, and low price of both devices make them useful in sonar, radios, instrumentation, test equipment, and in other signal-capture and -analysis applications. When its throughput is suitable, the AD7723's low cost and special properties are useful in bandpass applications, where a standby condition is necessary, where choice of serial or parallel operation is required, and/or where an oversampling ratio of 16 or more is desirable.

ARCHITECTURAL CONSIDERATIONS

Sigma-delta A/D converters traditionally offer high resolution at low cost for industrial, audio and low-frequency communication applications, but the tradeoffs between resolution and speed have generally limited bandwidths to below 200 kHz. Second-order single-bit modulators can meet the high resolution requirements of the industrial market, but at the cost of large oversampling ratios (OSR) and inherent unsuitability for high output-data-rate (ODR) applications.

*For data, consult our Web site, **www.analog.com** ("Product Center"), AnalogFax line **800-446-6212** (with Faxcode), or use the reply card.

Increased bandwidth is typically pursued with single-loop modulators by increasing the order of integration in the loop. For example the AD7722, which uses a 7th-order modulator, has 90-dB SNR at a 195-kHz output data rate, while being clocked at 12.5 MHz. To improve bandwidth by increasing the ODR rate of such converters would be difficult because it would require a more costly manufacturing process and power-hungry integrating amplifiers capable of settling to the required accuracy. Thus practical considerations limit the single-loop single-bit architecture to output data rates of 100-200 kHz.

To extend the resolution/bandwidth frontier, new architectures are required. Though the details are beyond the scope of this brief discussion, it is worth noting that the AD9260 ventures into new ground to achieve a state-of-the-art *tour de force* solution; and AD7723 successfully implements an advanced cascade design approach. The single-bit DACs used in most of our sigma-delta ADCs, although guaranteeing excellent distortion, generate large amounts of quantization noise that degrades SNR. By using multi-bit DACs within the modulator and employing shuffling techniques to randomize the non-linearity of the DACs, both high resolution and good distortion are realized in the AD9260. To reduce the effect of quantization noise further, in both the AD9260 and AD7723, the quantization noise added by the DACs is first measured and then subtracted digitally.

FEATURES AND PERFORMANCE

The **AD9260** (Figure 3) achieves both high dynamic range and very wide input signal bandwidth at a modest 8× oversampling ratio by combining sigma-delta techniques with a high-speed pipelined A/D converter. The differential analog input is fed into a 2nd-order sigma-delta modulator employing a 5-bit flash quantizer and 5-bit feedback. At the same time, a 12-bit pipelined A/D converter quantizes the input to the flash converter with greater accuracy. The loop architecture provides the equivalent of a stable second-order loop with 12-bit quantizer and 12-bit feedback, free from idle tones and other idiosyncrasies sometimes associated with higher-order single-bit ∑-Δ modulators.

The modulator output is fed into a three-stage decimation filter, and a MODE control allows the output to bypass any or all stages,

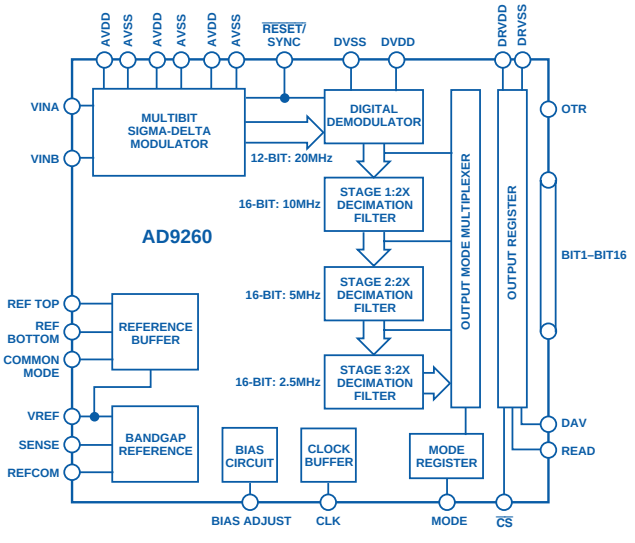

Figure 3. AD9260 block diagram.

providing the choice of output at the clock rate (1×), or decimated by 2×, 4×, or 8×. The decimation filter's stopband rejects frequencies between 1.25 and 18.75 MHz, substantially easing antialiasing requirements on the analog input. A reference, with buffer, is provided on-chip. In the 2.5-V mode (optimum noise & distortion), 4-V p-p full-scale differential inputs can be handled. In the 1-V mode, the range is 1.6 V p-p. Arbitrarily programmable values are also available via an external resistive divider. A bias adjustment scales the power proportionally to the clock rate, permitting reduced dissipation (and performance) over clock rate reduction from 20 to 5 MSPS and 585 to 150 mW.

The **AD7723** (Figure 4) uses a number of cascaded first and second-order sigma-delta modulators, each comprising one or more integrators, a comparator, and a 1-bit DAC. The first modulator performs the actual analog-to-digital conversion, and the modulators that follow, with their correction logic, successively remove the quantization noise contributed by the preceding modulators and at the same time lower their own noise floor by shifting their own quantization noise upward in frequency. To meet the performance requirements of the AD7723, 5th order noise shaping was employed, resulting in an output that contains only the input signal and 5th-order shaped quantization noise from Modulator 4.

The AD7723 can be clocked at up to 19.2 MHz. A 5-stage FIR decimation filter is used to both reduce the output data rate and remove the out-of-band quantization noise. The ADC output can be taken from either the 4th or the 5th filter. Data from the fourth filter has an output data rate (ODR) of 1.2 MHz and a SINAD of 85 dB, while data from the 5th filter has an ODR of 600 kHz but a higher SINAD of 88 dB. The 5th filter can also be configured as a high-pass filter, allowing the AD7723 to be used as a band-pass ADC.

The AD7723 provides flexible serial or parallel interfacing, high oversampling rate (OSR) to minimize anti-alias filter complexity, and accepts unipolar or bipolar inputs for simple interfacing to input drive circuits. Operating temperature range is –40 to +85°C.

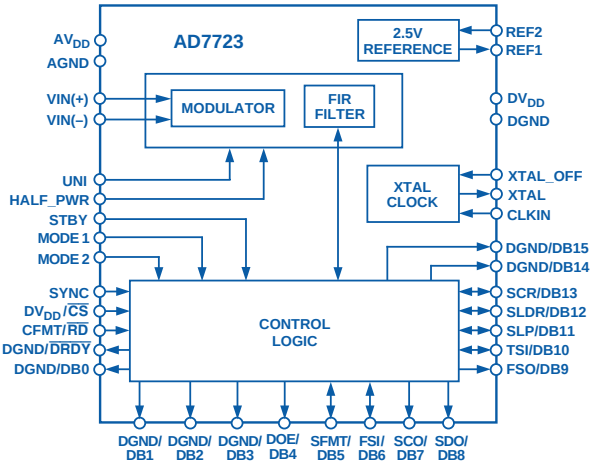

Figure 4. AD7723 block diagram.

The AD9260 was designed by a team comprising members of our high-speed converter group, in Wilmington, MA, led by Todd Brooks. The AD7723 was designed by Peter Hurrell (who also furnished much of the above text) and Colin McIntosh, of our design group in Newbury, England.

Analog-to-Digital Converters

High-Resolution Σ–Δ

24-b AD7730L,16-b AD7705/6

AD7720 7th-order modulator

The AD7730L is a complete 24-bit low-noise A/D converter with an on-chip PGA for digitizing low-frequency signals, e.g., from bridge transducers. It runs from a single +5-V supply, consuming 23.5 mW, packaged in 24-lead SO & TSSOP. Price (1000) $8.12. **Faxcode 2112 or Circle 8**

The 16-bit **AD7705/06** are complete low-cost ADCs, including an on-chip PGA, for dc and low-frequency measurement applications. Power required is low (1 mW max at +3 V), and they are housed in DIP, SO and TSSOP-16. Price (1000) is $4.12. **Faxcode* 2156 or Circle 9**

The **AD7720**, a 7th-order Σ–Δ modulator, is typically used in 16-bit ADCs. Designed for use with custom filters, its output is a stream of 1s and 0s at up to 12.5 MHz. It operates from a single +5-V supply and is available in a TSSOP-28. Price is $8.00 (1000). **Faxcode 2431 or Circle 10**

12/10-Bit, 65/60 MSPS

AD6640: Fastest IF-sampling

AD9051: Lowest power

The **AD6640** is designed to be at the heart of digital radio receivers. With 80-dB SFDR at 65 MSPS, it can accurately sample 30-MHz bandwidths and handle content up to 70 MHz, allowing programmable digital filters to replace expensive analog filters. It dissipates 710 mW from a single +5-V supply (outputs can run from 3.3 V). An evaluation board is available. The AD6640 is housed in a 44-lead TQFP; 1000s price is $57.20. **Faxcode 2142 or Circle 11**

Using 250 mW typical, 315 mW max, the **AD9051** is the lowest-power 10-bit, 60-MSPS ADC available at this writing. Dynamic performance includes 58-dB (56 min) SNR (9.3 ENOB) @ 10.3-MHz AIN. Typical applications include medical imaging, instrumentation, communications. In 28-lead SSOP, it operates on +5-V (compatible with 3-V logic). Price (1000s): $8.50. **Faxcode 2164 or Circle 12**

10-Bit Temp-to-Digital

AD7817: 4 channels + temp.

AD7416: Instead of LM75

The AD7817 is a 10-bit, 9-µs a/d converter with 3-wire serial output. Its input mux chooses among four analog inputs and an internal temperature sensor with ±1° max error at 25°C (B version). It operates over a 2.7 to 5.5-V supply range with low power consumption (3 µW at 10 samples per second), including a 50-nA power-down mode. Temperature range is –40 to +85°C, and a –55 to +125°C S version is available. It is packaged in a 16-lead narrow-body SOIC. Prices start at $2.95 (1000). **Faxcode 2091 or Circle 13**

The **AD7416** is a complete temperature monitoring system on a single chip. It is an improved direct replacement for the LM75 10-bit temperature-to-digital converter with setpoint comparator; it is available in 8-pin SOIC and microSOIC packages. Operating range is 2.7 to 5.5 V, and it consumes 3 µW at 10 samples/second. Price (1000) is $1.30. **Faxcode* 2437 or Circle 14**

8-Bit Serial & Parallel

Serial-out 1-MSPS AD7827

1-, 4-, 8-ch AD7822/25/29

The **AD7827** is a low-power 8-bit ADC for direct serial interfacing to most popular DSPs. Conversion time is 420 ns, with up to 1-MSPS throughput, depending on the clock speed of the DSP's serial interface. Specified to operate from –40 to +85°C with 3-V or 5-V supplies, it is housed in an 8-pin plastic DIP or SOIC. Price in 1000s is $2.60. **Faxcode 2238 or Circle 15**

The **AD7822/25/29** form a family of three 8-bit microprocessor-compatible converters, with, respectively, 1, 4, and 8 channels of input. Included on chip are a 2.5-V reference, multiplexer of appropriate width, track-hold amplifier, half-flash ADC, and a high-speed parallel interface. The converters can operate from a single +3-V (±10%) or +5-V (±10%) supply. They are available, respectively, in 20/24/28-pin choice of DIP, SOIC, and TSSOP packages. Respective prices (1000s) are $2.95/$3.40/$3.70. **Faxcode* 2106 or Circle 16**

10 & Dual 10/8-Bit Fast

AD9202: 10-bit, 32-MSPS

AD9201/81: Dual 20/28MSPS

The **AD9202** is a complete high-speed, 10-bit 32-MSPS CMOS ADC (including a built-in dc-restore clamp circuit) ideally suited for video and communications applications. The 300-MHz-BW sample-hold permits Nyquist or undersampled (40-45-MHz IF) scenarios. It is housed in a 28-lead SSOP, uses 2.7 to 5.5-V supplies (90 mW on 3 V). Price (1000s) is $4.97. **Faxcode* 2484 or Circle 17**

The **AD9201** and **AD9281** are complete *dual* (well-matched I and Q channel on each) 10- and 8-bit ADCs with respective sampling rates of 20- and 28-MSPS for use in wideband communications receivers. They can operate on +3 or +5-V supplies. Respective SFDRs are 73 dB and 65 dB. They are housed in 28-lead SSOP. Prices (1000s) are $5.27 and $4.23, respectively.

AD9201 **Faxcode 2116 or Circle 18**

AD9281 **Faxcode 2117 or Circle 19**

Multichannel 14,12-Bit

14: AD7856 (8 ch), AD7863 (2×2)

12: AD7864 (4-ch coincident)

The **AD7856** is a complete 14-bit sampling A/D converter with an 8-channel multiplexer on a single chip with throughput rate of 285 ksps per channel. It runs from a single +5-V supply, consuming 60 mW (5 µW in "sleep"), packaged in 24-lead DIP, SO & SSOP. Price (1000) starts at $9.90. **Faxcode 2085 or Circle 20**

The **AD7863**, with a pair of 14-bit ADCs, each having a pair of multiplexed inputs, is pin-compatible with 12-bit AD7862. It runs off a single 5-V supply and accepts input levels of ±10/±2.5/+2.5 V. It is housed in 28-pin SOIC & SSOP. Price (1000) starts at $14.50. **Faxcode* 2086 or Circle 21**

The **AD7864** is a highly integrated 4-channel simultaneous-sampling fast (0.35-µs acquisition time, 1.6 µs conversion time) 12-bit A/D converter in a PQFP-44. It operates from a single +5-V supply, and has 6 input ranges ≤±10V. Price starts at $13.65 (1000). **Faxcode 2087 or Circle 22**

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Digital-to-Analog Converters

14-Bit, 32-MSPS DAC

4× interpolation filters permit 13.5-MHz data reconstruction

The AD9774 is the first high-speed D/A converter on the market to achieve SFDR performance >78 dB for output signals of up to 13 MHz. This TxDAC+™ integrates a complete low-distortion 14-bit TxDAC® core with a voltage reference, a 4× digital interpolation filter, and a 4× PLL clock multiplier. The two-stage, 4× digital interpolation filter reduces both passband distortion and the cost and complexity of analog reconstruction filters. It is useful in all sorts of wideband wireline and wireless digital data-transmission applications.

The AD9774's on-chip PLL multiplier generates all necessary clocks from the user's data clock to support an input data rate of up to 32 MSPS and a DAC output rate of 128 MSPS. The AD9774 operates from a 2.7-V to 5.5-V supply, is specified from –40 to +85°C, and is available in a 44-pin MQFP package. Price is $24.95 (1000).

Faxcode* 2168 or Circle 23

10-Bit 170-MHz DAC

Lo-cost AD9731: fast, cool, tiny For GP, set-top, cable, comms

The AD9731, a direct replacement for the AD9721 (*Analog Dialogue* 26-2, 1992), can provide a 75% increase in throughput rate at 40% of the power. A 28-lead space-saving (50%) SSOP version is available, as well as a 28-lead SOIC, both at a substantially lower price ($10.17 in 1000s).

A general-purpose DAC with good wideband and narrowband spur performance, it is useful in waveform reconstruction and capable of interfacing with high-speed CMOS and TTL logic. Its high 175-MHz throughput rate supports 5 to 65-MHz upstream hybrid fiber cable (HFC) and 70-MHz direct IF for communications, the latter further supported by a wideband SFDR of 50 dB at 65 MHz. Settling time to within 1/2 LSB is 3.8 ns.

It operates on +5 and –5.2-V supplies, and typically dissipates 440 mW in 170-MSPS operation. Its internal reference is 1.25 V.

Faxcode 2167 or Circle 24

8/10/12 Bits in SOT23

Serial-input AD5300/10/20 250 µA max over temperature

This unique family of DACs, offering 8, 10, and 12-bit resolutions, offer the package choice of tiny 6-lead SOT-23 and 8-lead microSOIC. Specified to operate on 2.7 to 5.5-V single supply, they draw 250 µA max of quiescent current, over the –40 to +105°C range, and only 1 µA max under power-down conditions. Their small size and low power requirement makes them especially appropriate for portable battery-powered instruments.

Their serial interface, compatible with SPI™, QSPI™, MICROWIRE™, and DSPs, operates with clock speeds up to 30 MHz. They have rail-to-rail buffered voltage outputs (1 V/µs slew rate), are guaranteed monotonic. Power-on reset is to 0 V. The reference is power-supply based.

	AD5300	AD5310	AD5320
Resolution (bits)	8	10	12
Price(1000)	$1.25	$1.70	$2.50
Faxcode*	2173	2197	2405
Circle	**25**	**26**	**27**

Quad 8-Bit DACs

Serial/Parallel AD7304/05 +3 to +5-V Supply or ±5 V

The AD7304 and AD7305 are 4-channel 8-bit DACs which operate from a single +3 to +5-V supply or from ±5-V supplies. Double buffered, the **AD7304** has a serial interface and the **AD7305** has a parallel interface. The DACs are multiplying types with buffered rail-to-rail outputs. The individual reference inputs can swing over the power-supply range, with 2.6-MHz bandwidth.

Typical applications are in digitally controlled calibration and in gain adjustment of ac signals. When operating from less than 5.5 V, the AD7305 is pin-compatible with the popular industry-standard AD7226.

Both types are available in P-DIP, SOIC, and 1.1-mm-high TSSOP packages; AD7304s have 16 leads, AD7305s have 20 leads. Temperature range is –40 to +85°C, and extended temperature-range devices are available. AD7304/05 prices (1000s) start at $3.25/ $3.75 in SOIC packages.

Faxcode* 2088 or Circle 28

12/10-Bit Duals

Low-Power AD7394/95 200 µA max, 0.1 µA shutdown

The **AD7394** and **AD7395** are pin-compatible dual D/A converters, with serial data interfaces and 12- and 10-bit respective resolutions. Operating from +2.7 to +5.5 V, they draw maximum quiescent current of 200 µA. They are useful in digitally controlled calibration, process control, communications, automotive.

Output buffer amplifiers swing rail-to-rail, and the reference can be directly derived from the power supply; or, for even more efficient operation, the devices' very low power (only 600 µW at 3 V) can be derived from a *reference* source.

They are packaged in 14-lead P-DIPs and SOICs. The AD7395 is also offered in ultra-compact TSSOP, only 1.1 mm high—compatible with PCMCIA cards. The AD7394 operates from –40 to +85°C, and the AD7395 operates from –40 to +125°C. Respective prices (1000) are $5.74/$3.38.

Faxcode* 2089 or Circle 29

10-Bit, 240-MHz Video

ADV7123/7127 triple/single Low cost, low power, +5 & +3 V

The monolithic **ADV7123** has three 10-bit video-speed DACs with complementary current outputs and an on-chip voltage reference. It is compatible with a variety of high-resolution color graphics systems, including RS-343A and RS-170A. The part also includes a number of low-power modes, including a power-save feature. It comes in a tiny 48LQFP, and operates from –40 to +85°C. Prices (1000) range from $5.95.

Faxcode 2243 or Circle 30

The **ADV7127** is a single-DAC version of the 240-MHz high-speed low-cost, low-dissipation on-chip-referenced ADV7123. Its variety of applications include graphics display (up to 1600 × 1200 pixels @ 100 Hz), digital video, modulation schemes, and general-purpose video-speed applications. It is specified for –40 to +85°C operation and is available in a 24-lead TSSOP and 28-lead SOIC. Prices (1000) start at $4.84.

Faxcode* 2244 or Circle 31

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Amplifiers

5-μA max in SOT-23

OP186: Fast recovery; rail-rail
OP181: 4 μA max in DIP/SOIC

The OP186 is a low-voltage, low-power (12.1 μW @ 2.2 V), single op amp with rail-to-rail outputs. Performance is specified at +2.2V, +2.7V, +5.0 V, and ±5.5V. It is housed in a tiny SOT-23 5-lead package and operates from –40 to +125°C. The **OP181**, available in plastic DIP and SOIC packages and specified at +3, +5, and ±5.5 V, is somewhat identical but is optimized for offset voltage. It has lower quiescent current and less bandwidth, and is specified from –40 to +85°C. The Table compares some key specifications:

	OP186		OP181
Supply voltage	+2.2	+5	+5
I_{SY} (μA max)	5	6	4
V_{OS} (mV max)	5	5	1.5
GBP (kHz)	150	155	100
Sat. recov (μs)	NS	60	120
Price (1000s)	$1.09		$1.69
Faxcode*	2096		2075
Circle	**32**		**33**

Single-Supply In-Amp

Low-cost AD623: R-R output
84-dB CMR; I_{SY} 550 μA max

The AD623 instrumentation amplifier is used to sense and amplify the difference between two voltages while rejecting common-mode voltage. This function is frequently assembled by users with op amps and passive components, a "kludge" using excessive space, power, expense, and diversion of design talent. The AD623 replaces all this—a low-cost, low-power, single-supply, low-offset-and-drift amplifier in a small package (miniDIP, μSOIC or SO); a single external resistor sets the gain.

It can operate on a single 3-V to 12-V supply (480 μA max @ 5 V), and its performance is specified for +5 V and ±5-V supplies (550 μA max). Its output can swing essentially rail-to-rail. Offset is only 200 μV max, drift is 2 μV/°C (A grade), and common-mode rejection (CMR) is 84 dB min (G = 5). Price in 1000s starts at $1.55.

Faxcode 2109 or Circle 34

Fast, High Efficiency

AD8012: Dual 350 MHz,125 mA
AD8010: 25-ns settling, 200 mA

The AD8012 is a dual current-feedback amplifier capable of 350-MHz bandwidth, while drawing only 1.7 mA per amplifier. Intended for high-frequency wide-dynamic-range systems needing low distortion with high speed and efficiency, it is capable of 20-ns settling time and 2,250-V/μs slew rate, and can furnish 125 mA of output current. Specified for –40 to +85°C, and +5 or ±5-V supplies, it is available in 8-lead SOIC and μSOIC. Price is $2.75 in 1000s. **Faxcode* 2054 or Circle 35**

The **AD8010**, with its high speed and output-current, can drive eight 75-Ω cables with high-quality video signals. Performance includes 200-mA output, 800-V/μs slew rate, 25-ns settling, 230-MHz bandwidth, and 73-dBc SFDR at 1 MHz into 18.75 Ω. Specified for ±5-V and –40 to +85°C, it is available in 8-lead DIP and SOIC, and SOIC-16 reels. Prices (1000s) from $2.75.

Faxcode* 2193 or Circle 36

Single Supply R-to-R

AD8054/2/1:100 MHz, lo cost
OP2/450 Low-bias dual/quad

The **AD8054/52/51** are a family of low-cost quad, dual, and single high-speed voltage-feedback op amps with >100-MHz bandwidth and rail-to-rail performance. They are specified at +3, 5, & ±5 V. Typical performance includes –80 dB distortion @ 1 MHz, output within 0.2 V of rail with 150-Ω load, <5 mA I_{SY} per amplifier. Packages include SOT-23-5 and 8- and 14-lead SOIC & μSOIC. Operation is –40 to +85°C. Prices from <$0.66/channel (quad in 10,000s).

Faxcode 2105 or Circle 37

OP250/OP450 are dual/quad low voltage, single-supply, rail-to-rail, input- and output-op amps with 40-pA bias current, offsets <<10 mV max and open-loop gain of the order of 10^6 V/V. They operate from +2.7 V to 5.5 V supplies, with operation specified at 3 & 5 V. They are available in 8- & 14-lead SOIC & TSSOP, operate from –40°C to +125°C. Price (1000s) $0.50 per channel.

Faxcode* 1950 or Circle 40

Fast FET, Video Quad

AD825: 20-pA I_b, 41-MHz BW
AD8026 quad with fb resistors

The **AD825** is a low-bias-current, wide-bandwidth FET-input op amp, useful as a preamp for high-impedance signals. The wide bandwidth helps to maintain accuracy for lower-frequency applications, e.g., high-gain amplification or low-distortion filtering in the audio band. It is available in 8-lead SOIC for –40 to +85°C, fully specified for ±5-V and ±15-V operation (7.5 mA max). Price in 1000s is $1.65.

Faxcode* 2403 or Circle 39

The **AD8026** is a quad high-speed (135 V/μs, 55-ns settling to 0.1% with 100 pF) op amp with integrated precision input & feedback resistors to meet the accuracy needs of applications such as driving LCD panels for data/video projectors from high-speed DACs. It is specified at ±6 V, for 0 to 70°C, available in 14-lead SOIC. Price is $4.45 (1000).

Faxcode* 2474 or Circle 38

Dual Audio Amplifiers

SSM2275's THD&N: 0.0006%
Rail-to-rail outputs, +5 V, ±15 V

The SSM2275 is a dual low-distortion, rail-to-rail-output audio amplifier that can operate from a single +5-V or from ±15-V rails. It has noise and distortion specs similar to those of the popular OP275, but is available in smaller packages and at lower cost per channel. Its noise is 7 nV/$\sqrt{\text{Hz}}$, THD+N at a low 0.0006% (6 ppm), and gain-bandwidth a generous 8 MHz. Use it for audio amplification and active filtering.

The SSM2275 is designed to be unity-gain stable, with >45° phase margin. It can directly drive capacitive loads of up to 600 pF with no compensation. Its low crosstalk makes it practical for stereo, quad, and six-channel audio applications. It is available for –40 to +85°C operation in 8-pin PDIP, SOIC, and SO-8 MINI (approximately the same footprint as TSSOP, and 1.1-mm thick). Prices (1000s) start at $0.44 per channel.

Faxcode* 2102 or Circle 41

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

New-Product Briefs (For information use reply card or see back cover)

Power-Management ICs & RS-232/RS-485 Transceivers

100 mA anyCAP™ LDO

In SOT23, 0.8% accuracy and 126-mV dropout at 100 mA

The ADP3307 is a high-accuracy anyCAP™ low-dropout regulator with 100-mA output current. It is housed in a SOT23-6 package. Accepting a 3.0 to 12-V supply voltage range, its standard output voltage options are 2.7, 2.85, 2.9, 3.0, 3.2, and 3.3 V. Typical applications are in portable and battery-powered equipment, such as cellular phones, notebook and palmtop computers, camcorders, bar-code scanners, etc.

It is stable with a 0.47-µF capacitor of any type (anyCAP™), regardless of ESR, including MLCC ceramics. This avoids expensive, space-consuming tantalum types. Other features include temperature and current limiting, and low noise. Output voltage is accurate to within ±0.8% at 25°C, and within ±1.4% overall—temperature, line and load. The ADP3307 is designed to operate at ambient temperatures from –20 to +85°C. It is priced at $0.87 (1000s).

Faxcode* 2300 or Circle 42

1-A Switch in SO-8

ADP1073: Step-up or -down Operates from 1-V supply

The ADP1073 is a boost-buck switching regulator that can operate with input supply voltages from 1.0 V to 30 V. This permits operation on single-cell batteries. The ADP1073 can be configured to operate in either step-up or step-down mode (however, the ADP1173 is recommended for inputs >3 V). Standard options are available for fixed (3.3, 5, or 12 V) or adjustable output. Applications include single-cell-to-5-V converters, laptop and palmtop computers, pagers, cameras, battery backup supplies, cellular phones, portable instruments, etc.

The AD1073 family, pin-for pin replacement for the LT1073, uniquely includes a 3.3-V fixed output-voltage option. Requiring few external components, it is housed in 8-lead SO-8 and DIP packages and includes a low-battery detector. Its current limit is user-adjustable. Operating temperature range is 0 to +70°C. Price (1000s) starts at $2.22.

Faxcode* 2450 or Circle 43

Step-Up Regulators

Supply voltages 2–12 V
ADP1109/A replace LT1109/A

The ADP1109 and ADP1109A are step-up switching regulators that operate from input supply voltages of 2 to 12 V and 2 to 9 V. They are similar in many respects, except that the power ground (emitter of the output switch), internally connected in the **ADP1109**, is brought out separately in the **ADP1109A**. Both devices are pin-for-pin replacements for the LT1109 and LT1109A. The Analog Devices ICs are available with variable-output and 3.3-, 5-, and 12-V fixed-output versions.

The 5-V version can deliver 100 mA (3-V input), and the 12-V version can deliver 60 mA (5-V input). Features include logic shutdown to conserve power and 120-kHz oscillator frequency. They are available in plastic DIP and SO-8 packages, for 0 to +70°C operation. ADP1109/09A are priced (1000s) from $2.40/$2.22, respectively.

09: Faxcode* 2018 or Circle 44
09A: Faxcode* 2364 or Circle 45

Step-Down Controller

ADP1147:3.5-16 V input range
3.3 and 5.0-V outputs in SO-8

The ADP1147 is a high-efficiency step-down switching regulator controller. It features an automatic power-saving mode that maintains efficiency at lower input currents. It operates at supply voltages from 3.5 V to 16 V, has greater than 95% efficiency, and is short-circuit protected. Options are currently available for 3.3 V and 5-V outputs, packaged in PDIPs and SO-8. Typical applications are in portable computers, modems, cellular phones, portable equipment, GPS systems, and handheld instruments.

The ADP1147 is a direct pin-for-pin replacement for LT1147. It has logic-controlled shutdown, with low shutdown current, drawing 1.6 mA in normal mode, 160 µA in sleep mode, and 10 µA in shutdown mode. Operating temperature range is 0 to +70°C. Prices (PDIP & SO-8) are $2.75 & $2.90 (1000s).

Faxcode* 2022 or Circle 46

Regulator Controller

for Pentium II power supplies
ADP3152: integrated crowbar

The ADP3152 is a high-efficiency synchronous switching controller optimized for Pentium II processor applications in desktop PC power supplies, where 5 V is stepped down to a digitally controlled output voltage between 1.8 V and 3.5 V. Using a 5-bit DAC to read a voltage-ID code directly from the processor, the ADP3152 uses a current-mode constant-off-time architecture to generate its precise output voltage (and provide adjustable current limiting and short-circuit protection). It drives two N-channel MOSFETs in a synchronous-rectifier buck converter, at frequencies <250 kHz. With the recommended compensation and guidelines, the dc-dc converter circuit meets Intel's stringent transient specs with few capacitors and smallest footprint.

The ADP3152, with 12-V supply, in a 16-lead SOIC, operates from 0 to +70°C. Price in 1000s: $2.14.

Faxcode* 2422 or Circle 47

232/485 Transceivers

3-V, 2-channel RS-232
3-V full-duplex RS-485

The **ADM3202**, **ADM3222**, **ADM1385** are 3-V variations of the popular ADM202 2-channel transceiver. Connected to the UART, it translates between full RS-232 levels (±5 V) and TTL, using an internal charge pump based on 3 V to obtain the required voltages. They are used in mobile phones, digital still cameras, PDAs, and "mobile anything." They are variously available in DIP, SOIC, SSOP, TSSOP, for –40 to +85°C. Price is $1.35 (1000s).

Faxcode* 2146 or Circle 48

The **ADM3491**, a 3-V full-duplex RS-485 transceiver, sits between the serial comms controller and the RS-485 connector, and converts between TTL and RS-485 levels. Uses are in motor control, numeric control, as low-cost multidrop connector, intercard connection in telecommunications systems. Available in DIP, SOIC, TSSOP for –40 to +85°C. Price is $1.35 (1000s).

Faxcode* 2424 or Circle 49

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Switches, Video Encoders, Fast 12-Bit ADCs

Video Crosspoints

AD8108/8109 8×8, G=+1/+2
AD8110/8111 16×8, G=+1/+2

These newest variants of the EDN prize-winning AD8116 (16×16: *Analog Dialogue* 31-2, page 6) are used to route high-speed signals from any inputs to any outputs via an array of internal switch points programmed by a serial or parallel word. Many types of analog and digital signals can be routed, including compressed or uncompressed composite or component video signals in a variety of applications, such as broadcast video and video-on-demand. An evaluation board is available.

Pin-compatible (80-lead TQFP), they are characterized by high speed (200 MHz), excellent differential gain and phase (0.02%, 0.02°), 60-MHz 0.1-dB gain flatness, and require no external buffers to drive video loads. Operation is from –40 to +85°C. Prices (1000s) are $22 and $37.50 for AD8108/09 and AD8110/11, respectively. **Faxcode* 2191 or Circle 50** (8×8) and **Faxcode* 2436 or Circle 51** (16×8)

Fast Switch Family

Low voltage, high performance
SOT-23 and µSOIC Packages

The ADG7xx family of switches operate from a single supply of 1.8 to 5.5 V and have R_{ON} of less than 5 Ω. Fabricated on a 0.6-µm CMOS process, they have a signal bandwidth >200 MHz and can switch on in less than 20 ns. Leakage is only 350 pA (max) over temperature. The parts are packaged in the smallest packages available including 6-lead SOT-23 and 8-lead µSOIC. Currently released are ADG719 (single SPDT), ADG701/02 (single SPST), and ADG721/22/23 (dual SPST)—with a quad SPST, dual SPDT and 4:1 mux to follow.

Low R_{ON} Switches

4-Ω Switches Cut Distortion
Suitable Relay Replacement

The ADG451/2/3 (quad SPST) are the lowest on-resistance 15-volt switches in the market place today. Specified with dual supplies of ±15 volts or a single supply of +12 volts, these parts have only 4-ohm on-resistance, with 0.2-ohm flatness, resulting in greatly reduced distortion. In addition, the parts can carry 100 mA continuously in the on condition. With their low on-resistance, this makes them a suitable replacement for relays in many applications. They are available in 16-lead SOIC and DIP packages.

	ADG719	ADG701/02	ADG721/22/23	ADG451/52/53
Type	1 × SPDT	1 × SPST	2 × SPST	4 × SPST
Supply specs	+5 V, +3 V	+5 V, +3 V	+5 V, +3 V	±15 V, +12 V, ±5 V
R_{ON}	4 Ω	3 Ω	4 Ω	4 Ω
Packages	µSO, SOT-23	µSO, SOT-23	µSOIC	PDIP, SOIC
Faxcode	**2411**	**2410**	**2412**	**2196**
Circle	**54**	**52**	**53**	**55**
Price (1000)	$0.55	$0.51	$0.62	$1.95

10-Bit Video Encoder

Converts YCrCb to NTSC/PAL
ADV717x: SSAF™ Technology

The ADV7170 & ADV7171 interface digital video systems (DVD, set-top boxes, PCs, digital cameras) to standard analog TVs and VCRs. New super sub-alias filter (SSAF™) technology has resulted in industry-leading "professional studio" video quality with smart power management for mobile PCs and battery-powered applications (100 nA in power-down). Features include multi-standard switchable 4-DAC video output, SCART, S-Video, component (YUV) video, composite video, WSS, & CGMS-A.

They interface gluelessly to MPEG I & MPEG II video decoders. They differ only in that ADV7170 supports Macrovision Anti-Taping, Rev. 7.01. Sleep-mode current is <1.0 µA. They are specified for 3.3- and 5-volt single supplies and are housed in 44-lead PQFP and TQFP packages, for 0 to +70°C. An evaluation board is available. Device prices (10,000) start at $4.50. **Faxcode* 2428 or Circle 56**

RGB to NTSC/PAL

AD725 analog encoder
Includes luminance trap port

The AD725 is a very low cost general-purpose RGB to NTSC/PAL encoder; it converts red-green-blue color component signals to corresponding luminance and chrominance values in accordance with either NTSC or PAL standards. The outputs are also combined on-chip to provide a composite video output. All three outputs are available at twice the standard voltage level for convenience in driving 75-Ω reverse-terminated cables. Applications include computers, games, digital cameras.

Included is a luminance trap (YTRAP) pin to provide a means of reducing luminance-associated cross color. The device is 5-V single-supply operated and can be powered down to less than 1 µA of current consumption; TTL-compatible logic levels can support logic requirements of 3-V CMOS systems. The device is packaged in 16-lead SOIC Price (1000s) is $4.25.
Faxcode* 2302 or Circle 57

12-Bit, 40/25 MSPS

CMOS ADCs in SOIC & SSOP
5-V supply; support 3-V logic

The AD9224 and AD9225 are 12-bit, 40- and 25 MSPS complete A/D converters. They are pin-compatible upgrades of the AD922x series with sample rates from 1.25 to 10 MSPS. They offer price and performance advantages in new and emerging applications in communications, medical imaging, ultrasound, instrumentation, scanners, and signal-capture.

Features of the AD9224/25 include SFDRs of 75/85-dB, SINAD of 67.5/70.5 dB, SNR of 69.1/71 dB, low power dissipation (376/280 mW), differential inputs, wide input bandwidth (120/105 MHz), 10.9/11.4 ENOB (effective number of bits), and 12-bit no-missing-codes. They are housed in 28-pin SOIC and SSOP packages, and are specified for operation from 0 to +70°C (AD9224) and –40 to +85°C (AD9225). Prices (1000s) are $18.66 and $15.35.
AD9224: **Faxcode* 2165 or Circle 58**
AD9225: **Faxcode* 2166 or Circle 59**

*For immediate data, visit our **WorldWide Web** site: **http://www.analog.com.** In North America, call ADI's 24-hour AnalogFax™ line, **1 (800) 446-6212** and use **Faxcode.**

Magnetic Sensor, Digital Isolator, Log Amp, etc.

Magnetic Field Sensor

Hall & IC practice combine in linear & stable AD22151

The AD22151 is a monolithic integrated circuit in an 8-lead SOIC package that outputs an analog voltage proportional to magnetic field strength perpendicular to the plane of the package (positive top-to-bottom). The Hall-effect sensor is centrally located, with an area of approximately 0.25 mm^2. The device operates over a range of –40 to +150°C, with nominal sensitivity of 0.4 mV/gauss, offset error of ±6 gauss over temperature, and 1% gain error over temperature. Offset and gain are adjustable, and first-order temperature compensation can be adjusted to adapt to commonly used magnetic materials. The output is ratiometric with supply voltage.

Principal applications are in automotive and industrial settings, mainly for position sensing of such elements as throttles, pedals, valves, and suspensions. Nominal supply voltage is +5 V. Price is <$5.

Faxcode* 2240 or Circle 60

5-Line Digital Isolator

Isolates dc-20-MHz 5-V logic AD261 has 3.5-kV rms barrier

The AD261 isolates 5 microcontroller input or output signal lines from 5 field or system destinations with common supplies. The six optional versions of the device establish the channel mix, i.e., how many of the lines are inputs and how many are outputs. Although designed to isolate µPs from ADCs and DACs, the AD261 can be used for isolating just about any 5-V logic signal from dc to 20 MHz. Current consumption (both sides—system and field) ranges from ≤8 mA at ≤1 MHz to 26 mA at 20 MHz.

Typical applications are in process control, factory automation, motor drives, utility monitoring, etc. The device has UL1950, IEC950, and EN60950 certification, and VDE and CE are pending. It is housed in a 22-pin plastic DIP, and requires isolated +5-V supplies for input and output circuitry. It is available in 1.75 & 3.5 kV rms versions, priced at $9.60 & $11.30 (1000). **Faxcode 2161 or Circle 61**

Demodulating Logamp

AD8307: 500 MHz BW, ±1-dB accuracy, 92-dB dyn. range

The AD8307 is a high-speed logarithmic amplifier designed to convert high-frequency signals (20 Hz to 500 MHz) into their demodulated low-frequency (dc) equivalents. The output is proportional to the logarithm of the input voltage or power. Typical applications are in determining the strength of wide-dynamic-range rf signals (i.e., received signal strength indication—RSSI), and in wide-dynamic-range rf power control, especially for cellular/PCS base stations. It is also useful in converting rf signal levels to true decibels in network and spectrum analyzers.

Available in 8-pin PDIP or SOIC, it is temperature stable, easy to use, and operates on +3 to +5-V supplies. It is accurate to within ±1 dB, and it handles signals with dynamic ranges of up to 92 dB. An evaluation board is available. The device's price in 1000s is $5.25.

Faxcode* 2098 or Circle 62

Digital Potentiometer

AD7376 has 128 levels Replaces pots and trimmers

The AD7376 is a single-channel, 128-position digitally controlled potentiometer, available in resistance values of 10 kΩ, 50 kΩ, 100 kΩ and 1 MΩ. Complementing our line of low-voltage AD840x digital pots, the AD7376 operates with single (+5 to +28 V) or dual (±5 V to ±15 V) supplies. Replacing pots and trimmers in new analog circuit designs, a few typical applications include delays, programmable filters, time-constant setting, volume controls, panning, line impedance adjustment, and gain and offset adjustment.

The potentiometer setting is established via an SPI-compatible 3-wire serial interface. Settling time is 4 µs and THD is 0.005%. Power dissipation is 30 mW max. The AD7376 is available in 14-lead PDIP and TSSOP, as well as 16-lead widebody SO packages for operation from –40 to +85°C. Price (1000s) is $2.57. **Faxcode* 2111 or Circle 63**

Radio on a Chip

Complete 900-MHz transceiver Includes transmit, receive, LO

The AD6190 is a complete RF/IF transceiver for use in 900-MHz spread-spectrum wireless systems. A big leap forward in high-integration RF chips, it is a real "radio-on-a-chip" device, including transmit, receive, and local oscillator functions. It is designed for use in conjunction with the Zilog Zphone baseband digital processor (or equivalent). With a processor and a few additional low-cost components and filters, it forms the basis of a high-performance, low-cost spread-spectrum cordless telephone (reference design available).

The AD6190 is designed for operation within a battery voltage range of 3.0 to 4.6 V and is specified at 3.3 V. It typically draws 93 mA in Transmit, 59 mA in Receive, and 270 µA in Sleep mode. Housed in SSOP-28, its operating temperature range is –25 to +85°C. Price in very large quantity is well below $5.00. **Faxcode* 2231 or Circle 64**

ADSL Chip Set

Complete standard-compliant modem solution

These are the parts of the **AD20msp910** ADSL modem chip set:—an easy-to-use chipset that meets industry standards, including ANSI T1.413, ETSI TR328, and ITU G.dmt and G.lite.

The AD6435 is the interface/framer that connects the chipset to the rest of the system. It buffers the data, formats and frames it to the ADSL standard and also performs FEC. The AD6436 is the "engine" of the DMT chipset. It takes clean data from the AD6435 and does all of the digital modulation/demodulation, signal processing, equalizing, filtering, and related tasks. The AD6437, the codec, or mixed-signal stage in the ADSL chipset, includes 12-bit Tx & Rx signal paths, with 70-dB performance and sampling rates that support multi-MHz bandwidths or oversampling. This part can be used separately as a general-purpose codec.

Circle 65

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Worth Reading

DESIGNER'S CD REFERENCE MANUAL

The 1998 edition of the Designers' CD Reference Manual contains PDF data sheets and other information on about 1300 models covering all aspects of analog signal processing from dc to rf, as well as information on our digital signal-processing (DSP) product line. In addition to a three-way product-selection search engine, the manual includes application notes, SPICE models, a Worldwide Sales Directory, and a cross-reference guide to competitive equivalents. In addition, products designed for low-voltage operation (+3 V) or low physical profile (1.78-mm max height) can be searched for independently, without requiring a search of the entire database. Designed principally for PCs, it can also be used, with some limitations, in a Mac or Unix environment. **Circle 68**

SHORT-FORM DESIGNER'S GUIDE

The 1998 Short-Form Designer's Guide has 312 pages of information on Analog Devices products and applications. Included are Selection Trees and Selection Guides for 21 classes of products from amplifiers and converters to sensors and signal conditioners to digital signal processors. Especially highlighted are more than 27 pages of New Products and 23 pages of New-Product Application Ideas, plus 8 pages of listings of Evaluation Boards. Also included are ordering guide, package options, Worldwide Sales Directory, Technical Publications, including 4 pages listing our Application Notes. **FREE. Circle 69**

SERIAL PUBLICATIONS

DSPatch—The digital signal-processing applications newsletter. No. 39, Spring, 1998, 20 pages**.** This issue introduces the 3.3-V ADSP-2183, the world's smallest (1 cm^2) DSP package; Also featured: DSPs as systems-on-a-chip; the low-cost SHARC: ADSP-21065L; Single-chip RAS modem; Designing low-voltage systems; Using SHARCs: in weather tracking, in reconfigurable audio, in radar processing, in voice processing. In addition, departments such as Q&A, news of workshops and software releases. **FREE**. **Circle 70**

Communications Direct—System-level IC solutions for digital communications. Vol. 3, No. 2, 8 pages. Features: New chips optimize GSM baseband mixed-signal processing; Digital receiver design considerations; Single-chip radio cuts cordless costs. Also, an opinion piece: Personal communications systems; the design challenge; and brief articles: ADI makes custom DSPs for 3Com's 56-K modems; an overview of the AD20msp415 GSM baseband chipset. **Circle 71**

Accelerometer News. Issue 6, 8 pages. Features: Accelerometers in earthquake detection systems; Repackagers provide cost-effective turn-key solutions to many accelerometer applications; An inertial brake light system. Also, The signature verification system (using an accelerometer-based pen and a hidden Markov model); and ADXL05 prices reduced. **Circle 72**

*For copies of any of these publications, use the reply card, or get in touch with Literature Distribution (see page 24).

BROCHURE

The anyCAP™ family of low-dropout regulators—More power to the portable world, 4 pages. Lists low-dropout regulators, battery chargers, switching regulators, and charge pumps. Describes the patented anyCAP™ principle and product line, as well as the patented dissipation-facilitating Thermal Coastline package. **Circle 73**

A FREQUENTLY ASKED QUESTION

To Richard J. Higgins, Director,
Global Innovation for Engineers Program
http://www.ece.gatech.edu/academic/gie

Dear Mr. Higgins,
I am a Masters student at Macquarie University, Sydney, Australia and have been using your book *Digital Signal Processing in VLSI** for study. Most book stores (for example amazon.com) state that the book is out of print. Can you tell me whether a new edition is in the cards? It is an excellent DSP text—you seem to have captured the flair of DSP rather than just all the mathematics!

Best Regards,

Michael Goorevich

michaelg@iceberg.mpce.mq.edu.au

Thanks for your kind words. We worked pretty hard at it . . . By copy of your note to Dan Sheingold at Analog Devices, with whom this book was written, I am alerting him to the status of DSP in VLSI being out of print . . . (He) may be able to update you on any plans underway.

Richard Higgins

Dear Michael:
It's out of print at Prentice Hall, but we still have copies of it at Analog Devices and continue to distribute them. We haven't yet determined whether to order another printing after it runs out this time. Certainly, none of the fundamentals have changed, and 6 of its 8 chapters still provide an excellent basis for understanding the underlying philosophy, physics, and mathematics of DSP, regardless of the hardware/software of specific implementations. The principal changes to be made would be in this latter area, but the field is so fast-moving that whatever we published in a new edition would again be obsolete within a short time.

Also, the specific architectural implementations of Analog Devices and our competitors get increasingly integrated (XLSI?) and depart more and more from the recognizable basic elements found in the simple structure and instruction set of the ADSP-2100. Nevertheless, the next generation of floating-point SHARCs uses essentially the same instruction set as the first generation of SHARCs, and the SHARC instruction set is recognizably related to that of the fixed-point 2100, described in the book.

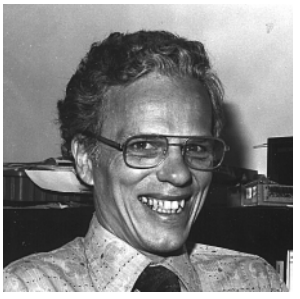
Once you've gotten what you need to know from this advanced primer, the sensible next steps are to collections of algorithms specifically relating to solving problems of interest to you, and to the instructional materials of your chosen manufacturer.

Dan Sheingold

*Higgins, Richard J., *Digital Signal Processing in VLSI*. Englewood Cliffs, NJ: Prentice Hall, ISBN 0-13-212887-X. ©1990 by Analog Devices, Inc. Available from ADI ($38.00)—see book card at page 13, or Literature Support, page 24.

Editor's Notes [*Continued from page 2*]

FRANK GOODENOUGH—IN MEMORIAM



Last December, at 72, Frank Goodenough finally succumbed after a long and courageous fight against cancer. At the time, he was *Electronic Design*'s Analog and Power Technology Editor. For nearly two decades, he reported to *Electronic Design*'s readers on just about everything new and important in analog circuit progress. In the two to three years just before he joined *ED*, we had the good fortune to get to know Frank as a colleague at Analog Devices and a regular contributor to these pages. We knew him to be articulate, fearless, innovative, enthusiastic, lively, and intellectually omnivorous. He had a hunger for new ideas, and a passion to find new ways to apply them. With Frank, there was always something interesting to talk about, never a dull moment.

We were fortunate that his new calling, as an ED editor, kept him in touch with us, and we were glad to see him on his occasional visits to our facility. His colleague at *Electronic Design*, Roger Allan, wrote a beautiful farewell tribute (March 9, 1998 issue) so accurate that reading it virtually brings him to life in our minds. We were glad to have known him and to have had a part in the preparation for his ED career—the culmination of the colorful and varied panoply of experiences that shaped a truly unique person.

Dan Sheingold

ANALOG DEVICES WEB SITE UPDATE *www.analog.com*

From Application Notes to comprehensive industry overviews, visitors to ADI's homepage can acquire information far beyond simple product search and selection. Here are some of the more recent enrichments to the site. Why not bookmark them? They will offer frequently updated information:

Design Support
http://www.analog.com/support/Design_Support.html
Organized by product group, the Design Support Center offers FAQs, technical articles and applications notes, software libraries, SPICE models, Selection Tables, whitepapers, & more. It also offers you the opportunity to request assistance from our experienced Applications Engineering group using available phone numbers—or with a handy e-mail form.

Industry Solutions
http://www.analog.com/industry/Industry_Solutions.html
The Industry Solutions area gives designers and engineering managers information about important new products of special interest for specific markets, technologies and applications.

Topics covered by the comprehensive overviews include:

- Accelerometers / iMEMS®
- Digital Signal Processing (DSP)
- IOS: I/O Subsystems
- Military / Aerospace
- Motor Control
- PC Pavilion
- Products for Industrial Apps
- RAS Modem
- Signal Chain℠ Diagrams

Product Center gives you easy access to samples!
Samples can be ordered online. Many products are available for sampling; more are added every day. Visit the Product Center:
http://www.analog.com/product/Product_Center.html
for full details on this latest development and to register as a user.

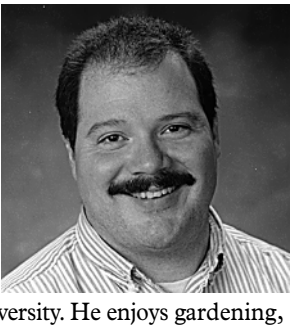
Alice Petrescu

THE AUTHORS

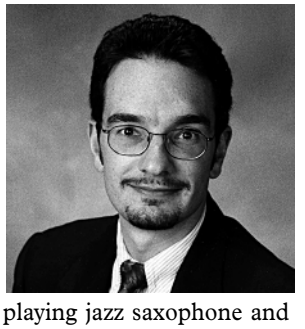
Roya Nasraty (page 3) works as an Applications Engineer at ADI's Thermal Management and Voltage Reference product line in Santa Clara, CA. Roya holds a BSEE from San Jose State University. She joined ADI in 1995, working in Central Applications, and then moved to the TMP/REF product line. In her spare time, Roya enjoys reading and listening to classical music.

Troy Murphy (page 5) is the applications engineer for ADI's Precision Amplifier and Analog Audio group in Santa Clara, CA. He was graduated with a Bachelor of Music Engineering degree from the University of Miami in 1992 and received an MS from Georgia Tech in 1995. He joined Analog Devices in early 1996. An accomplished saxophone player, he is also a proficient juggler—and is currently working on a way to do both simultaneously.

Erik Barnes (page 6) is an Applications Engineer for ADI's High-Speed Converter group in Wilmington, MA, specializing in imaging systems. After receiving a BSEE from Tufts University, he joined ADI, working in Central Applications in support of amplifier and converter products. In his free time, Erik enjoys building loudspeakers, playing the guitar, and listening to live- and recorded music.



David Skolnick (page 9) is a Technical Writer with ADI's Computer Products division, Norwood, MA, where he writes and illustrates manuals and data sheets and has written or edited a number of DSP Application Notes. He holds a Bachelor degree in Electrical Engineering Technology and a Master of Technical and Professional Writing degree from Northeastern University. He enjoys gardening, outdoor sports, and anything to do with his family.



Noam Levine (page) is a Product Manager in the 16-bit DSP product line, working on new-product definitions and fixed-point DSP applications. He holds a BSEE from Boston University and an MSEE in DSP from Northeastern University. He has authored several application notes, technical articles, and conference papers. When not in the digital domain, Noam can be found playing jazz saxophone and working on his SCCA competition driving license.

Cover: The cover illustration was designed and executed by **Shelley Miles**, of ***Design Encounters***, Hingham MA.

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•Low-dropout 20-A regulator/controller in 8-pin SO, *ADP3310*
•96-kHz stereo DAC, 113-dB SNR, –97 dB THD+N, *AD1855*

ERRATA • • • **AD53040 data sheet**: Bypass capacitors should be connected between VEE & VLDCPL and VCC & VHDCPL. Keep lead lengths as short as possible • • • **AD7304/AD7305 data sheet, Rev. 0:** Pin 4 should be VREFA, pin 5 is VREFB (corrected in Rev A).

PRODUCT NOTES • • • **AD7714** has a –40 to +105°C "Y" grade with improved specs, including 0.001% max INL, Schmitt trigger inputs, 3-5-V supply range, 2.7 V min operating voltage (<1 mW), 24-lead TSSOP, and *lower price* • • • **AD7715** is now available in tiny TSSOP 16-pin packages • • • The **AD976** 16-bit sampling ADC has had substantial price reductions, which include availability in a very low price "C" grade • • • The **AD620**, **AD622**, and **AD623** Instrumentation Amplifiers now have reduced sensitivity to temperature. The gain/temperature spec is 10 ppm/°C at G = 1 • • • The AD422 HART system on a chip mentioned in Analog Dialogue 31-1, page 15, is not (and will not be) available.

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