Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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ANALOG DEVICES

Editor's Notes

NEW FELLOW

We are pleased to note that Scott Wurcer was introduced as the newest Analog Devices Fellow, the highest level of achievement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their creative technical contributions in product or process technology will have led to commercial success with a major impact on the "bottom line."

Their attributes include roles as mentor, consultant, entrepreneur, organizational bridge, teacher, and ambassador. They must also be effective leaders and members of teams and in perceiving customer needs. Scott's technical abilities, accomplishments, and personal qualities well-qualify him to join Fellows Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980) Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Doug Mercer (1995), Mohammad Nasser (1993), Wyn Palmer (1991), Richie Payne (1994), Carl Roberts (1992), Paul Ruggerio (1994), Brad Scharf (1993), Mike Timko (1982), Bob Tsang and Mike Tuthill (1988), and Jim Wilson (1993).

SCOTT WURCER

Scott's first major product design was the AD524 instrumentation amplifier (*Analog Dialogue* 16-3, 1982), the first IC in-amp to use current feedback; it also used JFET input protection, and its distortion was below 10 ppm. It was reported on at the IEEE Solid-State Circuits Conference and quickly became an industry standard. It was the first of a family of in amps that made ADI a leader in the field.

Other important and innovative op amp designs, some involving patents, include: the AD712 BiFET (FETs trimmed for ac & dc performance to be independent of temperature and manufacturing variations); the low-noise AD797, fabricated on a complementary bipolar (CB) process and using a patented distortion-nulling process for low audio distortion; and the 800-MHz, 5-mA AD8001 (XFCB process). More recent innovations, in ADSL and 16×16 video crosspoint switching, will soon make their mark.

Besides contributing handsomely to Analog's product mix (and bottom line), Scott, in a quiet way, demonstrates the qualities of technical leadership that we expect of a Fellow: as *consultant*, whose advice on low distortion circuits is continually sought; as a *spokesman* for ADI at technical conferences; as an effective *teacher* who has contributed behind-the-scenes to building and sustaining our core competence in linear design; and as a *team player* highly regarded by colleagues for pursuit of team goals.

Scott is a member of IEEE and AES. A native of Milwaukee, he went to MIT, working in X-Ray astronomy in the Center for Space Research. Joining ADI after graduation, as a product test engineer, he later became an IC circuit designer. His recreational interests include cooking, carpentry, and non-commercial music.

Dan.Sheingold@Analog.Com

AUTHORS

Aengus Murray (p. 3), of ADI's Transportation & Industrial Products Division, in Wilmington MA, leads the Motion-Control Group's Systems Engineering team. He has a BE (Elec.) and a Ph.D. degree from University College, Dublin, with a specialism in ac motor control. He continued his work on brushless systems at Kollmorgen, Ireland, Ltd., later became a Senior Lecturer and Director of the Power Electronics Research Laboratory at Dublin City University. In his spare time, he enjoys skiing and sailing.

John McDonald (p. 10) was a Senior Applications Engineer at Analog Devices, Santa Clara. His responsibilities included publication of design ideas, techniques, and applications, and developing SPICE models. John holds a BSEE from the University of Washington; he joined ADI in 1994 after working in neuro-physiological equipment design; he left ADI recently. In his spare time, he enjoys basketball and entertaining his children.

Pete Predella (p. 12) is a Marketing Communications Manager at Analog Devices in Wilmington MA. Since joining ADI, in 1979, he has been a Technician for the Component Test Systems and Motion-Control divisions. Peter is a graduate of GTE Sylvania Technical School and is currently pursuing a BSET from Northeastern University. His interests include reading, salt-water fishing, and golf.

Steve Guinta (p. 18) is the Technical Training Manager for ADI's Central Applications group in Wilmington MA. He is responsible for developing and managing training programs for ADI's Sales and Field Applications Engineers worldwide. Steve joined ADI in 1981 after serving for 15 years as an Applications Engineer with Cambridge-based test-equipment manufacturer, Krohn-Hite Corp. Steve holds a BSEE from Northeastern University.

[more authors on page 22]

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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Motion-Control Chip Sets

DSP and motor-control chips simplify DSP-based AC motor control hardware

by Aengus Murray

Variable-speed motor control systems have a wide range of applications, from high-end industrial robotics to ordinary home appliances, such as domestic washing machines. The control loops in these systems were first implemented using analog components. Typically, op amps were used in the feedback compensation circuits, and comparators were used to generate the control signals for the switching power converter. However, the advent of low cost microcomputers has increasingly led to the implementation of the control and user interface functions by digital means. The continuing reduction in the cost of processing power has made it possible to simplify the system hardware even further by implementing all the motor control functions on the same processor.

The Analog Devices Motion Control Group has been the leading supplier of resolver-to-digital conversion products to the ac servo motor market for the last ten years. Devices such as the AD2S80 and AD2S90 R/D converters are used to process the analog feedback signals for digital control of position and velocity in permanent-magnet ac servo drive systems. The latest offerings from the Motion Control Group, the ADMC200 and ADMC201 motion coprocessors, carry this concept farther. These multi-function devices combine, on a single chip, all the interface and signal-processing functions required to provide feedback-controlled current for ac motor control.

The ADMC201 provides the analog acquisition system to capture the motor current or voltage signals, the vector processing functions which condition these signals, and the pulse width modulator required to control the power converter. The ADMC201, combined with the ADSP-2105 digital signal processor, functions as a high performance control engine for ac motor drive systems. The following example describes the principal device features and their use in a motor-control application.

AC servo motor control system: A servo motor control system typically has two cascaded control loops, as shown in Figure 1. The *outer* motion loop controls the motor position and velocity based on feedback signals from a position or velocity sensor. The output of this loop is a demand for an increase or decrease in motor torque, which is fed to the *inner* current loop. The current loop generates signals for the power converter which supplies suitable motor currents to produce the desired output torque. The power flow from the dc supply rail to the motor is controlled by rapidly varying the on and off conduction periods of power semiconductor switches such as IGBTs or power MOSFETs. These control signals are typically fixed-frequency, variable duty-cycle waveforms that can be produced digitally using timing circuits.

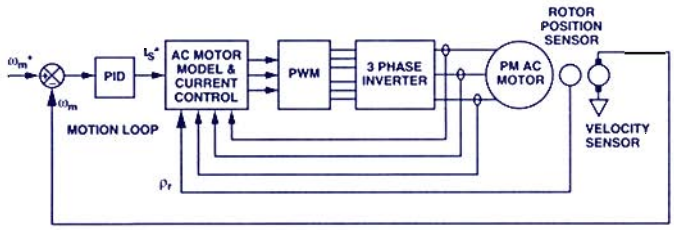


Figure 1. Servo-motor control system.

In general, the motion loop design is independent of the motor type (ac or dc) but is solely a function of the mechanical properties of the system such as inertia, dynamic friction, etc. However, the current loop varies very much in sophistication depending on the motor type. In dc motors the torque is directly proportional to the dc current in the armature windings. But to control the torque in ac motors, the currents must be synchronized to the position of the rotating rotor field. One way to simplify the control of the motor torque is to transform the measured stator currents to a reference frame synchronized to the rotor field. This process (Figure 2) results in two equivalent dc motor current quantities: a torque-producing component, I_q, and a field-control component, I_d. The ac motor control system calculates the two quadrature voltages, V_d and V_q, required to force the I_q current to directly follow the torque demand and the I_d current to maintain a constant rotor field. An inverse transformation is then used to transform the "dc-motor" V_d and V_q voltages back to the stator reference frame to give the required winding voltages.

Figure 3 shows an all-digital implementation of a control scheme for a permanent magnet ac servo motor. A resolver-to-digital (R/D) converter derives digital angular position feedback information from the output signals of a shaft-mounted resolver. The outer position and velocity loop calculates the required motor torque current, I_q*. Motor velocity is calculated from position measurements, using an estimation algorithm. The field-reduction component, I_d, is normally zero so as to maximize the motor torque output. However, the field weakening function can set a non zero I_d* to effectively reduce the rotor field strength, thus increasing the motor speed range.

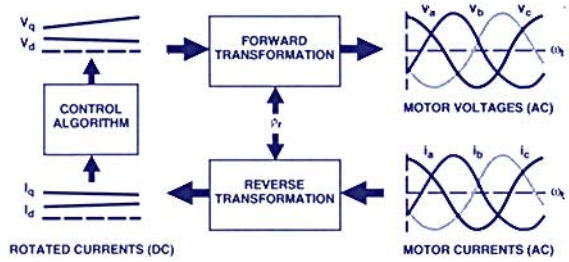


Figure 2. Vector-rotation function.

IN THIS ISSUE

Volume 30, Number 2, 1996, 24 Pages

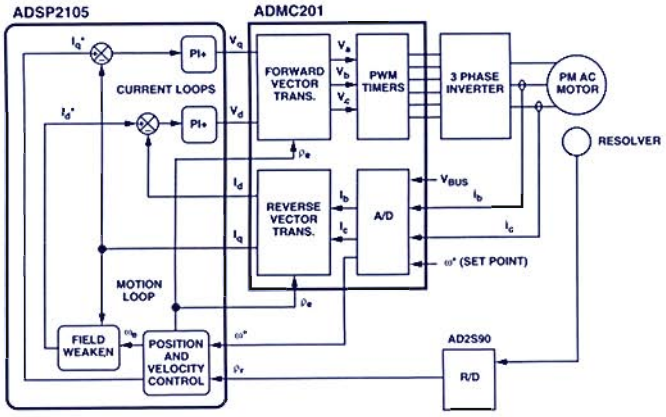


Figure 3. Control system for AC motor.

An A/D converter conditions the motor's stator current measurements, which are passed on as an input to the vector transformation. The reverse transformation takes two stator current signals—and the rotor electrical angle, ρ—and calculates the torque and field components, I_q and I_d. The third stator current signal is inferred, since all three stator currents sum to zero. There are two current loops, a torque loop and a field loop, with proportional and integral compensation (PI). The response of these loops can be improved by feeding forward the estimated winding back-emf and winding-impedance drops (hence the '+' annotation). The V_d and V_q outputs of the calculation are then transformed in the vector-transformation block to digital equivalents of the three-phase stator voltages, V_a, V_b and V_c, for driving the motor.

The PWM timer block converts the digital inputs to pulse width modulated timing signals for the three phase inverter. The voltage applied to the motor windings is controlled by the conduction times of power transistor switches in each inverter leg. In the example below (Figure 4), when the upper inverter power transistor, Q_A, is turned on, winding "a" is connected to the +V bus power rail causing the winding current, i_a, to increase. When Q_A is turned off the winding current "free wheels" through lower inverter diode, D_{AP}, and connects the winding "a" to the -V bus power rail. The average stator winding voltage, V_A, is proportional to the conduction period, t_A, of power transistor, Q_A, and is given by:

$$V_a = \frac{(+V_{bus}) \times t_A + (-V_{bus}) \times (T - t_A)}{T} = V_{bus} \times \left(\frac{t_A - \frac{T}{2}}{\frac{T}{2}} \right) \qquad \text{Eq. 1}$$

For negative stator currents, the winding current flows through lower transistor Q_{AP} and "free wheels" through upper diode D_A. In this case, the winding voltage is a function of the conduction

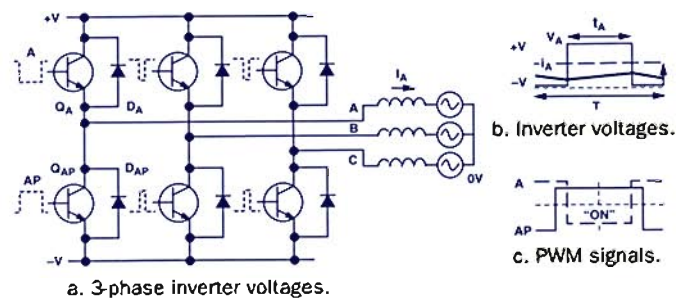


Figure 4. Three-phase inverter operation.

period of the diode D_A. In order to make the applied stator voltage independent of the stator current sense, the power transistor, Q_{AP}, is turned on when Q_A is turned off. However, to prevent the possibility of simultaneous conduction of these power transistors a brief "dead time" is inserted between the *on* signals for the upper and lower devices. The resultant active low PWM signals, shown in figure 4 (c), are complementary timing wave forms with a short "dead" time between the active portions.

The ac servo system described above can be built using three principal control components. The ADSP-2105 DSP implements the control loops, the ADMC201 interfaces to the three-phase inverter, and the AD2S90 interfaces to the resolver position sensor. The ADSP-2105 fixed point DSP has been optimized for high speed signal processing applications. It is very suitable for ac motor current control because of the short control loop cycle times—of the order of 50-100 µs. The AD2S90 resolver-to-digital converter can be simply interfaced to the DSP using the serial port. [If the ADSP-2115 is used, it makes available an additional serial port.]. A companion oscillator IC, the AD2S99, is used for resolver excitation and provides loss-of-signal detection.

The ADMC201 provides the required interface functions between a DSP controller and the three phase inverter; it is suitable for use in controlling both permanent-magnet ac motors and ac induction motors. A detailed description of the ADMC201 and the interface to the ADSP-2105 follows.

The ADMC200 Motion Coprocessor family: The ADMC200 motion coprocessor has three principal functional blocks: a 4-channel, 11-bit, simultaneous-sampling A/D conversion system, a 12-bit zero-centered PWM timer block, and a vector-rotation block. The ADMC201 provides, in addition, three additional analog input channels and 6 bits of programmable digital I/O pins. The device has 25 internal memory-mapped registers for storing the peripheral input and output data. An embedded control sequencer decodes the chip-select line, Read- and Write lines, and 4 address lines—and maps these data registers directly into the DSP memory address space. This means that *all registers are directly accessible to the DSP at all times*. An on-chip Interrupt controller can interrupt the DSP at the end of an A/D conversion sequence or on completion of a vector transformation. The A/D converter's Start-of-Conversion line can be driven by the PWM timer block, to synchronize the control software and signal sampling to PWM frequency.

The ADMC200, designed on a CMOS process, combines low cost and low power consumption. The A/D converter, based on a CMOS-compatible switched-capacitor technique, is an 11-bit successive approximation device with a 4-channel simultaneous-sampling track-and-hold amplifier as its front end. This allows up to four motor current or voltage signals to be acquired without "skew" in less than 14.4 µs. The ADMC201 has an internal 4:1 multiplexer, which provides an additional three asynchronous channels for slower signals, such as temperature or dc bus voltage. The converted values are in a twos-complement format to match the fixed-point DSP processor. The analog input range is 0 to 5 V, with 2.5 V equivalent to digital zero. The on-board reference has an absolute accuracy to within 5% (fully loaded). The overall accuracy of the analog to digital converter is 8 LSBs, while the channel to channel match is to within ±2 LSB. A high Start-of-Conversion pulse acquires all four input channels and starts a conversion sequence for 2, 3 or 4 channels, depending on the

control-register settings. The end of conversion can be programmed to generate an interrupt pulse for the DSP, which can read the results registers in any order.

The 12 bit PWM block produces three pairs of constant-frequency variable-duty-cycle wave forms for the power converter switches, with a frequency ranging from 1.5 kHz to 25 kHz. The signals, described in Figure 5, are center based active-low signals so that the On (low) periods are symmetrical about the midpoint between timing pulses. This makes it easier to synchronize the current-sampling with the PWM wave forms. The wave forms are complemented, i.e., the power devices are switched in pairs: one device "on", the complementary device "off". To prevent the possibility of simultaneous conduction in the inverter power devices, complementary PWM wave forms are dead time adjusted (PWMDT). An active high PWMSYNC pulse, produced at the beginning of each PWM cycle, synchronizes the operation of the power inverter with the A/D converter.

The 12 bit hardware vector-rotation blocks can perform both forward- and reverse Park- and Clarke transformations between the stator (ac currents and voltages) and the rotor (dc machine equivalent) reference frames. The reverse transformation converts three-phase stator currents signals, I_a, I_b and I_c, to two orthogonal rotor referenced currents, I_d and I_q. The transformation consists of three stages (Table 1), where ρ is the angle of the rotor field.

Table 1. Reverse Park transformation

1. Third phase calculation: $I_a = -I_b - I_c$

2. Transformation: $\begin{pmatrix} I_x \\ I_y \end{pmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix}$

3. Reverse Park Rotation: $\begin{pmatrix} I_d \\ I_q \end{pmatrix} = \begin{bmatrix} \cos\rho & \sin\rho \\ -\sin\rho & \cos\rho \end{bmatrix} \begin{pmatrix} I_x \\ I_y \end{pmatrix}$

The forward transformation converts two orthogonal rotor referenced voltages, V_d and V_q, to three-phase stator voltage signals, I_a, I_b and I_c. The transformation consists of two stages (Table 2), where ρ is the angle of the rotor field.

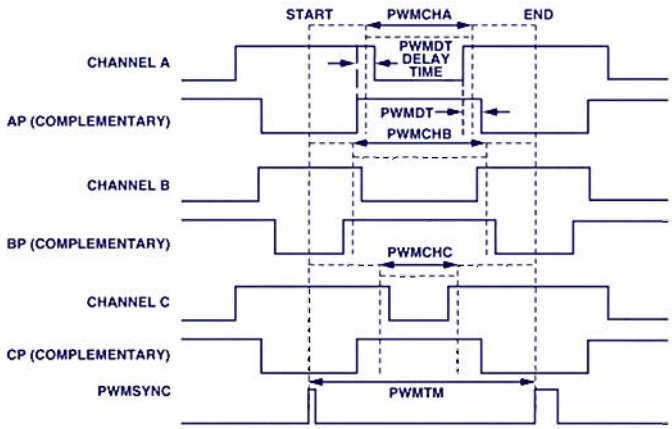


Figure 5. PWM waveform features in ADMC201.

Table 2. Forward transformation

1. Forward Park Rotation: $\begin{pmatrix} V_x \\ V_y \end{pmatrix} = \begin{bmatrix} \cos\rho & -\sin\rho \\ \sin\rho & \cos\rho \end{bmatrix} \begin{pmatrix} V_d \\ V_q \end{pmatrix}$

2. Inverse Clarke

Transformation: $\begin{pmatrix} V_a \\ V_b \\ V \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3/2} \\ -1/2 & \sqrt{3/2} \end{bmatrix} \begin{pmatrix} V_x \\ V_y \end{pmatrix}$

The ADMC201 digital I/O block has six digital lines, which can be configured as either inputs or outputs. They can also be configured as interrupt sources for system-protection functions. The I/O block is accessed via four memory-mapped registers.

AC servo motor control software: The software required to control an ac servo motor using the ADSP-2105 can take fewer than 500 lines of DSP code. Space limitations prevent a full description of the software here, but we will describe some of the core algorithms and code.

The current-control algorithm is synchronized to PWM frequency through an interrupt signal. The motor currents are sampled at the start of the PWM cycle by connecting the ADMC201's PWMSYNC pin (from the timer block) to the ADC's CONVST pin. The ADMC201's interrupt (IRQ) signal, connected to the ADSP-2105's IRQ2 pin, interrupts the DSP at the end of the A/D conversion cycle. The captured current signals represent the average winding current value since the sampling is at the mid-point of the current waveform. A set of current measurements are presented to the DSP after the start of each PWM cycle; and a new set of stator voltage values and PWM times are calculated before the next cycle.

The current loop signal flow diagram, in Figure 6, describes the flow of information between the ADSP-2105 DSP and the ADMC201 coprocessor. The algorithm starts when an interrupt from the ADMC201's A/D converter indicates that a new set of current samples are available. The DSP reads two phase-current values from the ADMC201's V and W registers, adjusts them for A/D and current sensor offsets, and writes them to the ADMC201 PHIP2 and PHIP3 vector transformation block, along with the rotor angle, RHO. The ADMC201 starts the reverse vector rotation, while the DSP may perform protection functions, such as overload detection or bus-voltage monitoring. The end of the transformation is signaled by an interrupt; then the DSP reads the ID and IQ registers and implements the current-loop control algorithm. The calculated VD and VQ values are written to the ADMC201's VD and VQ registers, along with the rotor angle RHOP. The ADMC201 starts the forward vector rotation, while the DSP may perform some further house keeping functions. The end of the transformation is signaled by another interrupt; the DSP reads the PHV1, PHV2 and PHV3 registers and scales these values according to the PWM period and bus voltage. The DSP then writes three new values to the PWM registers: PWMCHA, PWMCHB and PWMCHC, to close the current control loop.

The control algorithm consists of a number of control laws and some reads and writes to ADMC201 data registers. The ADI fixed point DSP is particularly well-suited to implementing control laws such as P-I (proportional + integral control) loops and state-space algorithms, for which there are many examples. The memory-mapped structure of the ADMC201 has the advantage that no

special read or write sequence is required to access the data registers. The ADMC201 read and write registers are mapped to a block in the DSP external DM address space through the chip-select line on the device. A sample of the interrupt service routine code for an ADMC201 A/D converter interrupt is shown in the table below to illustrate this point. The first instruction is to read the ADMC201 system status register, using a data-memory read instruction. The AR register is then loaded with a constant which has the ADMC201 A/D interrupt bit set. If the A/D interrupt is not set then proceed to check for other sources of interrupt such as the PARK block interrupt. If bit is set then read the A/D registers and start the current loop algorithm.

```
IRQ2_ISR  AY0 = DM(ADMC201_SYSSTAT_);  read ADMC201 stats register
:         AR = ADMC201_AD_INT;         ADMC201 A/D interrupt bit
          AR = AR AND AY0;             test: is this bit set?
          IF NE JUMP PARK_INTERRUPT;   if not set then jump to next interrupt
          AX0 = DM(ADMC201_ADCV_);     read the A/D channel V register
          DM(I_PH_V) = AX0;            save value in data memory
          AX0 = DM(ADMC201_ADCW_);     read the A/D channel W register
          DM(I_PH_W) = AX0;            save value in data memory
          .....
```

Conclusion: We have selected an example of a control scheme for a permanent-magnet ac servo motor implemented with an ADSP-2105 (or ADSP-2115), ADMC201 and AD2S90 chip set.* These hardware choices allow for a lot of flexibility in the system configuration. The ADSP-2115 can be upgraded to an ADSP-2101 or an ADSP-2181 if more processing "horsepower" is required. The lower-cost ADMC200 can be used if the additional analog channels and digital I/O are not required. The ADSP-2105 and ADMC201 can also be used to control ac induction motors, with an encoder used in the place of the resolver.

An evaluation system is available,† using the ADSP-2101 EZLAB and an ADMC201 board. It comes with software, which illustrates the key features of the ADMC201 function blocks. This system can be used to build the control elements of a three-phase motor-control demonstration system.

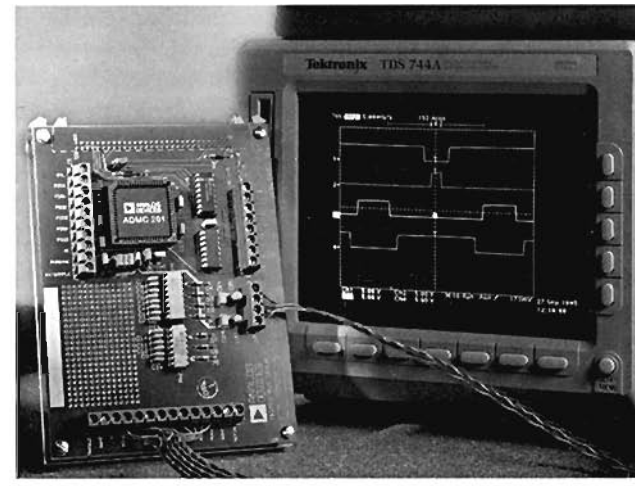


Figure 7. Motor-control evaluation system.

The ADMC200/201 core team included Art Lucia, Chris Coughlin, Jerry Hershkowitz, Tony Scavo, Bill Ahern, Lori Berenson, and Paul Kettle at ADI's Transportation and Industrial Products Division, in Wilmington, MA.

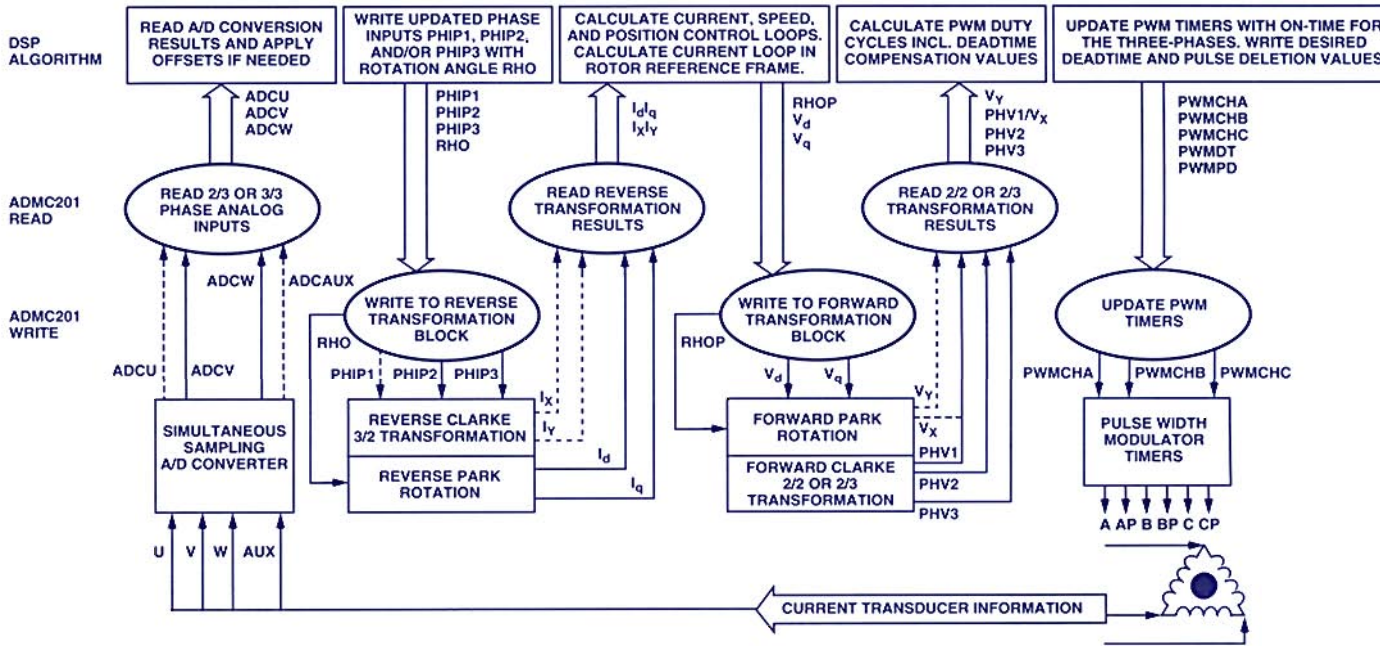


Figure 6. Control signal flow in AC motor control loop.

*For data on these devices, Circle 1
†For information on the evaluation system, Circle 2

Industry's First Integrated Wavelet Video Codec Sets New Standards for Cost, Image Quality and Flexibility

by Alex Zatsman, Mark Rossman, Rich Greene, Will Hooper, Phil Halmark, Bill Valentine, and David Skolnick

The ADV601 is a low-cost, single-chip, all-digital, dedicated-function CMOS VLSI chip for compression and decompression of digital video signals in real time. It can support compression rates of up to 350:1, with essentially lossless 4:1 compression of natural images. The ADV601 supports all common interlaced video formats (see Table 1). The device has been optimized for video applications demanding compression in real time at low cost and with broadcast quality—applications such as nonlinear video editing, video capture systems, remote CCTV surveillance, camcorders, high quality teleconferencing and video distribution systems, video insertion equipment, image and video archival systems, and digital video tape. In addition to compression and decompression, the subband coding architecture of the ADV601 offers inherent support of video scaling and spatial filtering.

Table 1. ADV601 Field Rates & Sizes

Standard	Active Region		Field Rate	Pixel Rate
	Horizontal	Vertical	(Hz)	(MHz)
CCIR-601/525	720	243	59.94	13.50
CCIR-601/625	720	288	50.00	13.50
Sq. Pixel/525	640	243	59.94	12.27
Sq. Pixel/625	768	288	50.00	14.75

With landmark standards already existing in the form of JPEG, H.261, MPEG 1 and MPEG 2, do we need a new compression paradigm? Briefly, Yes. There are many closed-system applications where cost, image quality, and flexibility are more important than inter-operability (the advantage of a standard). For applications that do not require inter-operability, the choice of a compression solution should be driven by the evaluation of these factors, plus *symmetry*—low cost and complexity in both encode (compression) and decode (decompression). The following overview of Wavelet compression and its role in the ADV601 should be helpful in understanding the value it can bring to video compression applications.

Figure 1 shows that in the Encode mode, the ADV601 accepts component digital video through its Video interface and outputs a compressed bit stream though the Host interface. In Decode mode, the reverse is true: the ADV601 transforms a compressed bit stream at its Host interface to component digital video at the Video interface. The host has access to all of the ADV601's control and status registers via the Host interface.

Figure 1. Basic functions of the ADV601.

The ADV601 codec's compression algorithm is based on the bi-orthogonal wavelet transform, embodied with 7-tap high-pass and 9-tap low-pass filters, and implements field-independent sub-band coding. Sub-band coders transform two-dimensional spatial video data into spatial frequency filtered sub-bands. Then adjustable quantization and entropy encoding processes are used to provide compression (see Figure 2).

Figure 2. Basic functions within the ADV601.

The ADV601 is based on wavelet theory, a new mathematical tool first explicitly introduced in Morlet and Grossman's works on geophysics during the mid-1980s.[1] This theory quickly became popular in theoretical physics and applied math; and the late '80s and '90s have seen a dramatic growth in wavelet applications to signal and image processing.[2,3,4,5]

Understanding the wavelet kernel is key to comprehending the advantages of wavelets in video applications. This portion of the device contains filters and decimators that work on the image in both horizontal and vertical directions. The filters are based on carefully chosen segmented wavelet basis functions such as those shown in Figure 3. These basis functions have 3 key benefits: they correlate better to the broadband nature of images than do the sinusoidal waves of Fourier transforms; the ADV601 can implement these functions with simple, compact 7- and 9-tap FIR filters (key to low-cost silicon); and these functions provide full-image filtering—which eliminates the block-shaped artifacts in the compressed image that occur when an image is broken up into smaller areas to be compressed separately (JPEG and MPEG* can both be subject to this artifact in certain applications).

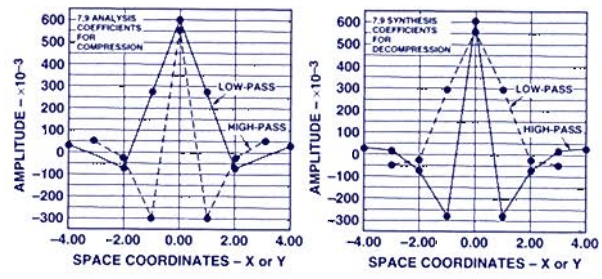
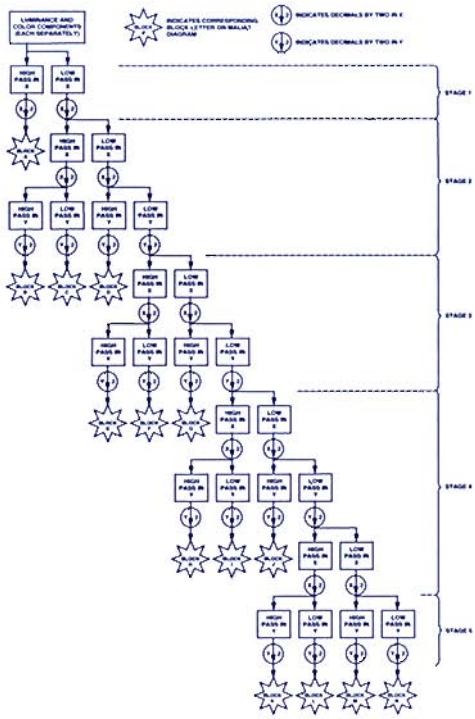


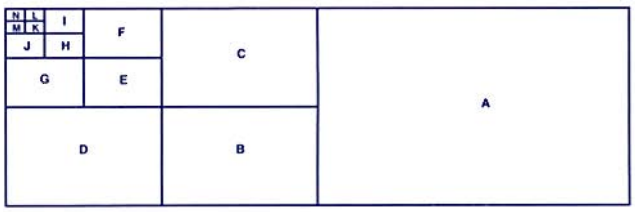
Figure 3. Impulse response of the internal filters. Left: analysis (compression); Right: synthesis (decompression).

The filter tree involves successive high- and low-pass filtering of two-dimensional (x and y) data, with decimation by 2 at each step (Figure 4a), resulting in successively smaller blocks of data, shown combined in a *Mallat diagram* (4b). All three components (e.g., Y,C_b,C_r) of a color video signal field are alternately passed through the filter tree to create a total of 42 new images (14 for Y, 14 for C_r, and 14 for C_b).

*Compression based on standards from Joint Photographic Experts' Group and Motion Picture Experts' Group.



a.



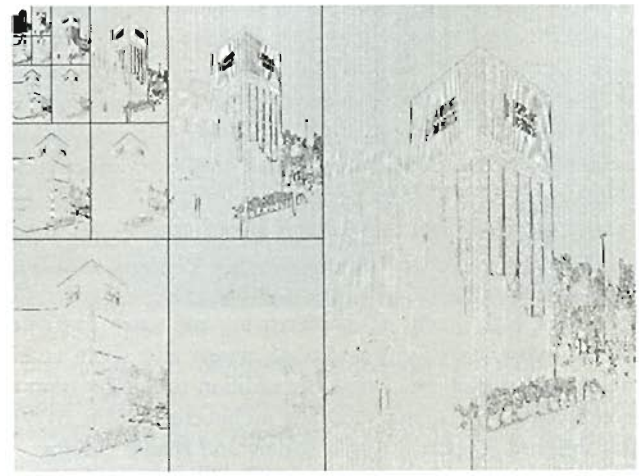
b.

Figure 4. a. Filter tree. Starred outputs are respective blocks of Mallat diagram. b. Modified Mallat diagram. Block letters correspond to those in filter tree.

An example of what the transform does to a black and white image (luminance only) is shown in figure 5. In this case the Analog Devices Headquarters image has been transformed into 14 new images, each containing a different set of information about the original image. One can clearly see the vertical edges resulting from high-pass x-filtering in block A, the horizontal edges from high-pass y-filtering in block D, and the reduced-size original image from decimation and low-pass filtering in block N. *No compression has occurred yet; the total number of data points used to describe the 14 blocks shown is identical to the number used in the original image.* But now that the image has been transformed, we can do some useful things: 1) implement nearly lossless compression, 2) achieve lossy compression at either constant quality or constant bit rate, 3) create high-quality scaled images without computational overhead, and 4) create an error-resilient compressed bit stream, since each block contains information about the whole image.

Figure 6 shows the scheme for using the ADV601 in lossless mode. In this case the 42 transformed blocks are sent to 2 types of lossless entropy coders. The entropy coders benefit from the increased correlation found within the transformed blocks. In this mode of operation, the compression performance is tied to the degree of complexity in the original. If the original image is of a simple ramp, all the blocks will contain zeros, except for the smallest block in the upper left hand corner (N). This would yield lossless compression in excess of 300:1 (requiring less than 0.5 M bits/s

a.



b.

Figure 5. a. Unfiltered original image (Analog Devices Corporate Headquarters, Norwood MA). b. Modified Mallat diagram of the image. Note that each block contains information drawn from the entire image.

for 4:2:2-coded CCIR601 resolution video at 60 fields per second). But if the image is of white noise, there are no correlation opportunities, and the compression must be near 1:1 (requiring approximately 168 M bits/s). In a typical real video application, the compression would range from 2:1 (84 Mb/s) to 5:1 (16 Mb/s), depending on the complexity within each field. In applications calling for near-lossless compression, the ADV601 can be used in this mode—if large swings in bit rate are allowed.

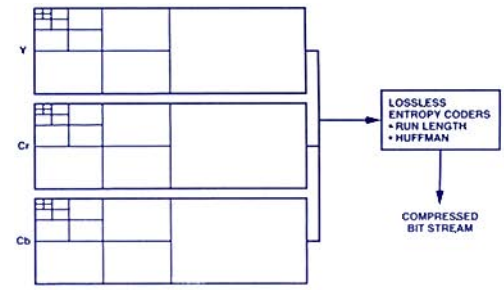


Figure 6. Lossless compression option.

Figure 7 shows how one might use the ADV601 in a lossy compression mode. As the image is being transformed, a set of statistics is extracted for all 42 blocks, including the sum of squares (or energy), minimum pixel value, and maximum pixel value for

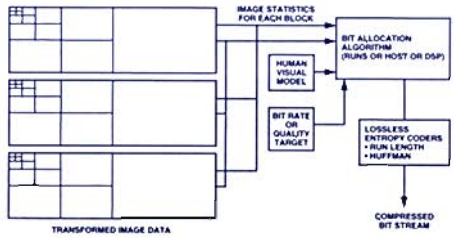


Figure 7. Lossy compression.

each block. This information goes to the quantizer and is coupled with the human visual model, which relates the importance of each block to the human visual system. The quantizer algorithm takes all this information, plus the user-programmed bit rate, and calculates 42 values—"bin widths"—for each field; they can be thought of as the accuracy budget per block. When lightly quantized (i.e., many small quanta), this number will be large. Heavy quantization (few large quanta), leads to a much smaller number. Two examples follow to help illustrate how this works. The actual quantizer is on the ADV601, but a host or external DSP performs the bin-width calculation.

The first case is of a high-quality application calling for visually lossless compression, while maintaining an accurate bit rate. In this case all low-frequency bands (the smaller blocks) will be given the maximum bin width to ensure perfect reconstruction. The high-frequency bands (the largest blocks) will get as large a bin width as can be allocated, based on the complexity of the image. In this case, a small amount of accuracy of high frequency information is given up in order to maintain a desired bit rate. This does not pose a difficult problem, because the human visual system cannot resolve high spatial frequencies to the same level as low spatial frequencies. It has been shown that frequency blocks with light quantization cannot be detected by the human eye (even with broadcast quality video playback equipment).

In the second case, extremely high compression (over 100 to 1) is required. This means that 99% of the bits in each field must be eliminated! Here, only the smallest block gets a large bin width. The remaining budget of bits is sprinkled across the rest of the blocks as determined by the bin-width allocator. Typical compression schemes based solely on information within each field usually fail at high compression; thus the ADV601's ability to maintain adequate information about the image is remarkable. When the algorithm was tested at 350:1 with a football sequence, it was possible to clearly identify the action—and even read numbers on players' uniforms. The video quality at such high compression ratios doesn't fit every application but can be more than adequate for video sequence identification and surveillance.

So what do the artifacts look like, using wavelets, when the compression ratio is too high to render an image accurately? As the compression ratio increases, more and more noise is injected into high spatial frequencies; with less accuracy to describe high frequencies, noise is increased in those bands. As a result, wavelet video compression degrades much like conventional broadcast analog video. Though artifacts in video are never pleasing, humans are highly conditioned to accept this type of artifact. Since the ADV601 allows control over the gain of each subband, it is possible to reduce the noise by making the image "soft". Most other compression schemes break the image up into smaller blocks, and each is processed separately. As compression increases, the first artifact to appear is a stationary grid of blocks laid on top of the image. There is general agreement that such blocking artifacts are more objectionable to the human visual system than high frequency noise or image softening.

Figure 8 is a functional block diagram of the ADV601, and Figure 9 shows how it would be used in a typical host-based ADV601 application. The ADV601 video interface is designed to work with all popular analog video decoders and encoders—including those from Analog Devices, Philips, Brooktree, and Raytheon. The video interface is also capable of interfacing directly to all parallel CCIR656-compliant devices (also known as "D1"). Table 1 shows the field rates and image sizes supported by the ADV601. The DRAM manager provides a glue-less interface to a 256 K × 16 fast page-mode DRAM required to support the ADV601 during both encode and decode modes. The general-purpose host interface can be configured in widths of 8-, 16- and 32 bits. The host interface also includes a 512 × 32-bit FIFO to help enable smooth transfer of compressed video data.

A host-based software driver, part of a complete Video for Windows driver package Analog Devices has developed to support the ADV601, assists the ADV601 in calculating the 42 bin-width values for each field. Analog Devices has also created a plug and play PCI board for Windows 95, called Videolab, for evaluating the video quality of the ADV601.

The ADV601 can also be used in stand-alone applications, with the assistance of an ADSP21xx-class DSP to calculate the bin-width values for each field. The ADV601 DSP serial interface supports a glueless interface to all Analog Devices DSPs.

The ADV601JS, packaged in a 160-pin PQFP, operates over the 0 to +70°C commercial temperature range. Get in touch with Analog Devices or your local sales office for further information. Budgetary pricing is $35 in 10,000s. For technical data, **Circle 3**

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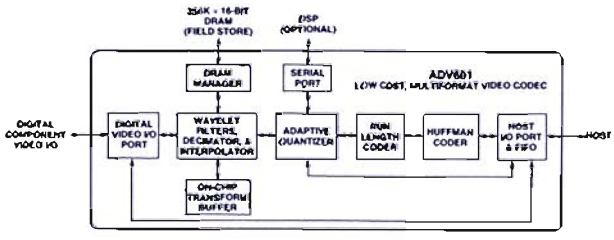

Figure 8. Functional diagram of the ADV601.

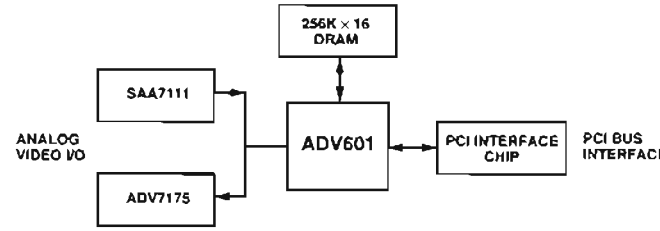

Figure 9. Typical application environment.

Audio Noise-Reduction IC

Single-ended system achieves 25 dB of noise reduction without pre-encoding

by John McDonald

The SSM2000* is an audio dual-channel noise-reduction IC that reduces noise through a combination of variable filtering and downward expansion, in conjunction with a unique adaptive noise-threshold detector. Without requiring pre-encoding of program material, this combination of techniques yields an overall noise reduction of up to 25 dB on a wide variety of program sources: AM and FM radio, open-reel and cassette tape, LPs, CDs, Dolby-B®-encoded programming, broadcast studio-transmitter links and telephone lines, and other audio sources—without the need for any additional manual adjustment. The HUSH® Noise Reduction System, as implemented in the SSM2000, has been demonstrated to reduce noise substantially—while preserving fidelity and transparency—in PC multimedia, intercom systems, teleconferencing systems, mobile communications, automotive audio, home stereos and TVs, and other consumer and professional audio applications.

Analog noise-reduction systems must be able to distinguish between "hiss", or white noise, and the source material, and then attenuate the noise. One method of noise rejection assumes that all signal levels below a pre-selected magnitude are noise, and then attenuates that noise via a voltage-controlled amplifier (VCA). A popular variation of this noise-reduction method is found in Dolby B® cassette tape systems. This double-ended (encode-decode) approach achieves about 9 to 10 dB of improvement in signal-to-noise ratio by incorporating a high-pass compressor on the recording side and a high-pass expander during playback.

Another technique senses and rejects noise by measuring the frequency content of the audio signal and then filtering all noise that occurs above the highest audio frequency. This method utilizes a voltage controlled filter (VCF) and is the key to operation in the single-ended DNR™ system, which achieves about 10 dB of noise rejection; performance is limited by the fixed noise threshold, which can be ineffective on very noisy material and can interfere with signal content of noise-free signals.

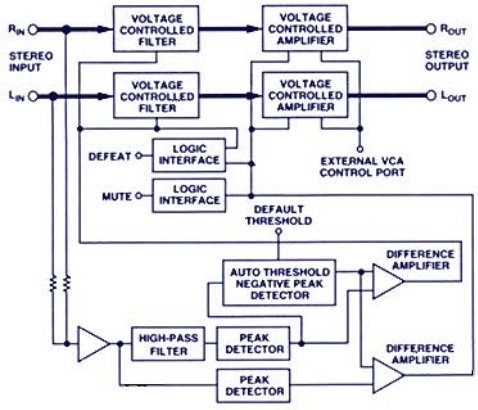

Figure 1. SSM2000 system block diagram

The HUSH® single-ended system (Figure 1) incorporates aspects of both approaches, resulting in up to 25 dB of noise rejection *without needing pre-encoding.*

The principal key to the SSM2000's ability to reject noise is its ability to *recognize* the noise floor, whether it be the low-level hiss of an audiotape, or the higher-level noise interfering with reception of weak stations in an automobile radio. This is accomplished in a patented noise threshold detector, which operates on the principle that virtually all program material contains gaps during which the only energy present (especially at frequencies in the 3-kHz to 8-kHz region) is noise. A negative peak follower finds the lowest of these intervals at a given time and subsequently causes the VCA gain to be substantially reduced (*downward expansion*) for input levels in the vicinity of that threshold. The threshold is constantly updated, *adapting* to the characteristics of the input.

Another principle is that the highest audio signal amplitudes typically occur at low frequencies (100 Hz to 1 kHz) and taper off exponentially as frequency increases. This allows the possibility of maintaining wide bandwidth for signal levels well above the noise floor, but significantly reducing the bandwidth for input levels approaching the noise floor—rejecting mostly noise, with little effect on signal reception, so long as changes in gain and bandwidth are not excessively rapid. Indeed, the SSM2000 responds well to sudden transitions from low noise levels to normal noise levels.

Both Dolby® and DNR™ require input line levels that are carefully controlled in order to reach rated performance. This is because the noise floor magnitude is assumed not to change substantially. In reality, the noise floor often changes with different types of audio input, as a function of equipment, recording media, receiver signal strength, and the environment. As noted above, the patented adaptive noise threshold detector in the SSM2000 senses these changes and will adapt the VCA and VCF operation for optimal noise-reduction performance.

Within the chip, both left and right audio paths through the SSM2000 are differential. This greatly reduces control feedthrough and distortion by taking advantage of the inherent common-mode rejection capability of the differential VCFs, VCAs, and inputs to the output amplifiers. The SSM2000 enables additional functions. For example, a TTL-level-controlled MUTE is provided, for full attenuation. In addition, a DEFEAT pin allows a simple on-off comparison for HUSH® noise reduction. An external VCA control port is also provided for gain control; with simple external circuits, it can provide valuable functions such as automatic volume leveling, compression, and road-noise compensation by taking advantage of the magnitude and frequency information available at separate SSM2000 pins. The SSM2000 can accept a wide range of audio line levels, but external circuitry (pre- or post-) can also be used for control.

The SSM2000 was designed by Analog Devices Fellow Derek Bowers at our Santa Clara facility. James K. Waller, Jr., of Rocktron, Inc., Rochester Hills, MN, is the inventor of the HUSH noise-reduction technology.

*HUSH® is a Registered Trademark of Rocktron Corporation; Dolby® is a Registered Trademark of Dolby Laboratories, Inc.; DNR™ is a Trademark of National Semiconductor Corporation. Technical data is available at our World Wide Web site (see page 24) and via AnalogFax (Faxcode 1952).

A Bibliography on EMC/EMI/ESD

And other threats to signal and circuit integrity

by Daryl Gerke, P.E. and William Kimmel, P.E.*

BOOKS

Electromagnetic compatibility in medical equipment, by William D. Kimmel and Daryl D. Gerke, Interpharm Press/IEEE Press, 1995. Written for the medical device industry, but should be of interest for any EMI discipline. Practical nuts-and-bolts treatment for designers and installers of medical electronics equipment.

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Introduction to electromagnetic compatibility, by Clayton Paul, John Wiley & Sons, 1992. Written as a college text, it is quite analytical.

Noise reduction techniques in electronic systems, by Henry W. Ott, John Wiley & Sons, 1988. Good, quite readable. General overview, strongest in analog electronics. Recommended for a first book.

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**Messrs. Gerke and Kimmel, the principals of Kimmel Gerke Associates Ltd., are consulting engineers in the EMI design and troubleshooting field. Their services include EMI design and systems consulting, EMI seminars, EMI design reviews, and EMI Toolkit® software—a collection of over 30 useful formulas, graphs, and tables. For information on their services write to 1544 N. Pascal, St. Paul, MN 55108, phone (612) 330-3728, or check their Web page at http://www.emiguru.com.*

PERIODICALS

"KGB Newsletter" (*Kimmel Gerke Bullets*), by the Authors. Authoritative quarterly newsletter by industry leaders. Free.

"Compliance Engineering," by Compliance Engineering, 271 Great Rd., Acton MA 01720, (508) 264-4208, Quarterly. General-interest regulatory issues, including EMC. Also an annual Reference Guide with the same title.

"ENR" (*Electromagnetic News Report*), Seven Mountains Scientific, P.O. Box 650, Boalsburg PA 16827, (814) 466-6559. Bi-monthly. Newsletter on EMC issues, with strong flavor on international regulatory issues. Subscription, about $70/year.

IEEE: *IEEE Transactions on Electromagnetic Compatibility*, monthly. Highly analytical. Subscription with IEEE EMC Society membership. We actually find more practical articles on EMI in *IEEE Industry Applications Society Transactions*.

"ITEM" (*Interference Technology Engineers' Master*), R&B Enterprises, 20 Clipper Rd., West Conshohocken PA 19428, (215) 825-1960. Annual reference guide plus quarterly updates. Reference material for design and regulatory requirements.

VENDOR REFERENCE MATERIAL

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[Ed. note—Our regular readers know that a plethora of publications from ADI, from data sheets to our seminar notes, Applications Reference Manual and these pages, include much practical advice on maintaining signal integrity. Check the list at the back of our *1996 Short Form Designers' Guide*.]

"Steward Suppression Ferrites, Product and Applications Guide," Steward, P.O. Box 510, Chattanooga TN 37401, (615) 867-4100. Reference on ferrite applications.

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MIL-STD-1857, 1976: Grounding, Bonding & Shielding Design Practices. Good reference.

Most military documents may be ordered from Naval Publications & Form Center, Standardization Document Order Desk, 700 Robbins Ave., Building 4, Section D, Philadelphia PA 19111-5094. Or fax order to (215) 697-2978. They won't accept telephone orders, but you can call for information on (215) 697-2667 or -2179. You need not be a government contractor to get most documents. ◘

Single-Chip Digital Stereo Subsystem

AD1859 simplifies audio playback, Improves fidelity, Easily handles a wide range of sample rates

by Pete Predella

The AD1859* offers the industry's most functionally complete 16/18-bit stereo digital audio playback subsystem on a single chip. It converts serial digital input data to filtered, buffered, low-distortion, gain-controlled stereo analog output. Its asynchronous master clock, a digital phase-locked loop (DPLL), allows it to accept data from a variety of sources, with clock rates from 28 kHz to 52 kHz (using an external 27-MHz crystal), rejecting sample-clock jitter and greatly simplifying interfacing.

It is ideal for many applications, including digital cable TV and direct broadcast satellite set-top decoder boxes, video CD players, CD-I players, high-definition televisions, digital audio broadcast receivers, digital audio workstations, multimedia computers, and all forms of CD and digital tape players.

The monolithic AD1859 comprises (Figure 1) a variable-rate oversampling digital interpolation filter, an innovative multibit sigma-delta (Σ–Δ) modulator with dither, a jitter-tolerant digital-to-analog converter (DAC), switched-capacitor and continuous-time analog filters, and analog output drive circuitry—as well as an on-chip dc voltage reference—housed in a 28-lead SOIC or SSOP package. The on-chip volume controls (a system cost saving) include a stereo attenuator and mute, programmed entirely through an SPI†-compatible serial control port.

A typical application where the AD1859 offers especial advantages, MPEG audio, calls out a requirement for three different sample rates: 32-, 44.1-, and 48 kHz. With a typical sigma-delta audio DAC, the designer would have to provide an external clock circuit to synthesize the "master clock" associated with each of these three sample frequencies. With the AD1859—the first audio DAC to have an asynchronous master clock—this task is simplified. All that is needed is a 27-MHz clock (furnished externally or generated on-chip using an external 27-MHz crystal); the AD1859's phase-locked loop automatically adapts to different incoming sample rates—a major system cost saving. The DPLL will lock to any new sample rate (applied to the Left-Right clock pin) within 100 to 200 ms; jitter components more than 15 Hz above and below the sample frequency are rejected at 6 dB per octave (e.g., jitter at 150 Hz above or below the sample rate is reduced by 20 dB).

Guaranteed performance characteristics include minimum dynamic range of 88 dB with an A-weight filter (85.7 dB without

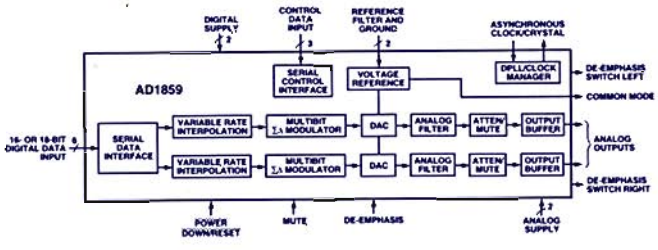


Figure 1. AD1859 Block Diagram.

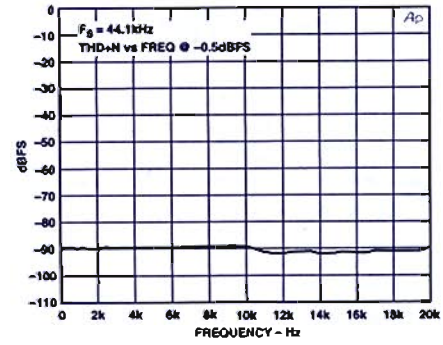


Figure 2. THD+N vs. frequency at –0.5 dBFS.

filter), and maximum total harmonic distortion & noise (THD+N) of –84 dB (0.0063%) over the audio band, 20 Hz to 20 kHz. Figure 2 is a typical plot of THD+N vs. frequency at –0.5-dBFS amplitude. Figure 3 is an FFT of a –90-dB, 1-kHz tone, accompanied by a time-domain plot, demonstrating the freedom from harmonics, spurs, and quantization effects at this low level, typical of analog systems but hard to achieve digitally.

Another feature uniquely available with the AD1859 is an innovative multibit sigma-delta modulator (see sidebar), that helps to reject clock jitter—a system audibility advantage—and reduces out-of-band energy, a system cost saving.

Interface to the AD1859 is simple—via a flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSPs, AES/EBU receivers, and sample-rate converters. The versatile serial data input port can be configured for left-justified, I²S-justified, right-justified, and DSP serial port compatible modes. The chip accepts 16 or 18-bit audio data in MSB-first, twos-complement format. The AD1859 supports continuously variable sample rates and with essentially linear (to within ±0.1%) phase response. De-emphasis is optionally available at the analog output stage, achieving improved, sample-rate invariant, noise reduction with the addition of just a few external components. (Figure 4)

A power-down mode (48 mW vs. 330 mW) minimizes power consumption when the device is inactive. The entire stereo digital audio playback subsystem operates from a single +5-V supply over the temperature range –40°C to +105°C; it is packaged in 28-pin SOIC and SSOP. Prices start at $4.90 in 1,000s.

The AD1859 was designed in Wilmington, MA, by Bob Adams, Tom Kwan, and Bob Libert, of our Computer Products Division.

*Technical data is available at our Web site, **http://www.analog.com**; or use **AnalogFax™** to request **Faxcode 1853 (16 pp.)** or **Circle 4**

†SPI is a registered trademark of Motorola, Inc.

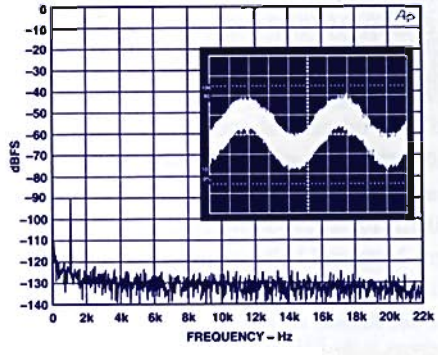


Figure 3. FFT of 1-kHz tone at –90 dBFS, and time-domain plot (band-limited to 22 kHz), showing freedom from harmonics, spurs, and quantization effects.

The AD1859 offers superb fidelity and low-level linearity, greatly reduces circuit complexity, can be interfaced easily to DSPs (digital signal processors) and ADCs (analog-to-digital converters), and cuts the power consumption and cost of digital audio playback systems.

It has two key differentiating features from conventional devices. First is its unique DPLL (digital phase-locked loop) clock manager. This is an asynchronous sample-rate manager that automatically adjusts to incoming sample frequencies and allows the AD1859 to be clocked by a different frequency from its own master clock. It is based on patented asynchronous sample-rate conversion technology developed at Analog Devices (*Analog Dialogue* 28-1, 1994, pp. 9-11). Until now, no other audio DAC has had this capability. Other audio DACs (digital-to-analog converters) require a well-tuned, high-frequency master clock that runs at 256 or 384 times the intended audio sample rate. The generation and management of this high-frequency synchronous clock is burdensome to the board-level designer.

An external asynchronous clock oscillator may be used to furnish the AD1859's master clock; however, the AD1859 includes an on-chip oscillator, so the designer need only provide an inexpensive quartz crystal or ceramic resonator as the external time base. The AD1859's on-board DPLL will lock to any incoming sample rate between 1/512 and 1/1024 of its master clock frequency in about 100 ms. Jitter on the crystal time base or MCLK input is rejected (by virtue of an on-chip switched-capacitor filter), as well as jitter on the incoming LRCLK input—to a level unprecedented in audio DACs.

The second differentiating feature of the AD1859 is its patented multibit sigma-delta modulator, which results in dramatically less out-of-band noise energy than competitive ICs. Lower out-of-band noise energy reduces the need for post-DAC filtering, so that all the necessary post-DAC filtering (except for optional analog de-emphasis) is integrated on chip. Another attribute of the multibit Σ-Δ modulator is its high immunity to digital substrate noise, further improving audio signal integrity.

What is a multibit sigma-delta modulator? In an elementary approach, typical sigma-delta modulators have two levels of quantization, and DACs must average pulsewidth-modulated full-scale square waves; but in the case of the AD1859, 17 levels of quantization are used, and the input to the averaging filter can be thought of as the much easier task of smoothing the 1/16th-full-scale elements of a 17-level staircase. In addition, the AD1859 samples the input signal at 128 times the input sample rate, double the conventional rate. The additional quantization levels and higher oversampling ratio means that the output spectrum contains dramatically lower levels of out-of-band noise energy; permitting a much simpler post-DAC reconstruction filter. Its reduced transition-band steepness and attenuation requirements result in lower phase distortion and improved fidelity.

Is there a downside? The problem that conventionally limits the performance of multibit Σ-Δ converters is the nonlinearity of the passive circuit elements used to sum the quantization levels. The designers have invented a revolutionary architecture that overcomes the problem[1].

Other interesting features of the chip include the use of a dither with a triangular probability distribution function to further reduce quantization noise; and on-chip low-pass filtering consisting of a 2nd-order switched-capacitor filter, followed by a first-order analog continuous-time filter. In addition to filtering out noise, it reduces the effects of any residual master-clock jitter.

[1]See "A stereo multi-bit Σ-Δ DAC with asynchronous master-clock interface", by Tom Kwan, Bob Adams, and Bob Libert, *1996 IEEE International Solid-State Circuits Conference Record.*

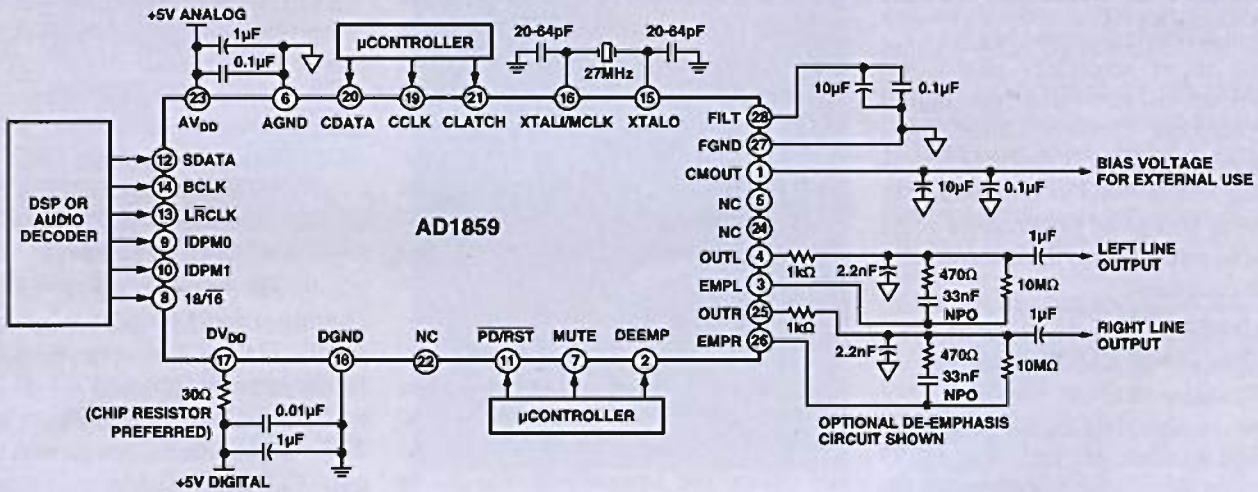
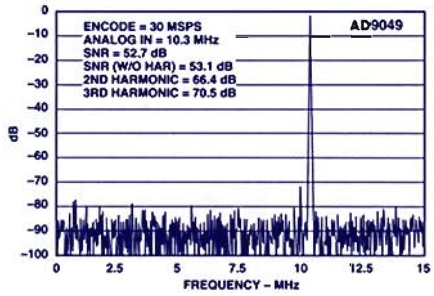


Figure 4. Recommended circuit connection with analog de-emphasis filters and 27-MHz crystal.

A/D Converters—Single Supply, High speed, Low power

9-bit, 30-MSPS ADC

Single-supply AD9049 has 100-MHz analog bandwidth



The monolithic AD9049 is a complete 9-bit parallel-output analog-to-digital converter with on-board track-and-hold and 2.5-V reference. Designed as a low-cost solution for high-performance applications, it can be clocked at rates up to 30 MSPS with excellent dynamic specifications. It is pin-compatible with, and can be upgraded to, the 10-bit, 40-MSPS AD9050 (*Analog Dialogue* 29-3).

Performance is excellent; at an encode rate of 30 MHz, and with a 10.3-MHz analog input, 2nd and 3rd-harmonic distortion are each −60 dB max, signal to noise-and-distortion (SINAD) is 53 dB typical (50 dB min), with a minimum effective resolution of 8 bits (ENOB). A low-power device, the AD9049 requires only 300 mW (400 mW max).

With its high performance and low price, the AD9049 is an excellent choice for applications in low-error-rate digital communication systems using QAM demodulation techniques (such as set-top boxes and wireless local loop receivers). Its economical high-speed performance could also lead to cost savings in medical and video imaging equipment.

The AD9049's Encode clock is TTL compatible, and its CMOS digital outputs are compatible with both +5-V and +3-V logic systems. Operating from a single +5-V supply and specified over the −40 to +85°C temperature range, it is available in 28-pin SOIC and SSOP versions. An evaluation board, the AD9049/PCB, is available. Price of the AD9049 in 10,000s is $9.40; the evaluation board is priced at $200 (each).
Faxcode* 1976

1- and 8-channel 12-Bit SADCs

AD7854/59 have self- and system calibration
Choice of 200-kHz & 100 kHz (L) throughput

The monolithic AD7854 and AD7859 are 1- and 8-channel low-power ADCs that can operate on +3- or +5-volt single supplies. With especially low-power "L" versions available, they are ideal for applications where battery operation and portability are essential. The AD7854 is available in 28-lead cerdip, SOIC, and SSOP, and the AD7859 is available in 44-pin PLCC and PQFP packages.

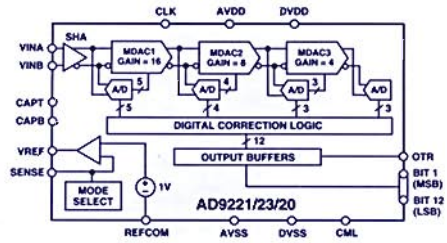
	AD7854	AD7854L	AD7859	AD7859L
Number of channels	1	1	8	8
Sampling rate, ksps	200	100	200	100
Supply voltage, V	+3 to +5.5	+3 to +5.5	+3 to +5.5	+3 to +5.5
SINAD, dB min (10-kHz sine)	70,71†	70,71†	70,71†	70,71†
THD, dB max (10-kHz sine)	−78	−78	−78	−78
Power requirements, V_{DD} = 5.5 V				
Normal mode, mW max	30	10	30	10
Sleep mode, µW max, CLK off	27.5	27.5	27.5	27.5
Conversion time, µs max	4.5	9	4.5	9
T/H acqu. time, µs min	0.5	1	0.5	1
Price, $US, 1000s, SOIC	$9, $11†	$6.65, $8.50†		
Price, $US, 1000s, PQFP			$11.75, $13.75†	$8.80 (A)
Faxcode*	**2006**	**2006**	**1874**	**1874**

†Data shown for A, B versions (−40 to +85°C). AD7854 S version (−55 to + 125°C) available

12-Bit, 1.25- & 3-MSPS CMOS ADCs

AD9221 and AD9223 use single +5-V supply
25 and 40 MHz full-power bandwidth, −86-dB spurs

The monolithic 3-MSPS AD9223 and 1.25-MSPS AD9221 options join the 10-MSPS AD9220 (*Analog Dialogue* 30-1) to provide a wide range of complete, high-performance, low-cost +5-V single-supply 12-bit A/D converter solutions for communications, imaging, medical, and data-acquisition systems. They all share the same analog and digital interface options, 28-pin SOIC packaging, and pinout, permitting easy upgrading or cost reduction, depending on required dynamic performance, sample rate, and power.



Their analog input range is highly flexible, allowing for ac- or dc-coupled differential or single-ended inputs of various amplitudes and offsets. The internal reference can be pin-strapped for either 1 V or 2.5 V, and the range can be further adjusted using external resistors.

With inputs of 0.1/0.5/1.0 MHz to the AD9221/23/20, sampling at their respective maximum rates, signal to noise-and-distortion (SINAD) is greater than 69 dB, THD is less than −83.4 dB, and SFDR is greater than 86 dB. Full-power and small-signal bandwidth are typically 25/40/60 MHz.

The devices all operate over the −40 to +85°C temperature range and are packaged in 28-pin SOICs. Evaluation boards are available. The devices are all uniformly priced at $15.80 in 1000s.
Faxcode* 1936

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Two Monolithic DACs and a Data Acquisition Board

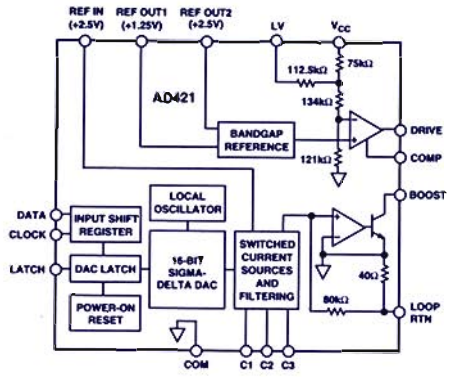
Loop-Powered 16-Bit D/A Converter

AD421 provides 4-to-20-mA process output
Serial input is compatible with HART FSK protocol

The monolithic AD421 is a complete loop-powered digital-to-4-to-20-mA converter, designed to meet the design needs of smart transmitters for industrial control. It provides a high-precision, fully integrated low-cost solution in a small 16-pin package.

Using power provided by the system voltage source in series with the output loop, the AD421 accepts a 16-bit serial digital input and converts it to a current output with a range of 4 to 20 mA.

The AD421 provides regulated power for itself and front-end components at V_{CC} = +3, +3.3, or +5 V, plus two references (+1.25 V and +2.5 V). With worst-case quiescent current of only 750 µA at 5 V, it can provide in normal operation up to 3.25 mA to external components, such as a CMOS signal-conditioning ADC (AD7714/15) and a µcontroller for "smart transmitter" processing of input signals.



Its 3-wire serial input, operating at up to 10 Mbps, is compatible with commonly used µPs and µCs, Motorola SPI bus, and National Semiconductor Microwire; and it can facilitate digital loop communications such as the HART protocol. It is available in plastic DIP & SOIC for –40 to +85°C. Price: $6.75 (1000s). **Faxcode* 1892**

10-Bit Octuple DACs

Rail-to-rail AD7808/09 use single supply, +3 to +5.5 V

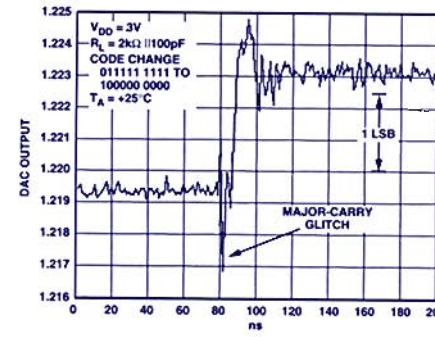
The AD7808 and AD7809 comprise eight 10-bit voltage-output D/A converters. The **AD7808**, in a 24-pin DIP or SOIC, accepts serial data, whereas the **AD7809**, in a 44-pin TQFP, is loaded in parallel.

These devices are octuple versions of the quad AD7804 and AD7805, introduced in *Analog Dialogue* 29-3 (p. 15), but they use only 50% more quiescent current (18 mA max) in normal operation. Power saving modes include System Standby—all DACs or individual DACs (250 µA max) and Power-Down (3 µA max over temperature, –40 to +85°C).

Like the AD7804/05, The AD7808/09 have flexible referencing, permitting a fourfold choice of internal and external references for each DAC, and including a digitally-programmable output offset for each DAC, contributed by an 8-bit sub-DAC with 1/16 the main DAC's sensitivity.

The three-wire serial interface of the AD7808 allows direct interfacing to SPI, QSPI, and Microwire standards. The DACs are double-buffered, allowing individual loading and simultaneous updating; and they can be individually or simultaneously cleared. Double buffering also results in reduced glitch (as shown).

Typical applications for the B grade are found wherever space, power, and cost must be conserved, 10-bit resolution is required, and 9-bit monotonicity is allowable. The AD7808/09 are priced at $10.30/$11.85 (1000s). **Faxcode* 1830**



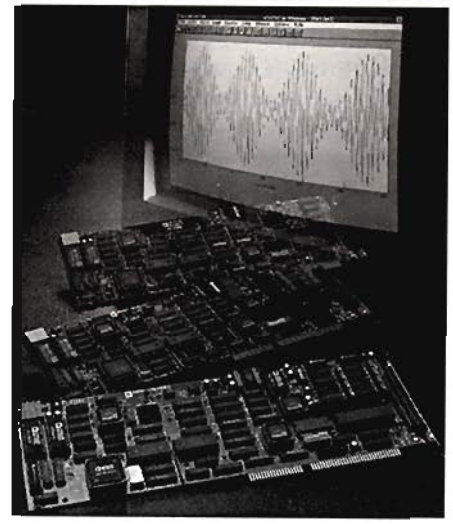
Data-Acquisition Boards Include DSP

RTI-2100 Series: Integrated hardware/software solutions; Sampling ranges 0.5 to 1 MSPS at 12 bits

The RTI-2100 series provides complete state-of-the-art integrated hardware/software solutions at an affordable price. The RTI-2100 offers programmable-gain amplifiers on each input channel (for full-scale signal ranges from millivolts to ±5 V) and on-board simultaneous sample/hold. Sample rates range from 500 kHz to 1 MHz with 12-bit resolution. Also on board are 12- and 16-bit DACs and 24-bit digital I/O lines. Prices start at $1,260.

Besides controlling channel and gain switching, data movement, and data packing, the on-board DSP (ADSP-2101) retains 2/3 of its capacity for functions such as signal filtering and averaging. With repeat string operations and DSP, the RTI-2100 achieves 1-MHz sampling under both DOS and Windows®.

A comprehensive variety of standard software is also available for DOS, Windows 3.1, and Windows 95™. Applications



include process monitoring & control, test & measurement, energy management, and SCADA. Phone 1-800-4-ANALOG or **Circle 5 or use AnalogFax: Faxcode* 7081**

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Amplifiers: Operational, Instrumentation, Isolation

2× & 3× Video Amps

Dual AD8072, Triple AD8073
Low power, Low price

The AD8072 and AD8073 are multiple monolithic video amplifiers with 2- and 3 channels for economical performance in applications such as line driving and RGB amplifying. Both types are available in DIPs and SOICs—the AD8072 in 8-pin packages, the AD8073 in 14-pin—and are specified for operation from 0 to +70°C. Their respective prices (1000s) are $1.25 and $1.50 (i.e., 50¢ per channel for AD8073).

Their supply voltage range is +5 to +12 V single, or ±2.5 to ±6 V dual, with quiescent current of 5 mA/channel max, 3.5 typical (±5 V). Dynamic performance includes 100-MHz bandwidth (–3 dB, G = 2), 500 V/µs slew rate, and 25 ns settling time to 0.1%. Video specs include 0.1-dB gain flatness to 10 MHz, and differential gain and phase errors of 0.05% and 0.1°. 30 mA of output current is available. **Faxcode* 1977**

120-kHz Iso Amp

AD215: Isolation with low distortion & on-board DC-DC

The AD215B isolation amplifier features: an uncommitted input op amp with 1500-V rms galvanic isolation; high speed and accuracy; excellent common-mode rejection; an integral isolated dc-dc power supply with spare power for front-end circuitry; and –40 to +85°C operation.

With full-power bandwidth of 120 kHz and 6 V/µs slew rate, its settling time to 0.1% is 9 µs. Its nonlinearity is low—typically ±0.005%—and not just at dc: harmonic distortion is –80 dB at 1 kHz. CMR is 105 dB, with max leakage of 2 µA rms at 240-V rms, 60-Hz CMV.

Two linearity/isolation grades are available. The AD215 is housed in a 0.840"H SIP package with a 2.48"L × 0.325"W footprint and operates from a ±15-V dc supply. Prices for grades A and B (1000s) are $35.50 and $39.50. **Faxcode* 1981**

Rail-to-Rail Dual OA

Low-cost AD8532 supplies ±250-mA output current

The AD8532, a dual operational amplifier with rail-to-rail inputs and outputs, can furnish up to ±250 mA of load current. This capability can be used to drive headphones, LC displays, and other high-current (and capacitive) loads in applications with 3 to 5 volt supplies, as well as low-voltage stereo equipment.

Features of the AD8532 include 3-MHz bandwidth with 5 V/µs slew rate, operation guaranteed on supply voltages from +2.7 to +5.5, and the ability to sink and source currents up to 250 mA. Input bias current is a low 50 pA max (and it doesn't increase exponentially with temperature!) Also, the input does not suffer phase reversal when overdriven.

Operating from –40 to +85°C, the AD8532 is available in 8-lead DIP, SOIC, and TSSOP packages. Price in 1000s is $0.92 (i.e., 92¢) **Faxcode* 1980**

Quad 15-MHz Op Amp

OP462 swings rail-to-rail
Single/dual available soon

The OP162, OP262, and OP462 are single, dual, and quad op amps combining wide bandwidth (15 MHz), precision (325 µV max offset, 45 µV typical) and low-power (500-µA supply current) operation. Noise is a low 9.5 nV/√Hz at 1 kHz, and drift is typically in the low 1 µV/°C range. Typical applications are in precision filters, portable instrumentation, video, buffering of sampling ADCs, as well as audio and display equipment.

These amplifiers will operate on single supply voltages from +2.7 to +12 V, and are specified for operation on +3, +5, and ±5 V supplies, with rail-to-rail output swing capability. The output stage can sink and source 30 mA. OP462 is housed in 14-lead DIP, narrow-body SO, and TSSOP (8-lead DIP/SO for OP162, 262). OP462 prices (1000s): $3.48 (PDIP,SO), $3.62 (TSSOP). **Faxcode* 1951**

µpower Op Amp

Rail to rail input and output
OP196 draws only 60 µA max

The monolithic OP196 is a single op amp, with similar specs to the rest of its family, the dual OP296 (A-D 30-1, p. 16) and the quad OP496 (A-D 29-3). It has low offset (300 µV max) and up to 450 kHz of bandwidth. Its low power requirements and guaranteed operation on +3 to +12 V supplies well suit it to operation from (and instrumentation of) batteries. Excellent dynamics and low noise (26 nV/√Hz) recommend it for battery-powered audio. It can stably handle up to 200 pF C_{LOAD}.

The input CMV range is equal to the supply; the output swings to <150 mV of the positive rail and ≤70 mV of ground. Temperature specs are 0 to +125°C (3 V) and –40 to +125°C (≥4 V). Packaging is in 8-pin plastic DIP and SOIC. Prices (1000s) for DIPs and SOICs are $1.18 and $1.20. **Faxcode* 1926**

Instrumentation Amp

AD622's price beats the cost of building your own

The AD622 monolithic instrumentation amplifier, an easy-to-use low-cost solution based on the traditional 3-op-amp design, requires no external resistor for unity gain—and only a single external resistor to set any gain from 2 to 1,000 V/V. Its max input offset and drift specs are 250 µV and 2 µV/°C, with 5 nA max input bias current and 86 dB max common-mode rejection (G = 10).

Input noise is low, 12 nV/√Hz (1 kHz), bandwidth is 800 kHz (G=10), and settling time is 10-µs to 0.1% (G=1 to 100). Use it for transducer interfacing, as a difference amplifier, or in low-cost data-acquisition system designs. It operates on power supplies from ±2.6 V to ±15 V, requiring only 1.5 mA, is available in 8-lead PDIPs and SOICs, and operates at temperatures from –40 to +85°C. Price is $2.50 (1000s). **Faxcode* 1986**

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Mixed Bag: DC-DC converters, Temp sensors, Switch, Video encoders:

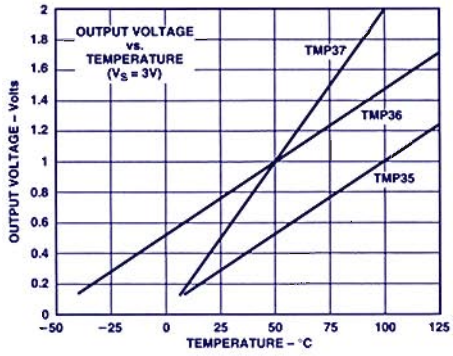
Low-Voltage Temperature Sensors

TMP35/36/37 outputs are proportional to °C
Supply voltage range is from +2.7 V to +5.5 V

The TMP35, TMP36, and TMP37 are monolithic IC temperature sensors that operate on low supply voltages—from 2.7 to 5.5 volts—drawing only 50 µA (max) of quiescent current (275 µW), to conserve battery power and minimize self-heating (< 0.1° in still air). They are available in SO-8, 5-pin SOT-25, and TO-92 packages. "G" grades are priced at $0.75 (75¢) in 1000s.

In addition to supply and output terminals, a fourth SHUTDOWN terminal (except in the 3-pin TO-92) provides for further power saving; in that mode, the device draws only 0.5 µA max (2.75 µW). Typical applications are in monitoring equipment of all kinds, circuit protection, energy management, and alarm systems.

TMP35, TMP36, TMP37 provide output voltage proportional to degrees Celsius.



Device	Sensitivity mV/°C	Range °C	25°C Output mV	Similar Function
TMP35	10	+10,+125	250	LM35/45
TMP36	10	–40,+125	750	LM50
TMP37	20	+5,+100	500	

"G" versions are pre-calibrated for accuracy to within 3°C (typically 1°) at 25°C, and 4°C over the range (2°). Linearity is typically within 0.5°. **Faxcode* 1972, Circle 28**

Dual SPDT Switch

High-precision ADG436
12-Ω R_{ON}, 110-ns t_{ON}

The ADG436 is a monolithic CMOS device comprising two independently selectable single-pole, double-throw (SPDT) switches. They are characterized by low *on* resistance (12 Ω typical, 25 Ω max over temperature), low ΔR_{ON} (3 Ω max over temperature) and R_{ON} match (2.5 Ω max over temperature). Switching time, t_{ON}, is 70 ns typical, 125 max over temperature; t_{OFF} is 5-10 ns less (i.e., break before make). In addition to these specs with ±15-V supplies, the device is also fully characterized for operation on a single 12-V supply.

The analog signal range is rail-to-rail, power dissipation is low, as are leakage current and charge injection. The ADG436 is available in plastic DIP and SOIC packages, for the –40 to 85°C temperature range. Price in 1000s is $2.50. **Faxcode* 1918**

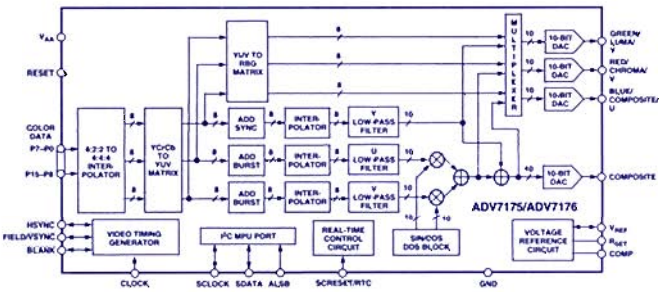
CCIR601 Digital Video YCrCb Encoders

Convert from digital to standard NTSC/PAL TV signals
Studio-quality digital video at consumer video prices

The low-cost, high-performance ADV7175/ ADV7176 convert digital video data into standard analog baseband television signals compatible with NTSC, PAL B/D/G/H/I, PAL M or PAL N standards. They handle both digital YUV (CCIR-601/656—4:2:2) and Square Pixel component digtal video data, gluelessly interfacing to all standard MPEG (I & II) decoders. Besides furnishing composite analog signals, they also drive EuroSCART (RGB), S-Video (Y/C) and YUV analog video signals; and they support close-captioning and Teletext. They are ideally suited for the full range of digital video applications: TV settop boxes, VideoCD, DVD, Internet/ Network Computers, Web TVs, and Multimedia/ Desktop PC video, as well as professional broadcast/head-end and studio video equipment. The ADV7175 incorporates Macrovision® anti-copy-protection process.

The ADV7175/ADV7176 are packaged in a tiny 44-Lead PQFP. 10,000-lot prices start at $7.59.

Circle 20 or Faxcode* 1948 (36-pp.)



DC-DC Converters

28 V in, ±12 and ±15 V out
@100 W, integral EMI filter

The ADDC02812DA and ADDC02815DA are 100-watt dc-to-dc converters for 28 volts dc to ±12 and ±15 V dc. They have an integral filter for differential- and common-mode EMI, designed to meet all applicable requirements of MIL-STD-461D when installed in a typical system setup. They are companion products to the 5-volt-output ADDC02805SA, (*Analog Dialogue* 30-1), and can be combined to implement a total power conversion system.

The many protection and system-level features eliminate the need for costly external components and EMI filtering. They offer built-in transient and thermal protection, along with system-level functions such as Current-sharing, Inhibit, and Status. Each can be used as a stand-alone power supply or as a subsystem in a more-complex design. Prices start at $700 (100s).

Faxcode 2012, Circle 6

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Ask The Applications Engineer—21

by Steve Guinta

CAPACITANCE AND CAPACITORS

I. Understanding the Parasitic Effects In Capacitors:

Q. I need to understand how to select the right capacitor for my application, but I'm not clear on the advantages and disadvantages of the many different types.

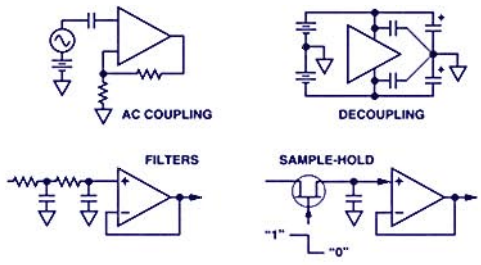
A. Selecting the right capacitor type for a particular application really isn't that difficult. Generally, you'll find that most capacitors fall into one of four application categories:

•*AC coupling*, including bypassing (passing ac signals while blocking dc)

•*decoupling* (filtering ac or high frequencies superimposed on dc or low frequencies in power, reference, and signal circuitry)

•active/passive RC *filters or frequency-selective networks*

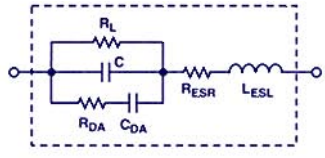
•*analog integrators* and *sample-and-hold* circuits (acquiring and storing charge)



Even though there are more than a dozen or so popular capacitor types—including poly, film, ceramic, electrolytic, etc.—you'll find that, in general, only one or two types will be best suited for a particular application, because the salient imperfections, or "parasitic effects" on system performance associated with other types of capacitors will cause them to be eliminated.

Q. What are these "parasitic effects" you're talking about?

A. Unlike an "ideal" capacitor, a "real" capacitor is typified by additional "parasitic" or "non-ideal" components or behavior, in the form of resistive and inductive elements, nonlinearity, and dielectric memory. The resulting characteristics due to these components are generally specified on the capacitor manufacturer's data sheet . Understanding the effects of these parasitics in each application will help you select the right capacitor type.



Model of a "Real" Capacitor

Q. OK, so what are the most important parameters describing non-ideal capacitor behavior?

A. The four most common effects are *leakage* (parallel resistance), *equivalent series resistance* (ESR), *equivalent series inductance* (ESL), and *dielectric absorption* (memory).

Capacitor Leakage, R_P: Leakage is an important parameter in ac coupling applications, in storage applications, such as analog integrators and sample-holds, and when capacitors are used in high-impedance circuits.

In an ideal capacitor, the charge, Q, varies only in response to current flowing externally. In a real capacitor, however, the leakage resistance allows the charge to trickle off at a rate determined by the R-C time constant.

Electrolytic-type capacitors (tantalum and aluminum), distinguished for their high capacitance, have very high leakage current (typically of the order of about 5-20 nA per μF) due to poor isolation resistance, and are not suited for storage or coupling applications.

The best choices for coupling and/or storage applications are Teflon (polytetrafluorethylene) and the other "poly" types (polyproplene, polystyrene, etc).

Equivalent Series Resistance (ESR), R_S: The equivalent series resistance (ESR) of a capacitor is the resistance of the capacitor leads in series with the equivalent resistance of the capacitor plates. ESR causes the capacitor to dissipate power (and hence produce loss) when high ac currents are flowing. This can have serious consequences at RF and in supply decoupling capacitors carrying high ripple currents, but is unlikely to have much effect in precision high-impedance, low-level analog circuitry.

Capacitors with the lowest ESR include both the mica and film types.

Equivalent Series Inductance (ESL), L_S: The equivalent series inductance (ESL) of a capacitor models the inductance of the capacitor leads in series with the equivalent inductance of the capacitor plates. Like ESR, ESL can also be a serious problem at high (RF) frequencies, even though the precision circuitry itself may be operating at DC or low frequencies. The reason is that the transistors used in precision analog circuits may have gain extending up to transition frequencies (F_t) of hundreds of MHz, or even several GHz, and can amplify resonances involving low values of inductance. This makes it essential that the power supply terminals of such circuits be decoupled properly at high frequency.

Electrolytic, paper, or plastic film capacitors are a poor choice for decoupling at high frequencies; they basically consist of two sheets of metal foil separated by sheets of plastic or paper dielectric and formed into a roll. This kind of structure has considerable self inductance and acts more like an inductor than a capacitor at frequencies exceeding just a few MHz.

A more appropriate choice for HF decoupling is a monolithic, ceramic-type capacitor, which has very low series inductance. It consists of a multilayer sandwich of metal films and ceramic dielectric, and the films are joined in parallel to bus-bars, rather than rolled in series.

A minor tradeoff is that monolithic ceramic capacitors can be microphonic (i.e., sensitive to vibration), and some types may

even be self-resonant, with comparatively high Q, because of the low series resistance accompanying their low inductance. Disc ceramic capacitors, on the other hand, are sometime quite inductive, although less expensive.

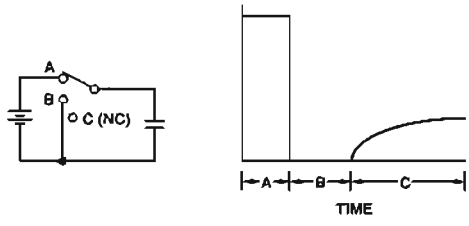
Q. *I've seen the term "dissipation factor" used in capacitor selection charts. What is it?*

A. Good question. Since leakage, ESR, and ESL are almost always difficult to spec separately, many manufacturers will lump leakage, ESR and ESL into a single specification known as *dissipation factor*, or DF, which basically describes the inefficiency of the capacitor. DF is defined as the ratio of energy dissipated per cycle to energy stored per cycle. In practice, this is equal to the power factor for the dielectric, or the cosine of the phase angle. If the dissipation at high frequencies is principally modeled as series resistance, at a critical frequency of interest, the ratio of equivalent series resistance, ESR, to total capacitive reactance is a good estimate of DF,

$$DF \approx \omega R_S C .$$

Dissipation factor also turns out to be the equivalent to the reciprocal of the capacitor's figure of merit, or Q, which is also sometimes included on the manufacturer's data sheet.

Dielectric Absorption, RDA, CDA: Monolithic ceramic capacitors are excellent for HF decoupling, but they have considerable *dielectric absorption*, which makes them unsuitable for use as the hold capacitor of a sample-hold amplifier (SHA). Dielectric absorption is a hysteresis-like internal charge distribution that causes a capacitor which is quickly discharged and then open-circuited to appear to recover some of its charge. Since the amount of charge recovered is a function of its previous charge, this is, in effect, a charge memory and will cause errors in any SHA where such a capacitor is used as the hold capacitor.



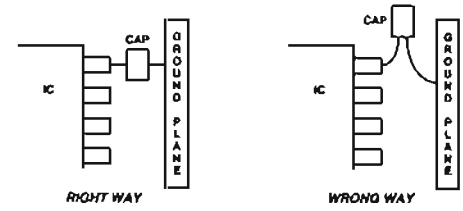
Capacitors that are recommended for this type of application include the "poly" type capacitors we spoke about earlier, i.e., polystyrene, polypropylene, or Teflon. These capacitor types have very low dielectric absorption (typically <0.01%).

The characteristics of capacitors in general are summarized in the capacitor comparison chart (page 21).

A note about high-frequency decoupling in general: The best way to insure that an analog circuit is adequately decoupled at both high and low frequencies is to use an electrolytic-type capacitor, such as a tantalum bead, in parallel with a monolithic ceramic one. The combination will have high capacitance at low frequency, and will remain capacitive up to quite high frequencies. It's generally not necessary to have a tantalum capacitor on each individual IC, except in critical cases; if there is less than 10 cm of reasonably wide PC track between each IC and the tantalum capacitor, it's possible to share one tantalum capacitor among several ICs.

Another thing to remember about high frequency decoupling is the actual physical placement of the capacitor. Even short lengths of wire have considerable inductance, so mount the HF decoupling capacitors as close as possible to the IC, and ensure that leads consist of short, wide PC tracks.

Ideally, HF decoupling capacitors should be surface-mount parts to eliminate lead inductance, but wire-ended capacitors are ok, providing the device leads are no longer than 1.5 mm.



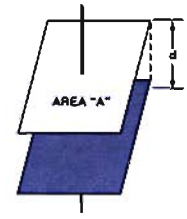
- USE LOW INDUCTANCE CAPACITORS (MONOLITHIC CERAMIC)
- MOUNT CAPACITOR CLOSE TO IC
- USE SURFACE MOUNT TYPE
- USE SHORT, WIDE PC TRACKS

II. Stray Capacitance:

A Now that we've talked about the parasitic effects of capacitors as components, let's talk about another form of parasitic known as "stray" capacitance.

Q. *What's that?*

A. Well, just like a parallel-plate capacitor, stray capacitors are formed whenever two conductors are in close proximity to each other (especially if they're running in parallel), and are not shorted together or screened by a conductor serving as a Faraday shield.

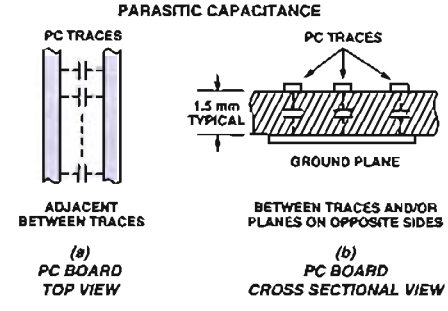


$$C = 0.0085 \times E_R \times \frac{A}{d}$$

C = CAPACITANCE IN pF
E_R = DIELECTRIC CONSTANT RELATIVE TO AIR
A = AREA OF PARALLEL CONDUCTORS IN mm²
d = DISTANCE BETWEEN CONDUCTORS IN mm

Capacitor Model

Stray or "parasitic" capacitance commonly occurs between parallel traces on a PC board or between traces/planes on opposite sides of a PC board. The occurrence and effects of stray capacitance—especially at very high frequencies—are unfortunately often overlooked during circuit modelling and can lead to serious performance problems when the system circuit board is constructed and assembled; examples include greater noise, reduced frequency response, even instability.



For instance, if the capacitance formula is applied to the case of traces on opposite sides of a board, then for general purpose PCB material (E_R = 4.7, d = 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3 pF/cm^2. At a frequency of 250 MHz, 3 pF corresponds to a reactance of 212.2 ohms!

Q. *So how can I eliminate stray capacitance?*

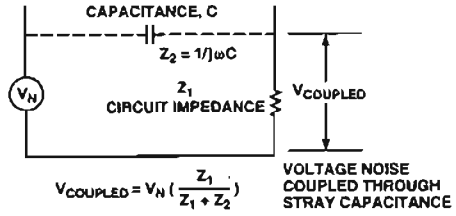
A. You can never actually "eliminate" stray capacitance; the best you can do is take steps to minimize its effects in the circuit.

Q. *How do I do that?*

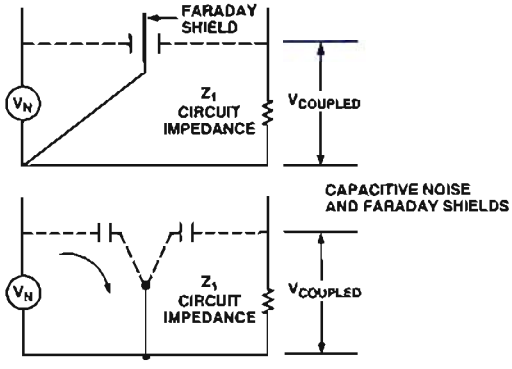
A. Well, one way to minimize the effects of stray coupling is to use a Faraday shield, which is simply a grounded conductor between the coupling source and the affected circuit.

Q. *How does it work?*

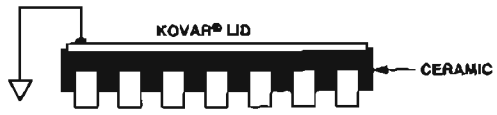
A. Look at the Figure; it is an equivalent circuit showing how a a high-frequency noise source, V_N, is coupled into a system impedance, Z, through a stray capacitance, C. If we have little or no control over V_n or the location of Z_1, the next best solution is to interpose a Faraday shield:



As shown, below, the Faraday shield interrupts the coupling electric field. Notice how the shield causes the noise and coupling currents to return to their source without flowing through Z_1.

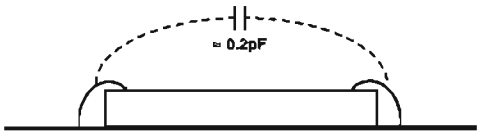


Another example of capacitive coupling is in side-brazed ceramic IC packages. These DIP packages have a small, square, conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected. Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. But many analog circuits do not have a ground pin at a package corner, and the lid is left floating. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is unshielded.

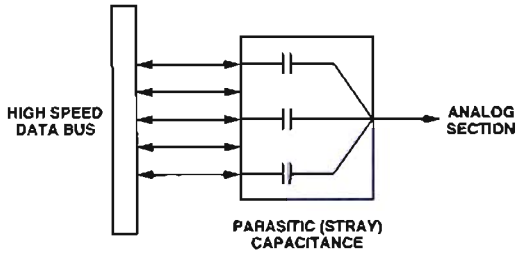


Whatever the environmental noise level, it is good practice for the user to ground the lid of any side brazed ceramic IC where the lid is not grounded by the manufacturer. This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip may be used to make the ground connection, or conductive paint can be used to connect the lid to the ground pin. *Never attempt to ground such a lid without verifying that it is, in fact, unconnected*; there do exist device types with the lid connected to a supply rail rather than to ground!

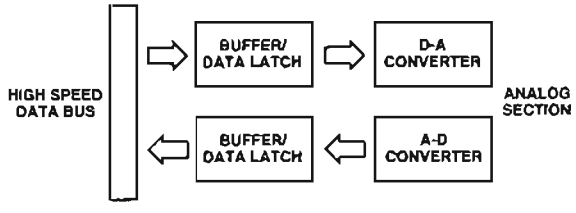
One case where a Faraday shield is impracticable is between the bond wires of an integrated circuit chip. This has important consequences. The stray capacitance between two chip bond wires and their associated leadframes is of the order of 0.2 pF; observed values generally lie between 0.05 and 0.6 pF.



Consider a high-resolution converter (ADC or DAC), which is connected to a high-speed data bus. Each line of the data bus, (which will be switching at around 2 to 5 V/ns),will be able to influence the converter's analog port via this stray capacitance; the consequent coupling of digital edges will degrade the performance of the converter.



This problem may be avoided by isolating the data bus, interposing a latched buffer as an interface. Although this solution involves an additional component that occupies board area, consumes power, and adds cost, it can significantly improve the converter's signal-to-noise. ◘



CAPACITOR COMPARISON CHART

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO ceramic	<0.1%	Small case size Inexpensive Good stability Wide range of values Many vendors Low inductance	DA generally low, but may not be specified Limited to small values (10 nF)
Polystyrene	0.001% to 0.02%	Inexpensive Low DA available Wide range of values Good stability	Damaged by temperature > +85°C Large case size High inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA available Wide range of values	Damaged by temperature > +105°C Large case size High inductance
Teflon	0.003% to 0.02%	Low DA available Good stability Operational above +125°C Wide range of values	Relatively expensive Large size High inductance
MOS	0.01%	Good DA Small Operational above +125°C Low inductance	Limited availability Available only in small capacitance values
Polycarbonate	0.1%	Good stability Low cost Wide temperature range	Large size DA limits to 8-bit applications High inductance
Polyester	0.3% to 0.5%	Moderate stability Low cost Wide temperature range Low inductance (stacked film)	Large size DA limits to 8-bit applications High inductance
Monolithic ceramic (High K)	>0.2%	Low inductance Wide range of values	Poor stability Poor DA High voltage coefficient
Mica	>0.003%	Low loss at HF Low inductance Very stable Available in 1% values or better	Quite large Low values (<10 nF) Expensive
Aluminum electrolytic	High	Large values High currents High voltages Small size	High leakage Usually polarized Poor stability Poor accuracy Inductive
Tantalum electrolytic	High	Small size Large values Medium inductance	Quite high leakage Usually polarized Expensive Poor stability Poor accuracy

Worth Reading

SERIALS

DSPatch—The DSP Applications Newsletter: Number 35 (Spring, 1996) features the ADSP-21csp01 Concurrent Signal Processor for telecommunications and computer applications that must handle several signals simultaneously. The "DSP in Use" section has articles on SHARCs in Mercury Computer's RACE® multicomputing environment and in a SEGA arcade game, and servo control using the ADSP-2171 in Pinnacle Micro's Apex optical hard drive. Also included are a section on C Tips, Q&A, third-party articles on Hyperception, Alex Computer Systems, plus Logic Modeling's full-function model of the SHARC. And more... **FREE, Circle 7**

COMMUNICATIONS DIRECT—Systems and IC solutions for demanding markets: Number 3, April, 1996, features DECT cordless phone technology; a Technical Brief, "Modulating the Alphabet Soup" (sorting out the terminology), an insight into a Standards Committee meeting, and a "Spotlight" on concurrent signal processing. **FREE, Circle 8**

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Signal-Processing Solutions for Today's Managed Medical Market, an 8-page explanation of ADI's focus on and commitment to lower costs for medical equipment manufacturers, through functional integration, system-level integration, partnerships, and technological breakthroughs. **Circle 9**

General-Purpose Converters: Reference Designs, Evaluation Boards, a 10-page description of evaluation hardware and software, including a new evaluation system for high- and medium-speed general-purpose A/D converters, employing an Eval-Control Board in conjunction with daughter cards which implement the test circuits. The powerful processor on the Eval-Control board enables the user to perform FFTs or histogram analysis at specific input and sampling frequencies. Also: evaluation boards for low-frequency converters, controlled from the printer port of a windows PC. **FREE, Circle 10**

Military Product Cross-Reference. More than 50 pages covering Standard-Microcircuit-Drawing (SMD), Joint-Army-Navy (JAN), and /883 Class B products available from ADI. They are listed 3 ways: by Function, by Generic model number, and by Military part or drawing number. **FREE, Circle 11**

PRODUCT HIGHLIGHT BRIEF BROCHURES:

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High-Density Multi-SHARC Modules: Low-cost multiprocessor solutions based on the ADSP-2106x SHARC, 2 pp. Includes overview, low-cost MCMs, next-generation modules. **Circle 13**

High-Density DC-to-DC Converters: Product development for MIL/AERO and commercial applications, 4 pp. Includes Overview, 100/200-W types, 30-W Military/aerospace products, 50/100/150-W Commercial devices, Power management, MCMs and more. **Circle 14**

AD10242 High-Speed Dual ADC: Dual 12-bit, 40-MSPS ADC with front-end signal conditioning and output data buffering, 2 pp. Includes Overview, MCMs and more, Highlights. **Circle 15**

NEW TECHNICAL DATA

ADSP-2100 Family DSP Microcomputers, 64-page technical data, Rev. B. Describes low-cost popular 16-bit fixed-point DSP microprocessors with on-chip memory. Contents: General description, Architecture overview, System interface, Specifications, Timing parameters, Pin configurations, Package outline dimensions. Includes: ADSP-2101, -2103 (3.3-V version of -2101) , -2105 (Low-cost DSP), -2111 (DSP with host interface port), -2115, -2161/2/3/4 (Custom ROM-programmed DSPs). [*Separate data sheets only*: ADSP-2100A, ADSP-2165/66, ADSP-21msp5x, ADSP-2171, ADSP-2181] **FREE, Circle 16**

APPLICATION NOTES

Acceleration-to-frequency circuits, by Charles Kitchin, Dave Quinn, and Steve Sherman [4 pp., AN-411]. Revised and updated. Combining accelerometers with VFCs for frequency-output acceleration-to-frequency circuits. **Circle 17**

Obtaining the best performance from the AD7893, 12-bit serial A/D converter, by Albert O'Grady and Mike Byrne [8 pp., AN381]. How to obtain the best performance from a 12-bit 6-µs ADC with on-chip track/hold, on-chip clock, and high-speed serial interface in a small 8-pin mini-DIP or SOIC. Introduction, layout hints, Evaluating AD7893 performance, Timing and control for optimum performance, Reading during conversion, Power supplies, Shorting plug options, Evaluation board interfacing, Setup conditions, PCB layouts. **Circle 18**

Low-cost, low-power devices for HDSL applications, by Ed Spence [4 pp. AN414]. Ideas for HDSL transceivers using Analog Devices low-cost standard linear ICs. Includes HDSL overview, Modulation method, Bit rates, Power constraints, Block diagram/functions, Future developments, Summary, References. **Circle 19**

MORE AUTHORS [*Continued from page 2*]

Teams Collaborate On Video Compression Chip

The ADV601 was a joint design and development effort between teams at two sites within ADI's Computer Products Division. Project management, algorithm design and development, systems-level engineering, and software-driver authoring were all done by a team in Norwood, Massachusetts. Meanwhile, all IC design and most of the layout were done by a separate team in Austin, Texas. Since the performance of the chip design in Austin needed to be bit-exact with the software simulator developed in Norwood, an extraordinary level of close collaboration was required between the two groups.

Austin team: Rich Greene, Bill Valentine, Will Hooper, Phil Hallmark, Mark Rossman.

Norwood team: David Skolnick, Alex Zatsman, Kevin Leary (project leader).

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Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS

NEW PRODUCT ..... *Circle*

Single-chip 10-bit, 50-MSPS DDS (direct digital synthesis) AD9830 25

NEW LITERATURE

SHARC DSP microcomputer family technical data 44-page data sheet for ADSP-21062/21060 22

Brochure: Signal Processing for Industrial Applications . 23

Application Note: ADSP-2181 IDMA interface to Motorola MC68300 family of microprocessors, AN-415 .. 24

1966 Short-Form Designers' Guide: 228 pages. Includes Selection Trees, Selection Guides, New Products, Military/Aerospace Products, and Appendix (packages, evaluation boards, power supplies, substitution guide, technical publications, worldwide sales directory) 27

IN THE LAST ISSUE

Volume 30, Number 1, 1996, 24 Pages

For a copy, Request 21.

ERRATUM • • • In **Analog Dialogue 29-3 (1995), page 6, Figure 11,** the correct part number for the **ferrite bead is 2677006302.**

PRODUCT NOTES • • • The **ADG608 and ADG609 multiplexers** (8:1 and dual 4:1), for ±5 V, +5 V, and +3 V, are now available in **16-pin TSSOP and narrow-body SOIC** packages. **Rev. A** data sheet is available, **Faxcode* 1912** • • • There are spec changes on the **AD679 complete 14-bit, 128-ksps sampling ADC,** amounting to about 2-dB reduction in min/max dynamic performance. If this is a problem, consult our sales/applications staff • • • **PCMCIA cards:** Hundreds of ADI **products of all types are available in packages thinner than 2.00 mm,** making them suitable for incorporation in PCM(CIA) cards. For suggestions of devices to fit your application, consult our sales/applications staff • • • More than 100 **products of all types are available for single-supply applications,** especially useful in power-saving 5- and 3-volt equipment. Consult the sales/applications staff • • • Cross reference: A 4-page **cross-reference guide to Interface and Supervisory ICs** is available, listing Analog Devices alternatives to other sources. **Circle 26.**

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PATENTS • • • 5,479,130 to Damien McCartney for **Auto-zero switched-capacitor integrator** • • • 5,479,316 to Mark Smrtic, George Molnar, and Jerome Lapham for **Integrated-circuit metal-oxide-metal capacitor and method of making same** • • • 5,480,831 to Craign Core for **Method of forming a self-aligned capacitor** • • • 5,486,720 to Oliver Kierse for **EMF shielding of an integrated circuit package** • • • 5,486,791 to Paul Spitalny and Martin Mallinson for **Programmable gain amplifier** • • • 5,489,854 to Roy Buck and David Tesh for **IC chip test socket with double-ended spring biased contacts** • • • 5,495,200 to Tom Kwan, Paul Ferguson, and Wai Lee for **Double sampled biquad switched capacitor filter** • • • 5,495,245 to James Ashe for **Digital-to-analog converter with segmented resistor string** • • • 5,495,512 to Janos Kovacs and Ronald Kroesen for **Hybrid phase locked loop** • • • 5,497,381 to Geoffrey O'Donoghue and Gary Cheek for **Bitstream defect analysis method for integrated circuits** • • • 5,510,789 to Hae-Seung Lee for **Algorithmic A/D converter with digitally calibrated output.**

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AD7859/54	1874	ADG438F	1855	ADSP-2166	1964	OP493	1858
AD7870*	1370	ADG441*	1513	ADSP-2173	1869	OP495*	1715
AD7870A*	1898	ADG444*	1515	AMP04*	1610	REF19x*	1761
AD7875*	1374	ADG511*	1520	CMP04*	1616		
AD7876*	1375	ADG608/9	1912	CMP401/02	1872		

*Data can be found in 1994 *Design-In Reference Manual.*
†Data can be found in 1995 *DSP/MSP Products Reference Manual.*

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