Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

FILTERING

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DISTORTION

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POWER

HARMONICS

DISSIPATION
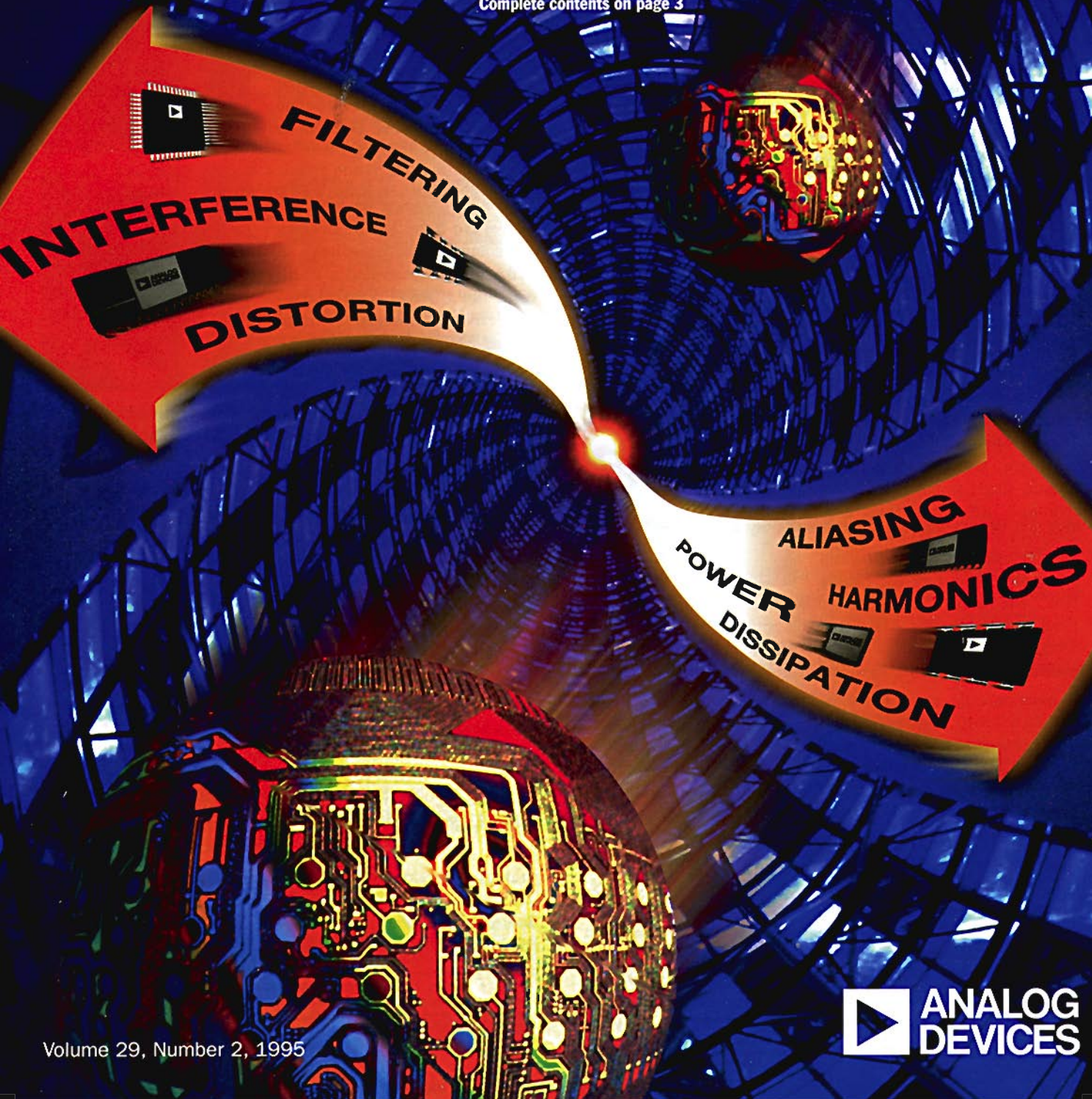
**ANALOG
DEVICES**

Editor's Notes

NEW FELLOW

We are pleased to note that Doug Mercer was introduced as the newest Analog Devices Fellow at our 1995 General Technical Conference. *Fellow*, at Analog Devices, represents the highest level of achievement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their significant technical contributions will have had a major impact on the company's revenue and demonstrated superior creative ability in product- or process technology leading to commercial success.

Other attributes include roles as mentor, consultant, gatekeeper, organizational bridge, entrepreneur, teacher, and ambassador. They must also be effective as leaders of teams and contributors to team effort and in understanding the needs of the customer. Our new Fellow's accomplishments and technical abilities, as well as his personal qualities, well-qualify him for this appointment. He joins Fellows Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980) Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Mohammad Nasser (1993), Wyn Palmer (1991), Richie Payne (1994), Carl Roberts (1992), Paul Ruggerio (1994), Brad Scharf (1993), Mike Timko (1982), Bob Tsang (1988), Mike Tuthill (1988), and Jim Wilson (1993).

DOUG MERCER

Doug Mercer's earliest major achievement at Analog Devices was designing the AD558 DACPORT® (*Analog Dialogue* 14-1, 1980), a complete, monolithic, voltage-output, single-supply 8-bit laser-trimmed μP-compatible D/A converter. He followed this with its ADC counterpart, the AD670, and a complete 12-bit μP-compatible DAC, the AD567. These, and other commercially successful products, including the AD1671 12-bit sampling ADC and—most recently—the AD768 low-glitch DAC, were major factors in maintaining ADI's unchallenged lead in the market for data converters.

In addition to designing products, Doug has contributed strongly to ADI's set of powerful computer-aided design tools and to development of our complementary bipolar (CB) and analog bipolar-CMOS (ABCMOS) processes. He is also a substantial contributor to product-trim technology. He has written papers on converter design and has several patents (received or pending) on bias-current networks, sample-holds, and output switching.

Doug grew up in a "sleepy little resort town," Saratoga Springs, NY, and went to college in Troy, NY, at Rensselaer Polytechnic Institute, receiving a BSEE in 1977. He spent most of his free time at school doing "tech stuff" at the college FM radio station (he had a first-class radio operator's license). After graduation, he joined ADI, a relationship which has led to mutual prosperity. Outside Analog: "When there's snow on the ground I like to ski, and when there isn't snow on the ground, I like to play golf." ▶

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AUTHORS

Steve Cox (*A-D* 28-3, page 4), a Senior Applications Engineer in the Computer Products Division at Analog Devices in Norwood, MA, specializes in Floating Point DSPs. He has a BSEE from Northeastern University. Before joining Analog Devices, he worked at the Naval Underwater Systems Center. In his spare time, he enjoys racing both his road and mountain bikes.
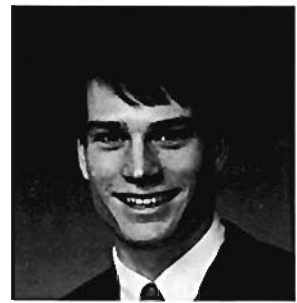
Doug Garde (*A-D* 28-3, p. 5), Design Manager for the SHARC processor family and the ADSP-21020, has been with Analog Devices since 1980. Earlier, Doug was with Hewlett Packard in Loveland, Colorado. He received his BSEE from Melbourne University, Australia. Doug is an avid sailor.

Bill Murphy (p. 3) is a Product Marketing Manager for low-cost, high-speed converters for imaging and communications. He holds an MBA from Babson and a BSEE from the University of Massachusetts at Amherst. Prior to joining ADI, he worked at Prime Computer and Polaroid. His hobbies include running, walking his Keeshound, and (for the moment) helping his wife teach his 8-month-old daughter to walk.

Stacy Ho (page 3) is a Design Engineer in ADI's Video and Image Processing group, Wilmington, MA, working on high-speed data converters. He joined Analog in 1992 after graduating from MIT with a BSEE and an MSEE. In his free time, he enjoys reading and learning to play piano.

Steve Ruscak (pp. 3, 7, 9) is a Senior Applications Specialist in our High-Speed Converter Group at Wilmington, MA. His photo and a biographical sketch appear in *Analog Dialogue* 29-1.

Cover: The cover illustration was designed and executed by **Shelley Miles**, of *Design Encounters*, Hingham MA.

New High-Speed, Low-Power Data-Acquisition ICs

Novel designs, faster processes, and single-supply operation make available a wide array of applications

by Will Drachler and Bill Murphy

Applications for high-resolution data converters and op amps operating in the multi-megasample-per-second region are rapidly increasing as cost, size, and power demand decrease. Between the covers of this special "High Speed" issue of Analog Dialogue, you can read about some of the applications they make possible, about test methods for noise and settling time—and (the focus of this article) some things you ought to know about typical leading-edge devices to help you better use them.

The recently introduced AD8011 op amp* and AD876 sampling analog-to-digital (A/D) converter* make available high-speed and accurate data acquisition at reduced power and cost. Together, they can deliver 10-bit, 20-MSPS data conversion using < 165 mW at prices attractive to designers of consumer equipment. This performance is available using a *single +5-V supply* (read about the AD8011 and AD876 in the sidebars on pages 4 and 6).

Historical Perspective: Over the last two decades, the design and manufacture of high-speed (>1 MSPS) ADCs and op amps has changed drastically. Figure 1 shows A/D converter cost reduction—represented by mW/MHz—in the past 10 years. Such major reductions are driven by evolving market forces, which have shaped the electronics industry over the past two decades.

In the mid-1980s, the Cold War was the major driver of progress in electronic devices and equipment. Military contractors—the technically leading customers—needed high performance, *plus* hermetic packages, stringent shock and vibration specs, thermal cycling, and radiation hardness—and cost seemed no object.

With monolithic ICs not yet available, vendors were driven to either card-mounted kludges or hybrid assembly. But such manufacturing processes were expensive, requiring a high degree of human assembly and extensive testing at each step. Large hermetic packages were expensive; military certification required time, technology, manpower, and extensive record-keeping.

The first monolithic 10-bit-or-better high-speed ADCs appeared by about 1990. The AD9020, culmination of an evolving series of IC pure flash converters, offered a huge reduction of size and power compared to the 5"×7" card-mounted CAV1020 10-bit, 20-MHz ADC. Low power consumption was achieved by an innovative flash architecture, employing half the number of comparators required by conventional flash architectures.[1]

Power consumption had to be low to keep equipment from getting too hot and to minimize thermal drifts. 2.8 W was considered "low power." The major applications—radar warning and guidance, digital oscilloscopes, medical imaging, infrared systems, and professional video could be line-powered.

[1]See Analog Dialogue 24-1.

*Analog Dialogue 29-1, pp. 7, 19. Use the reply card for technical data on these devices. Prices (1000s) start at $1.95 (AD8011) and $9.95 (AD876). **Circle 1**
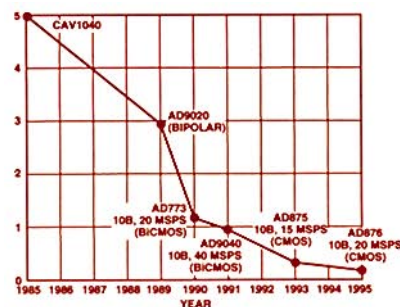

Figure 1. Trends in high speed ADC power consumption (mW/MHz).

But the '90s explosion of battery-operated equipment (camcorders, cellular telephones, portable computers, etc.) has led to a rapidly increasing need for designers to reduce power consumption. To meet these needs, a new ADC architecture emerged. Multi-stage pipeline converters (1990) employed a BiCMOS process, which allowed sample/holds to be incorporated on the monolithic chip. ADC suppliers could increase performance and reduce both power consumption and cost. In 1993 the AD875, the first 1-µm CMOS 15-MSPS ADC, helped reduce camcorder size & power.

Now, two years later, a new generation of small-geometry devices includes the CMOS AD876 A/D converter and the XFCB (extra fast complementary bipolar) AD8011 op amp. Lower junction capacitance reduces power and allows higher speed at lower voltage; and small die size leads to a cost structure well-suited to demanding consumer products. Single-supply avoids cost, size, and weight of additional supplies. This improvement coincides with the shift of application focus from military to commercial and consumer. Examples: in portable video cameras, high performance, low cost and long battery life are vital needs; in communications equipment, such as cable set-top boxes, speed and resolution are vital for decent-quality video from the receiver; but to succeed, the equipment must be offered at low cost.

APPLICATION EXAMPLE—ADC Driver

by Steve Ruscak

With each new generation, performance improvements are often accompanied by practical requirements the user must adhere to for the best performance from an op amp or a converter. Older-generation op amps often required external compensation to tailor response; flash A/Ds are fast but are power-hungry and have low input impedance. BiMOS converters simplify applications issues; the typically high-impedance, benign input structures are easy to

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drive. High-speed CB op amps and CMOS, switched-capacitor-based converters minimize power consumption and price. An application where an AD8011 op amp drives an AD876 A/D shows strengths and practical issues of new-generation ICs.

High-speed, switched-capacitor A/D architectures require the user to understand a unique set of issues when designing interface circuitry. The optimum interface depends on whether the application requires only low distortion and spurs (*dynamic* characteristics), low *noise*, or *both* low noise and low distortion.

- Systems where the entire signal chain (series of functional elements that process the signal) must optimize specs like total harmonic distortion (THD) and spurious-free dynamic range (SFDR)—for example, communications systems—typically involve spectral analysis or processing. Input signals change in relatively small increments between samples; signal content is confined to < Nyquist frequency (i.e., 1/2 the sampling rate).

- Systems focused on *noise* performance may sacrifice THD and SFDR to increase dynamic range (SNR). Though distortion specifications may not be as important in these low-noise applications (such as CCD-based imaging), wide bandwidth and fast transient response may be needed to insure fast settling.

- Data-acquisition systems, such as DSOs—digital sampling oscilloscopes—typify applications that require both low spurs & distortion *and* wide dynamic range (SNR). Besides voltage and current noise, *phase* noise, such as that generated from aperture jitter, is of concern. These systems often deal with a wide variety of signals, performing spectral signal processing and handling large-scale transients (typically from multiplexed front-ends).

Driving switched-capacitance ADC inputs: The input *hold* capacitor of the AD876 (see sidebar, page 6) must be charged to the new input voltage each clock cycle. The amount of charge the input driver must supply depends on the difference between the voltage stored on the *hold* capacitor from the previous conversion and the voltage applied to the A/D when the sample clock transitions from *high* (hold mode) to *low* (track). The smaller this difference, the less incremental charge is needed. On the other hand, for a full-scale change between conversions, the input driver must supply a large increment of charge. The circuit of Figure 2, with an AD8011 driving the AD876, illustrates performance options. Regardless of how the op amp itself is configured, adding a series resistor (and possibly a shunt capacitor) can improve performance of the op amp/converter pair.

To examine some of the considerations for selecting optimum-value resistors and capacitors for a particular application, the AD8011 was configured in a gain of +2 (bandwidth of about 180 MHz) and connected to the AD876 input as shown.
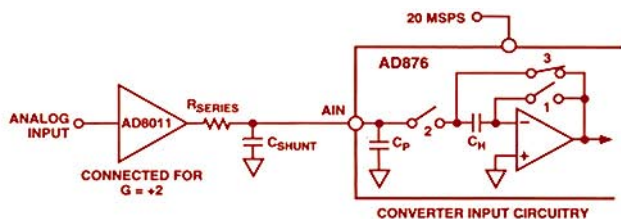
Figure 2. Driving a sampling ADC that has a switched-capacitor sample-hold.

The AD8011's excellent performance (table) and power economy are due to a unique two-gain-stage current-feedback architecture (Figure A1) and fabrication on Analog Devices's bonded-wafer extra-fast complementary bipolar (XFCB) process.

A1. AD8011 BASIC ARCHITECTURE. FEEDBACK CONNECTION FOR GAIN = 1 + R_F/R_{IN}.
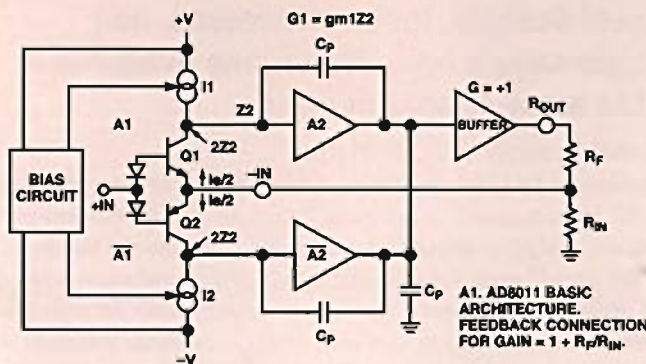
AD8011 PERFORMANCE

Supply voltage(s)	+5 V	±5 V
Supply current, max	1 mA	1.2 mA
Quiescent power	5 mW	12 mW
Bandwidth, –3-dB, small-signal, typical		
G = +1	325 MHz	400 MHz
G = +2	180 MHz	210 MHz
Bandwidth, –3 dB, 2.5 V p-p out, typical		
G = +10	57 MHz	57 MHz
0.1-dB gain flatness	20 MHz	25 MHz
Slewing rate, typical, G = +2	2000 V/μs	3500 V/μs
Settling to 0.1%, 2-V step, G = +2	29 ns	25 ns
Distortion: 2nd, 3rd, R_L=1 kΩ		
5 MHz	–84, –76 dB	–75, –70 dB
20 MHz	–59, –53 dB	–62, –63 dB
ΔGain error: R_L = 1 kΩ, 150 Ω	0.02%, 0.6%	0.02%, 0.02%
ΔPhase error: R_L = 1 kΩ, 150 Ω	0.06°, 0.8°	0.06°, 0.3°
Voltage noise @ 10 kHz, typical	2 nV/√Hz	2 nV/√Hz
Offset voltage, max	5 mV	5 mV
Output current available, typical	30 mA	30 mA
Input range	1.2 to 3.8 V	±4.1 V
Output swing, R_L = 1 kΩ	0.9 to 4.1 V	±4.1 V

What is a current-feedback amplifier? A current feedback, or *transimpedance*, op amp (CFA) is used in circuits that look much like the circuits that employ voltage feedback op amps (VFAs). What is the difference? First, the negative input of a CFA responds to current; the output voltage is proportional to that current, hence *transimpedance* ($V_{out} = Z_t I_{in}$). Instead of keeping the negative input current small by maintaining high input impedance, and using feedback and voltage gain to keep the input voltage difference small, the CFA keeps the voltage difference small by virtue of its *low* input imped-ance (like looking back into a low-offset emitter follower); and it keeps its net input current small dynamically by feedback from the output.

When an ideal CFA is driven at the high-impedance positive input, the negative input, with its low impedance, follows closely in voltage; and the high gain for error current and the negative feedback through R_f require that the currents through Rf and Rin be equal; hence $V_{out} \cong V_{in}[R/R_{in} + 1]$, just like for voltage-feedback amplifiers. A major difference is that the slew rate can be quite high, because large transient currents can flow in the input stage to handle rapid

FEEDBACK AMPLIFIER

Drachler

changes in voltage across the compensating capacitor(s). Also, the low impedance at the negative input means that stray input capacitance will not substantially affect the amplifier's bandwidth.

How does the AD8011 differ from conventional current amplifiers? Conventional IC current-feedback op amps, though built on complementary-bipolar processes, have been limited to a single gain stage, using current-mirror circuits for biasing and level-shifting (Figure A2a). Until now, fully complementary, two-gain-stage, current-feedback IC op amps have been impractical because of their high power consumption.


A2a. TYPICAL SINGLE-STAGE
CURRENT-FEEDBACK OP AMP.

A2b. AD8011 TWO-STAGE
CIRCUITRY
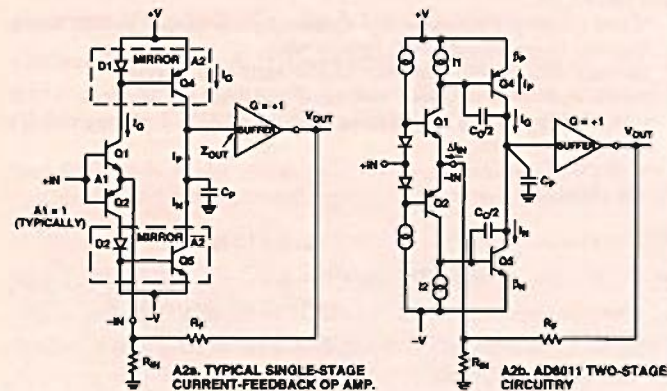
The AD8011 employs a second gain stage consisting of a pair of complementary amplifiers, A2 and $\overline{A2}$, exemplified by Q4 and Q5. The detailed design of current sources I_1 and I_2, and their bias circuit, are the (patent-applied-for) key to the success of the two-stage circuit; they keep the amplifier's quiescent power low, yet are capable of wide current excursions during slewing. Voltage developed at the output of the transconductance stage of a current-feedback amplifier (the high-impedance "C_P" node) is unloaded by the unity-gain buffer to provide output drive.

A further advantage of the two-stage amplifier is the higher overall gain-bandwidth (for the same power), which means lower signal distortion and the ability to drive heavier external loads. Conversely, the second gain stage divides down the drive required by the buffer, as well as its nonlinearities, resulting in lower distortion and higher open-loop gain. The AD8011 retains the advantage of current-feedback amplifiers that higher closed-loop gains do not involve a proportional reduction in bandwidth. Finally, the amplifier's wide common-mode and output ranges permit it to operate on a single 5-volt supply, with half the power and little degradation of performance over ±5-V operation.

Summing up, the novel bias circuit keeps the complementary currents equal and low—regardless of beta differences—albeit at the expense of slightly greater circuit complexity. However, the XFCB process permits fabrication of very small, fast transistors, so the die remains small (and the cost low). The AD8011's use of the second gain stage and the bias circuit provides it with all of the advantages of class-B operation, from input stage to output stage. It makes possible low distortion, high-speed, and high output current drive while running on low quiescent current.

Figure 3a shows the test signals: The top trace is the analog input to the AD8011, a 1-V p-p square-wave. The bottom trace is the AD876 sample clock. When the clock is low, the SHA tracks the input; when it goes high, the A/D's SHA switches to Hold. Note that the AD876 must acquire a full-scale change in input voltage each conversion; this condition places the most severe demands on the AD8011, since it must supply the maximum amount of charge each conversion period. The AD8011 cannot supply the Δcharge instantaneously, so there are transients at the converter's input during the transitions of the A/D sample clock.
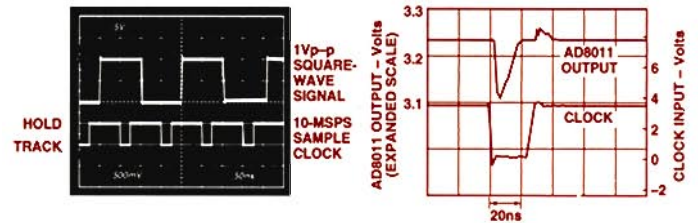

a. Input square wave and
10-MSPS sample clock.

b. Typical amplifier output
transient during sampling
of +FS input.

Figure 3. Input waveforms.

Figure 3b shows the transients while the input square wave is at its positive excursion on an expanded scale (upper plot), with the 25-ns track-mode clock pulse. The smaller rising-edge *hold* transient is unimportant; it occurs long before the next sample is taken. The falling-edge transient, as the ADC acquires the full-scale charge change, is about −114 mV; recovery and settling to 0.1% (10 bits or 2 mV) must take place within the duration of the track-mode pulse and prior to the rising edge—here, it occurs in 20 ns with a 100-Ω resistor. For a 20-MSPS sample rate (50% duty cycle), recovery must be within 25 ns. A slower amplifier could be used for lower sample rates.

Series resistors help: Most applications benefit from series resistance between the AD8011's output and the AD876's V_{IN} pin to isolate the output stage of the AD8011 from the input capacitance of the AD876, and to limit the peak current the op amp must supply. As little as 33 Ω (Figure 4a) greatly reduces THD (from −47 to −64 dB) and increases SNR (from 58 to 60 dB) and SFDR (from 48 to 68 dB); up to 500 Ω can be used without increasing distortion due to the nonlinear capacitive load. Settling time is also improved by small series resistance; without it, the ADC's capacitive load directly applied at the amplifier's output causes some peaking in the amplifier's response and slower settling. But increased resistance—considering the ADC's input capacitance, strays, and any added capacitance—reduces bandwidth through low-pass filtering. 500 Ω and 20 pF has a −3-dB frequency of about 16 MHz.
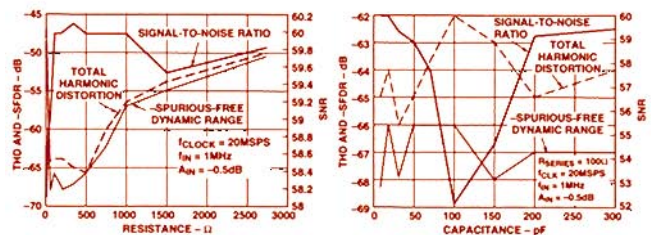
a. THD, SNR, SFDR vs.
series resistance.

b. THD, SNR, SFDR vs.
shunt capacitance.

Figure 4. Distortion and noise of converter and amplifier circuit.

Shunt Capacitance Limits Noise: The AD876 has a full-power bandwidth of at least 150 MHz and an even greater noise bandwidth. Wideband incoming noise at frequencies > 1/2 the sampling rate will be aliased back to baseband and will decrease the SNR of the digitized signal. For noise-sensitive applications, a shunt capacitor, with the series resistor (Figure 2) provides filtering of high-frequency external noise at the AD876 input.

Figure 4b shows noise and distortion using a 100-Ω series resistor and various shunt capacitances. SFDR is relatively unaffected, holding in the 66 to 68-dB range. However, for capacitances in the range from 50 pF to 200 pF, THD increases substantially (from –65 to –62 dB) and SNR decreases substantially (from 59 to as low as 52 dB). The reduced SNR is caused by aliasing of high-order harmonics due to glitching of the not-quite-settled hold-to-track transient; they show up as noise in the baseband signal at the output of the AD876 under the conditions of 4b.

For higher values of shunt capacitance, the SNR greatly improves, but at the cost of bandwidth. With (say) 200 pF, the overall system –3-dB bandwidth decreases to about 8 MHz—and any fast transients in the input signal may not settle to 10-bit accuracy in a single conversion period.

When using series R and shunt C to optimize system behavior, it is important to take into account the application's goals. If dynamic performance is paramount over a wide range of input frequencies, it is probably best to keep the shunt capacitance below 20 pF with a 100-Ω series resistor. If you want to optimize noise performance, consider longer RC time constants and whether transient response can be traded for low noise. In any case, best performance occurs when the input is given time to settle to 10-bit accuracy prior to the track-to-hold transition of the AD876 sample clock. Keep in mind also that the AD8011 is so quiet that wideband noise can be filtered at an earlier stage without concern that AD8011 noise will degrade SNR. ▶

REFERENCES
1. "Drive circuitry is critical to high-speed sampling ADCs," by Walt Kester. *Electronic Design*, November 7, 1994, p. 43.
2. Technical data, AD8011 and AD876. Use reply card. **Circle 1**
3. *System Applications Guide.* Norwood MA: Analog Devices (1993), p. 16-12, "Techniques For Verifying High-Speed ADC Performance". Use book purchase card.

A PIPELINED CONVERTER (AD876)

by Stacy Ho

The AD876, a CMOS A/D converter circuit, uses switched-capacitor techniques to combine low cost and low power. Figure B1 shows a conceptual block diagram of the AD876. The input is sampled at the front-end by a sample-and-hold (S/H) circuit, which also provides single-ended-to-differential conversion for the A/D's differential circuitry. The device's overall dynamic performance and wideband noise are established at the S/H stage. The conversion, accomplished by a 4-stage pipeline, is iterated by several subblocks that refine the conversion with increasing resolution as they pass the residues from stage to stage.

Each stage performs a flash A/D conversion; converts the result back to analog (D/A), subtracts it from its input, amplifies and holds the difference for the next stage. The digital results are combined via correction logic; and data is converted at the clock rate (but the output at any specific instant has a latency of 3.5 clock cycles (i.e., it represents a 3.5-cycle-earlier input value).


PIPELINED A/D CONVERTER
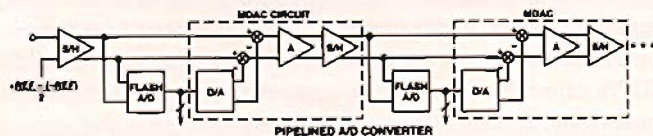
Following each A/D conversion step, the D/A and other analog functions are all implemented in a compact and efficient switched-capacitor circuit. The functions of this circuit, basically a multiplying D/A converter (MDAC), are shown within dashed blocks in Figure B1. Taking a closer look at the MDAC circuit, Figure B2 illustrates its basic operation. When CLOCK is low, the input voltage, V_{IN}, is sampled onto an array of identically sized unit capacitors (amplifier gain=1). When CLOCK goes high, a feedback capacitor is connected around the amplifier. The charge on all the capacitors in the input array is transferred onto the feedback capacitor, resulting in a voltage gain that is the ratio of the number of capacitors in the input array to the feedback cap. At the same time, the input array capacitors are switched to either the positive or negative reference (as selected by the digital results of the A/D conversion), and their sum is

thus subtracted from the V_{IN} sum, leaving at the amplifier's output an amplified residue, which is held as an input to the next stage. Thus the gain, D/A, differencing, and S/H have all been wrapped up into one block.

MDAC OPERATION

CLOCK LOW   CLOCK HIGH
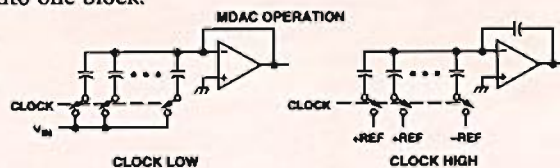
Like the MDAC, the input S/H is implemented as a switched-capacitor circuit, as shown (single-ended for simplicity) in Figure B3. When CLOCK is low, the hold capacitor is connected to the input and is charged up to the input voltage by an input driver (typically an op amp such as the AD8011). When CLOCK goes high, the cap is disconnected from the input and fed around to the output of the amplifier. Since the node that connects to the input of the op amp is now floating, no charge can escape and the input voltage is held. When CLOCK goes low again, the cap is reconnected to the input. If there is a difference between the voltage already stored on the hold capacitor and the voltage at the AD876 input, the capacitor is charged to the new value (after a transient glitch which the op amp must handle, as noted in Applications).

CLOCK LOW   CLOCK HIGH
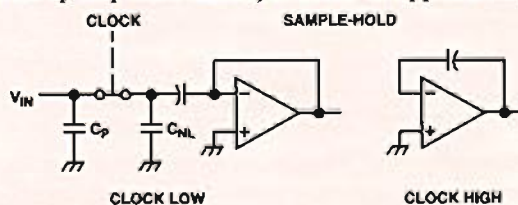
The reference inputs are being switched in the same way as the inputs. Care must be taken to minimize transients in the reference circuit, for example, by using external capacitors to source or sink transient reference currents. Note also that the AD876 differential input range (after the S/H) actually spans between two references, the bottom (or 'negative') reference and top (or 'positive') reference, to accommodate single +5-V-supply systems.

Using Histogram Techniques to Measure A/D Converter Noise

by Steve Ruscak and Larry Singer

This article describes a technique for using histograms to determine the rms noise of an A/D converter, referred to the input. It can complement the popular qualitative approach of evaluating A/D converter performance by applying a dc analog voltage and observing "code flicker" at the A/D's digital output.

Collect Data With A Histogram: A dc histogram reports the number of times each code appears at the output of the A/D converter. Here is a procedure to produce a histogram:

• Connect a "clean" dc source to the analog input of the A/D converter (and a "clean" reference, if an external one is used).

• Record the results of a large number of conversions, depending on the expected noise. One-to-two million conversions are usually more than adequate for a low-noise A/D.

• Sort the conversions into code "hits." The core of the histogram is essentially a bank of counters (or *bins*); there is one bin corresponding to each possible digital output of the A/D converter. After each conversion, the digital code at the A/D output is determined (by hardware or software) and the corresponding counter is incremented. If an ideal (noiseless) A/D were connected to a dc voltage, the histogram of *n* conversions would indicate *n* code 'hits' in the bin corresponding to the digital value of the dc input. All other bins would equal zero.

While the ideal A/D only produces code hits in a single bin, an actual A/D will produce additional codes outside the main bin for any dc input value, due to the presence of noise. The number of codes that fall outside the main bin is the key to measuring the converter's rms noise. Avoidance of an additional effect at certain codes due to differential nonlinearity will be discussed later.

Understand Noise Sources: The three dominant sources of A/D noise are *quantization*, *ac* (phase noise, or jitter in sampling of ac signals), and *wideband* (white noise, digital feedthrough, etc.). The last one is the most amenable to dc histogram testing. Quantization noise is a large contributor to the signal's error power,
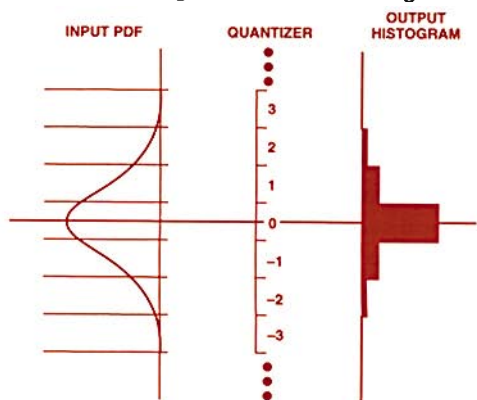
but (in the absence of drift during the measurement) it does not cause multiple code "hits" to show up in a dc histogram. AC noise, resulting from aperture jitter, is also not a factor when the input signal is dc. The remaining source, wideband noise, is the major input-referred noise component measured by the histogram technique.

What are our important assumptions? First, that the model for the A/D is an ideal quantizer with a Gaussian noise source added to the input of the device. The measurement will be somewhat erroneous if the dominant noise source is non-Gaussian; for example, digital feedthrough tends to be code and signal dependent. Second, the architecture of the device affects the measurements; but the technique is valid for the majority of high-speed, pipelined converters available from Analog Devices.

Determine RMS Noise Graphically: How do the histogram and noise relate to one another? Figure 1 shows a Gaussian input to an ideal quantizer and a histogram of the corresponding output. The probability density function (PDF) of the input shows that the majority of the output codes will occur in a single bin, but there must be additional codes corresponding to the tails of the distribution. The fraction that occurs outside the main code depends on the spread, or standard deviation, σ, of the noise distribution.

Figure 2 is a plot of a PDF for A/D input noise in which σ corresponds to the least significant bit (LSB) of the converter under test. The dc input to the A/D is adjusted to center the PDF on the midpoint of code *k*. After quantization, noise is measured by the fraction of codes occurring outside the main bin, equal to the ratio of the area of the shaded tails to the total area under the curve. With the analog input on a code center, the boundaries of the shaded area occur at ±0.5 LSB away from the code center.
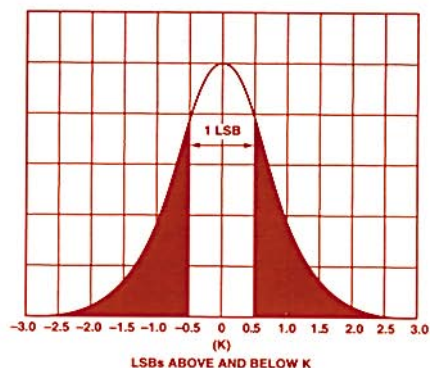
Figure 2. A Gaussian distribution scaled in LSBs about the mean.

For a symmetrical Gaussian PDF, the equation[1],

$$P = \frac{1}{\sigma\sqrt{2\pi}}\left[\int_{-\infty}^{-0.5\,LSB} e^{-x^2/2\sigma^2}\,dx + \int_{+0.5\,LSB}^{+\infty} e^{-x^2/2\sigma^2}\,dx\right]$$

$$= \frac{2}{\sigma\sqrt{2\pi}}\int_{-\infty}^{-0.5\,LSB} e^{-x^2/2\sigma^2}\,dx \tag{1}$$

expresses the probability of getting a code outside the main bin for that PDF. The terms inside the integral are simply the expression for a Gaussian distribution with unit area and standard

Figure 1. Quantization of a probability distribution.

[1]Drake, Alvin W., *Fundamentals of Applied Probability Theory*. McGraw-Hill Book Company, 1967

deviation, σ. Integrate from −∞ to −0.5 LSB to find the area under one tail, and from +0.5 LSB to +∞ for the other. By symmetry, one can simply multiply the area under one tail by 2.

To ultimately determine the A/D's noise, equation (1) must be solved for σ, with P determined from the histogram as the fractional portion of code "hits" outside the main bin. Unfortunately, the integral has no closed form solution in terms of σ. One option is to iterate σ and numerically evaluate equation (1) until the solution equals the fraction determined from the histogram. Alternatively, we can fix σ, iterate the upper limit of integration, plot the result as a graph, and use it to find the upper limit that corresponds to any value of P. Figure 3a is a plot of:

$$F = \frac{2}{\sigma\sqrt{2\pi}} \int_{-\infty}^{x} e^{-z^2/2\sigma^2} dz \qquad (2)$$

with σ equal to unity. For each point, x, it has been integrated and the fractional value, F, determined. Since we already know the value of F (= P) from the histogram, we can simply find the x-axis point, x_0, corresponding to P, from Figure 3a. This value is equivalent to having evaluated equation (1) from −∞ to −0.5 LSB, had we known the correct value for σ. To calculate the rms noise of the converter, simply solve the equation

$$-x_0 \, \sigma = 0.5 \, LSB \qquad (3)$$

The procedure's simplicity can be demonstrated with an example. Suppose that the fraction of codes outside the main bin equals 0.0027. Using Figure 3b, a magnified version of 3a, find 0.0027 on the y-axis [these values can also be found from a standard normal curve, or z-Table for the area under the unit normal distribution]. The corresponding intercept on the x-axis, x_0, is −3. Solve equation (3) for σ, the rms noise (= 0.167 LSB).

Figures 3a and 3b relate rms noise and code histogram values. Do a histogram, find the fraction of codes that occur outside the main bin, look up that number on the y-axis of 3a or 3b, and read off the x-axis value. Dividing 0.5 LSBs by this number gives the rms noise in LSBs.
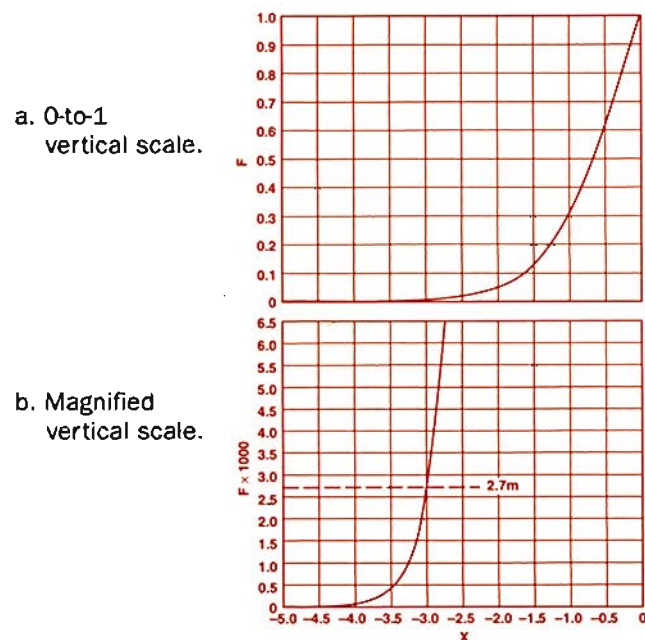

a. 0-to-1 vertical scale.

b. Magnified vertical scale.

Figure 3. Plots of F vs. x for equation (2).

On The Bench: There are some practical rules to follow when setting up the test fixture. First, use a dc source with noise below the level being measured. Then, using several conversions, set the analog input squarely on the center of the code (i.e., mid-way between adjacent transitions). This should make the side bins approximately equal in size, important for the symmetry assumption in using the above analysis. This also maximizes the number of code hits occurring outside the main bin(s), resulting in a statistically more-significant measurement. For example, if the input is centered on the *transition*, the histogram produces two 1-LSB-wide main bins with approximately equal numbers of code "hits", including some of the hits that would have appeared in the bins adjacent to a 1-LSB-wide centered main bin.

Determining the noise of the converter is useful for making a comparison, either to a specified requirement or to another A/D converter of the same, or different type. Figure 4a shows a typical histogram generated from the AD872A 12-bit, 10-MSPS A/D converter. All the codes appear in either the main bin or the two adjacent bins, roughly symmetrically disposed. From the histogram, the ratio of the 34,729 code hits outside the main bin to the 652,790 total number of codes counted is 0.053. From Figure 3a, the x-value corresponding to 0.053 on the y-axis is approximately 1.9 σ. From equation (3), 1.9 σ = 0.5 LSBs, and the rms noise (σ) equals 0.26 LSBs rms.

a. AD872A, sampled at 10 MSPS.
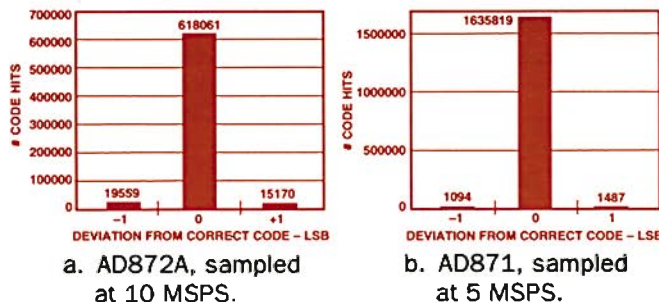
b. AD871, sampled at 5 MSPS.

Figure 4. Typical histograms for two A/D converters with dc input.

For comparison, Figure 4b shows a histogram of the AD871, a 12-bit, 5-MSPS high-speed A/D converter. Using the same procedure, the hit ratio is 2,581/1,638,400, about 0.0016, and the input-referred noise of the AD871 is thus 0.5/3.17, or 0.16 LSBs rms. With low-noise A/Ds, like the AD871, the test should be run long enough to acquire enough code hits *outside* the main bin in order to obtain a credible noise measurement.

DNL May Skew The Measurement: While the histogram measurement technique assumes an ideal quantizer, differential-nonlinearity (DNL) errors will influence the measurement. DNL, a measure of A/D converter code width, expresses the difference between an actual code width and the ideal width of 1 LSB; it is positive for a wide code, negative for a narrow code. It tends to be worst at major transitions, e.g., from 011...11 to 100...00. If the code is wide, the noise measurement will be optimistic because the main bin will contain more hits. If a code is narrow, the noise measurement will tend to be on the high side (however, since missed codes are the ultimate case of excessively narrow codes, the measurement is conservative). The easiest way to circumvent this problem is to compute σ at several points along the transfer function—avoiding major transitions, wide codes, and narrow codes—and then average the results. ▶

Single-Supply IF-Strip Digitizes QAM Signals

by Bob Clarke, Paul Hendriks, and Steve Ruscak

Quadrature amplitude modulation (QAM) and quadrature phase-shift keying (QPSK) systems abound. In quadrature schemes, two independent signals ("in-phase" and "quadrature") are transmitted via a single carrier, making use of the orthogonality of signal components at 90°. Cellular standards, such as the international GSM standard, the US IS54, IS95, and IS136 standards, and the Japanese PHS, all require I/Q demodulation in some form. Other applications for QAM or QPSK include CATV set-top-box converters and hybrid fiber/coax video transmission.

Two common demodulation schemes for QAM and QPSK IF signals are quadrature (I/Q) demodulation and direct digitizing. In quadrature demodulation, a pair of mixers driven in quadrature demodulate the IF into its baseband I and Q components; they are then digitized by a pair of A/D converters. In direct digitizing, a single A/D converter samples the IF, eliminating a down-conversion; the digitized IF is then demodulated digitally.

Direct digitizing can be implemented with a handful of passive elements and four low-cost ICs: the AD607* IF Subsystem [see the sidebar for details], developed for cellular radio applications, the AD876* 10-bit, 20-MSPS A/D converter, and two AD8011* op amps. The system (Figure 1) provides a 45-dB spurious-free dynamic range (SFDR) over a 4-to-6-MHz bandwidth for such applications as CATV and hybrid fiber/coax; it can demodulate 64 [8×8] QAM and 256 [16×16] QAM with a low bit error rate (BER).

The signal chain: The key components of the integrated solution are the AD607 IF Subsystem, and the AD876 A/D converter, plus an active filter tailored for the application.

A typical input to the IF strip is from a surface-acoustic-wave (SAW) filter that establishes the system bandwidth and filters out adjacent channels. The AD607's first stage down-converts the input from a 45-MHz first IF to a 5-MHz second IF, using a 40-MHz local oscillator (LO). The spectrum at the output of the AD607's mixer (MXOP) contains the desired demodulated IF frequency

$(f_{in} - f_c)$, and an image frequency $(f_{in} + f_c)$. The mixer's output is passively low-pass filtered by a three-pole, 7-MHz, Chebyshev filter,† comprising a two-pole LC stage that feeds the AD607's amplifier strip, plus a single-pole RC stage at the IFOP output.

Because of the high gain and bandwidth of the AD607's IF amplifiers, some filtering is necessary to limit noise and prevent aliasing in the AD876. The last stage of the Chebyshev, the simple RC section, limits the noise bandwidth of the IF strip to about 10 MHz. A 3rd-order Butterworth high-pass filter [U3 and U4] further reduces low-frequency noise. U3's 14-dB ac gain amplifies the ±100-mV (–10 dBm) IFOP signal from the AD607 so that peak signals span the AD876's full input range.

The input to the AD876 is ac-coupled; this level-shifts the signal to the A/D's nominal input range and avoids concerns about headroom at the output of the AD8011 with a single supply. The AD876's reference voltages, generated by a simple resistance network, set the boundaries of its input range. R1 and R2, in conjunction with the 250-Ω resistance ladder inside the AD876, provide 3.5 & 2.5-V reference voltages at REFTF and REFBF.

The 40-MHz local oscillator frequency is halved to provide a 20-MSPS sample clock for the AD876. Oversampling the analog input simplifies filtering of the output by the digital processor.

Distortion Analysis: Figure 2 shows measured output spectra at the extremities of an assumed input range of –35 dBm to –55 dBm. To predict the level of intermodulation distortion (IMD), the system is analyzed for both the minimum and maximum expected signal levels. To simplify the analysis, the effects of a low-noise amplifier (LNA) are not included. However, many systems would include an LNA at the front end to increase the signal-to-noise ratio.

The IMD for the AD607 is predictable and increases as signal levels increase. The third-order intercept specification of the AD607 indicates that performance will remain acceptably linear over the above input signal range. The amplitudes of the third-order products are generally the most important; they lie close to the input signal frequencies and are not removed by filtering. The calculated third-order intermodulation products should remain at least 45 dB below the fundamental for signals up to –27.5 dBm. Because the spurious-free dynamic range from the AD8011s and the AD876 is typically greater than 60 dB, they do not contribute substantially to the overall noise and distortion.
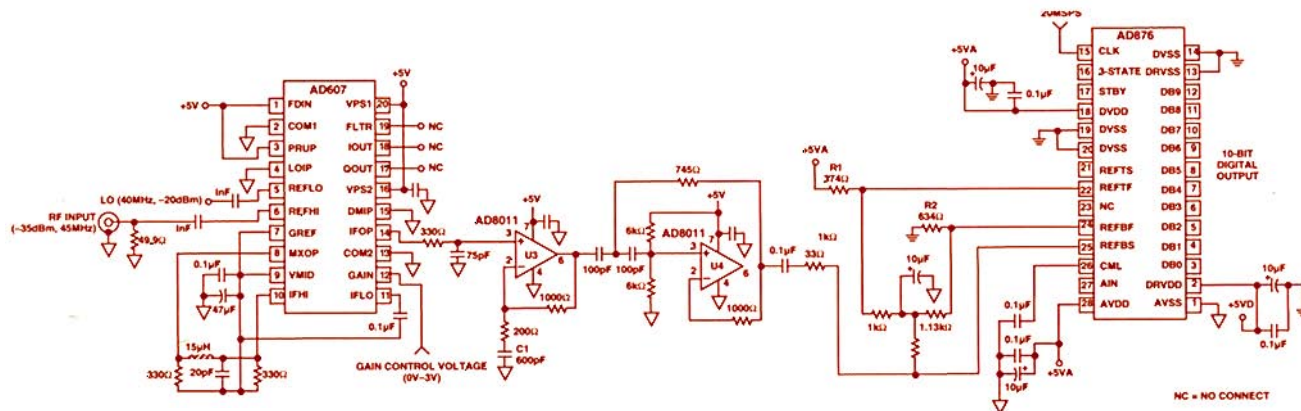

Figure 1. Schematic of direct IF-to-digital converter.

*Use the reply card for technical data. **Circle 2** for AD607 (prices begin at $5.95 in 1000s), **Circle 1** for AD8011 and AD876.

†The phase distortion introduced by the Chebyshev filter may be a problem in systems without some form of equalization.

The table summarizes the individual gains and cumulative levels at each stage for the max and min signal levels. It can be used for analyzing the effects of gain distribution on IMD and noise.

	Signal	Mixer	Mixer gain	Low-pass	IF amps	Low-pass	High-pass
Stage gain (dB)	Max	–6	7.9	–3	26.1	0	14
	Min	–6	13	–3	41	0	14
Cumulative gain (dB)	Max	–6	1.9	–1.1	25	25	39
	Min	–6	7	4	45	45	59
Level (dBm)	–35	–41	–33.1	–36.1	–10	–10	4
	–55	–61	–48	–51	–10	–10	4

Measurement of Performance: Communication systems use specialized tests, such as bit error rate (BER) and spectral analysis (FFT) to provide a figure of merit for receiver distortion performance. Figure 2 shows the 8-k FFT of the AD876 output resulting from a two-tone input at 45.02441 and 45.39056 MHz (IF outputs at 5.02441 and 5.39056 MHz) for the minimum and maximum signal levels. Shown are the (numbered, aliased) harmonics of the 5.39056-MHz signal, plus other related spurs. The SFDR for the entire system can be seen. All spurious tones are at least 47 dB below the fundamentals. The dominant spurious components are the 3rd and 5th order IMD products. ▶
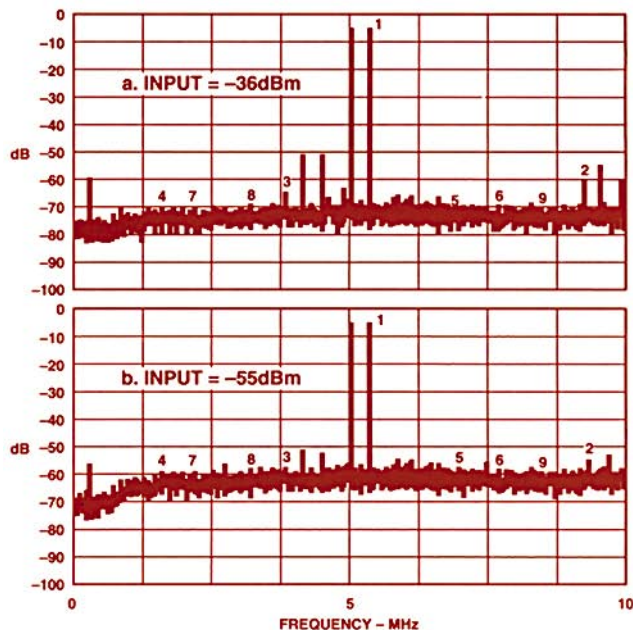

Figure 2. Two-tone FFTs of IF strip.

AD607 ARCHITECTURE

The AD607 comprises a mixer with a LO preamp, a linear IF strip with voltage-controlled gain, dual (I & Q) demodulators, each followed by a 2-pole, 3-MHz low-pass filter, and a phase-locked voltage-controlled quadrature oscillator to provide the in-phase and quadrature clocks, as well as an on-board peak detector and AGC loop with a received-signal strength (RSSI). The IF strip's output is available for insertion of a low-pass or bandpass filter for noise reduction and/or an A/D for direct digitizing, as in Figure 1.
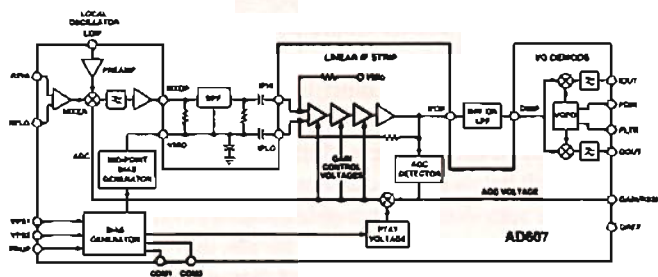
The signal path begins with the mixer. Although most IFs are in the 45 to 300-MHz range, it can accept inputs as high as 500 MHz. Its input-referred 1-dB compression point is –15 dBm (or ±54 mV, regardless of input termination) and its input third-order intercept point (IIP3) is –8 dBm. Both are measured with a 50-Ω source and 50-Ω input termination.

The mixer provides a high-impedance current output to drive a parallel-terminated filter; this avoids a 6-dB (voltage-mode) series termination loss. The conversion gain is specified for operation into an IF band-pass filter (BPF) load of 165 Ω, i.e., a 330-Ω filter doubly shunt-terminated and assuming a local oscillator drive at LOIP of at least –16 dBm (±50 mV, regardless of input termination). The IF signal voltage at pin MXOP can swing 2 V p-p when using a 3-V supply; the high headroom minimizes the likelihood of significant intermodulation from adjacent-channel and other strong interfering signals at the mixer output.

Both the mixer's conversion gain and the IF amplifier gain (dB) are proportionally controlled by the voltage, V_G, at pin GAIN/RSSI. The gain of all sections is maximum when V_G is zero, and decreases, reaching a minimum at $[V_P – 0.8$ V], where V_P is the supply voltage; for example, $V_G = 2.2$ V for $V_p = 3$ V. Gain-control scaling is proportional to a reference voltage applied to GREF; when GREF is at the mid-point of the supply (VMID), the scale is nominally 20 mV/dB, or 50 dB/V.

Pin GAIN/RSSI, as an output, provides an RSSI voltage derived from the IF peak detector's output voltage; as in input, it accepts an external gain control voltage. In either case, the gain-control voltage to the IF amplifier cells is multiplied by a voltage proportional to absolute temperature (PTAT) so that the overall gain scale-factor is insensitive to temperature.

Low-impedance IF output, IFOP, may be loaded by resistances as low as 500 Ω to VMID. This output can either be digitized by an external A/D converter, as in Figure 1, or routed to the on-chip demodulator (DMIP) via a low-pass or bandpass filter to attenuate wideband noise generated in the high-gain IF amplifiers. For example, a single-pole low-pass filter at the IF reduces the signal level by 3 dB, but it improves the S/N ratio by reducing the wideband noise presented to the demodulator. Each demodulator comprises a full-wave synchronous detector and a two-pole low-pass filter, producing single-sided outputs at IOUT and QOUT.

The I and Q demodulators are driven by quadrature signals provided by an on-chip phase-locked loop (PLL) with its reference (at pin FDIN) at the IF.

The PLL's variable-frequency quadrature oscillator (VFQO) ensures excellent phase accuracy, as well as low EMI and power consumption. The PLL uses a sequential-phase detector (SPD), implemented in low-power current-mode logic, and a charge pump, which can source or sink 40 μA. The VFQO control path is filtered using an external CR network connected to FLTR. The circuit is designed to hold the frequency-control voltage on this pin for rapid reacquisition after power-down.

Wideband Radios Need Wide Dynamic Range Converters

by Brad Brannon

Wideband receivers typically down-convert from frequencies like 900 MHz to basebands of from 5 to 25 MHz, using a fixed local oscillator—and convert directly to digital. The many individual signal channels within are filtered, demodulated, and processed digitally. Such systems for base stations reduce cost and complexity—they need only a single high-frequency analog front end. But the key link, the A/D converter, must have excellent performance.

A/D specs for wideband receivers are driven by system radio standards. To receive distant signals in the presence of strong nearby signals, a cellular base-station receiver must have wide dynamic range. For example, GSM specs call for receivers that can accurately digitize signals from –13 dBm to –104 dBm in the presence of many other signals (Figure 1)—a 91-dB dynamic range! This implies that the spurious-free dynamic range (SFDR) of the converter and analog front end must be about 95 to 100 dBFS.*
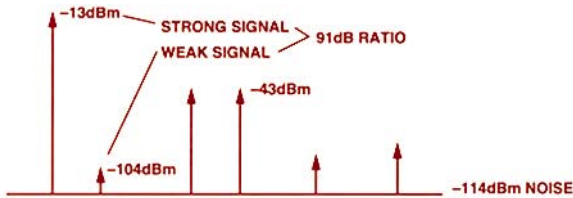

Figure 1. Weak signals must be detectable in the presence of strong signals in nearby GSM channels.

The largest spurs, usually produced by distortion components from strong signals at the front end, could mask weak fringe signals processed by the receiver. The *SFDR* spec permits assessment of signal to noise for signals near the noise floor of the receiver (or SNR's inverse, the bit error rate—BER—in a digital receiver).

GSM is one of the more difficult standards to realize using a broadband technique, so it serves as an excellent example of the importance of certain converter specifications. Other standards, such as AMPS (North American analog cellular), less demanding on receiver designs, are readily implemented using broad-band.

Full-scale SINAD and SNR, though adequate for single-tone input signals, can't provide the complete picture for the myriad signals and broad bands of spectrum present in wideband radios. Multiple-tone testing and SFDR power sweeps are more informative.

Converters often perform differently when digitizing a full-scale signal than they do with a smaller signal 10, 20, 30 or more dB below full scale—typical of broad-band radios. Figure 2 shows the SFDR of the 12-bit, 50-MSPS AD9042† as a function of signal amplitude. Because of converter integral nonlinearities and track/hold slew-rate limitations at full scale, the SFDR actually improves as the signal level is reduced in the vicinity of full span, providing increased dynamic range. SFDR ratios are better for lower signal levels because the converter is more linear over the rest of the

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*SFDR for a converted signal with a given amplitude is the log ratio (dB) of that amplitude to the largest spurious frequency component found in the converter's Nyquist spectrum (0 to F_S/2 Hz).

†For technical data on the AD9042 (price $199 in 1000s – ceramic; plastic available soon), use the reply card. Circle 3

range. Multiple signals also produce near-full-scale codes, but summing of randomized non-correlated signals resembles *dithering*.
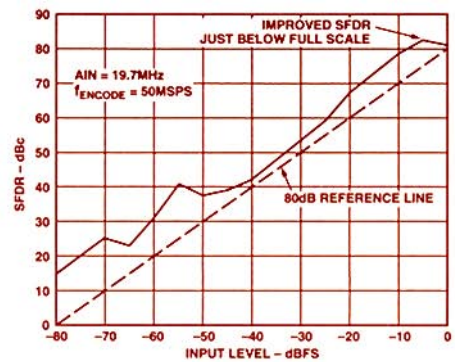

Figure 2. SFDR vs. input amplitude for AD9042.

Dithering is a technique used to lower non-linearities into the effective noise floor by making the converter use different parts of its range each time a given analog level is sampled. It can be implemented by either analog or digital methods. Digitally, a pseudorandom number (*dither*) is generated, converted to analog, and repetitively summed with the analog input signal [so each conversion result for a given level depends on the dither value]. After each conversion, the pseudorandom digital value is subtracted from the digital output. This technique reduces the spectral content that would be generated by repetitively exercising the same nonlinearity. In a wideband receiver, background noise and other non-correlated signals offer some of the benefits of dither, but dither is often intentionally added to improve dynamic performance.

Third Order Intermodulation Distortion: (IMD) is important where there are two large signals in the presence of many smaller signals. The two largest signals will generate spurs caused by non-linearities at $(2f_2 - f_1)$ and $(2f_1 - f_2)$. Significant spurs can override small desired signals located at these frequencies in the same way that harmonics can mask small signals; since these products always fall in band, they cannot be filtered. IMD is not important for its effect on the larger signals, but for interfering with smaller signals in nearby channels. The upper IMD product in Figure 3, aliased back in band, can clearly be seen. Also shown is that, besides IMD, other spurs can present problems. In this case, a large spur at $2(f_2 - f_1)$ indicates that measurements such as two-tone SFDR are just as important as two tone IMD.
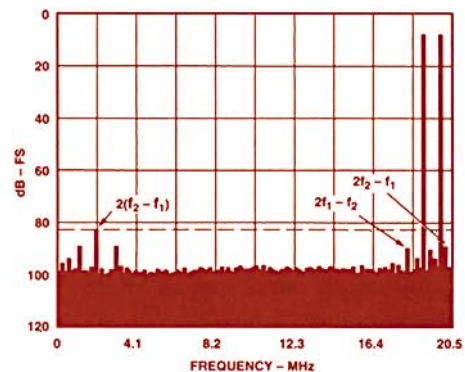

Figure 3. Two-Tone performance of AD9042.

Differential linearity errors (DNL), although architecture-specific, are increased by mismatches within multi-stage converters. They become important when low signal levels straddle a relatively bad code (one that stands out in a DNL plot). The effect can be seen

in the SFDR plot of Figure 4 by the sharp drop in SFDR between –25 and –40 dBFS. The rms error of the mismatch remains constant, but the SFDR becomes worse as the signal level is reduced and becomes a more-significant contribution to the spurious terms. Further down, the signal no longer crosses these mismatches and the SFDR stays high. Multiple signals or added dither can reduce this error source, improving the receiver's performance.
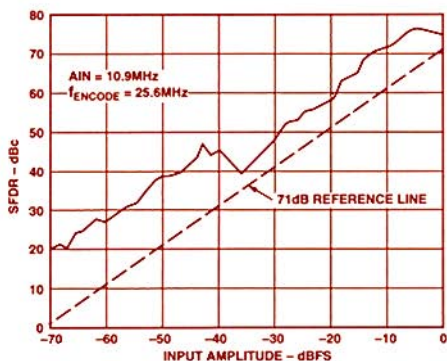

Figure 4. A "bad" SFDR plot. Note decrease near 35 dB.

Head room: When A/D converters receive multiple channels in a broadband architecture, each signal level must be considerably less than full scale of the converter. One signal alone may use the full-scale range of the converter, but when two signals may be present, each must be half-amplitude (–6 dB), assuming equal signal power, to prevent output clipping as these signals sum together at their peaks. *Each doubling of the number of signals requires individual levels to be reduced by 6 dB.* For example, –12 dBFS for 4 channels, –18 dBFS for 8 channels. A multi-channel radio must have enough dynamic range to account for the SNR lost through reduced usable signal levels. In addition, radio designers keep from 3 to 15 dB in reserve as headroom at the top of the ADC range to prevent clipping that comes from inevitable high incoming peak-to-rms ratios and saturation as additional signals come in band as new callers enter the cell zone.

OTHER ADC REQUIREMENTS

Sample rate: Many wide band radios mix down the RF spectrum to baseband (a range of signals from dc to some upper frequency) using wide-dynamic-range, ultra-high-intercept-point mixers such as the AD831 (*Analog Dialogue* 28-2, pp. 3-5). Converters for such radios require a sample rate at least twice the highest frequency (Nyquist rate), i.e., 20 MSPS minimum for signal range from dc to 10 MHz, and generally with at least 20% additional margin, raising the required encode rate to about 25 MSPS.

With both analog and digital standards, oversampling provides a processing gain that improves the effective SNR. For digitally modulated data, the ADC should sample at an integer multiple of the data rate, so that channel centers will fall in the center of FFT or filter bins. For example, if the receiver were decoding GSM packets, the sample rate would be a multiple of the 270.833-kHz data rate. The typical GSM receiver uses a multiple of 48 samples per bit, for a base sample rate, F_S, of 13 MSPS.[1] Sample rates for analog receptions, such as AM and FM, are multiples of the channel bandwidth. With AMPS, a 30-kHz standard, a typical sample rate 1024[2] times higher than the bandwidth is 30.72 MSPS.

Drive and filtering: An alternative to baseband sampling is to sample an IF signal that is in the second or third *Nyquist zone* [i.e., from $(N-1)F_S/2$ to $NF_S/2$]. Thus, the second Nyquist zone is from $F_S/2$ to F_S ; the third is from F_S to $(3/2)F_S$. For F_S = 25 MSPS, the second zone is 12.5 MHz to 25 MHz; the third is 25-37.5 MHz.

Using a higher zone can greatly relax the driving amplifier's harmonic requirements because filtering is much easier for frequencies above the first Nyquist zone.

At 10-MHz baseband, for 70-dB harmonic rejection with a 1-MHz signal, the drive amplifier must have 70-dB harmonic performance, because the antialias filter mustn't filter out harmonics below 10 MHz. But if the system were designed for a 1-MHz baseband signal at 26 MHz (F_S + 1 MHz, in the third Nyquist zone) the 2nd harmonic would be at 52 MHz, well outside the 25-to 37.5-MHz passband of the digitizer's anti-alias filter (Figure 5). Converter accuracy need not be sacrificed; all converter harmonics always fall "in-band", due to signal folding within the sampled system. Analog circuit requirements are simplified by the tradeoff of increased amplifier performance for relaxed filter specs. But intermodulation requirements cannot be reduced; IM has to always fall in-band for both amplifiers and converters. ▶
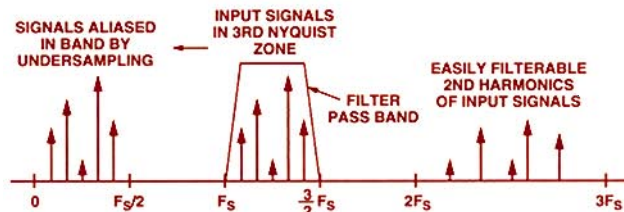

Figure 5. Easy filtering: Undersampling signal in 3rd Nyquist zone to eliminate harmonics at baseband.

[1]Other possible sample frequencies include 26 MSPS and 39 MSPS, both multiples of 13 MSPS.
[2]Other multiples are possible—usually powers of 2 and within the sample rate capabilities of available converters.

WIDE BAND RADIO OVERSAMPLING AND PROCESS GAIN

SNR can be improved by numerical operations called *processing gains*. In any digitizing process, the faster the signal is sampled, the lower the noise floor. The SNR doesn't improve and the total integrated noise remains constant, but it is spread out over more frequencies. The noise floor follows the equation (b = resolution):

$$Noise\ Floor = 6.02\ b + 1.8 + 10 \log\left(\frac{F_S}{2\ BW}\right)$$

This represents the converter's quantization noise and shows the relationship between noise and the sample rate. Each doubling of the sample rate lowers the effective noise floor 3 dB.

Although some gains are achieved by increasing the sample rate, they are relatively small. However, important gains are achieved in the digital filtering process when it is time to channelize and filter the signals with digital signal-processing chips. For instance, if a 30-kHz AMPS signal is being digitized with an AD9042 sampling at 40.96 MSPS, only a small portion of the broadband noise is passed through the digital filter pass band. The reduction of noise in the pass band, 0.03 MHz/20.48 MHz, is, in log form, 10 log(20.48 MHz/30 kHz), or 28.3 dB.

With this in mind, the effective SNR for a given signal is then

$$SNR = 6.2\ b + 1.8 + 10 \log\left(\frac{F_S}{(2 \times BW)}\right) - HR$$

If the actual SNR specification is known, substitute it for the (6.02 b +1.8) term. If the converter's SNR spec is 67 dB, with 8 signals, each signal will be 18 + 12 dB (headroom-HR) below full scale (as noted above). Thus, the overall signal levels will be 30 dB below full scale (i.e., SNR reduced to 37 dB). But the *effective* channel SNR will be 67+28.3–30 = 65.3 dB.

Choosing High-Speed Signal Processing Components for Ultrasound Systems

Figure 1. Transducer phased array for ultrasonic scanning.

by Paul Errico and Allen Hill

Medical ultrasound requires the control and processing of a variety of high-speed signals. Those signals include high-frequency sound waves, high-frequency/wide-dynamic-range continuous/pulsed waves, high-speed digital processing and video displays. The challenge facing many circuit designers is to combine all those high frequency signals while facing severe constraints on power consumption, circuit-board area and cost.

Ultrasound research, development, and commercialization have sprouted in the last four decades. It wasn't until the late '60s that the first commercial ultrasound scanner became available for cardiology, neurology and ob/gyn applications. The next major breakthrough came with the introduction of gray-scale imaging, followed by real-time gray scale scanning. Another major advancement was introduction of color Doppler, which is used to determine the velocity and direction of blood flow.

An ultrasound instrument for imaging interior portions of the human body is a sophisticated system; it comprises many high-speed processing elements and subsystems. The underlying concept behind ultrasound imaging is similar to that of sonar. A sound wave is transmitted from a transducer or transducer array, which also "listens" for the reflected signal (Figure 1). By using signal processing techniques to combine the reflected signals, and performing this process over a wide scan area, an image can be constructed to profile the area. Unlike sonar, ultrasound operates at high frequencies (1 to 10 MHz), penetrates to depths of many centimeters inside the human body, and can be used to create 1-, 2-, and 3-dimensional images.

Market Technology Hurdles and High Speed Products

Unlike other diagnostic imaging modalities, ultrasound offers real-time video and audio outputs unachievable with other imaging techniques. To the trained eye and ear, video displays and audio signals offer important diagnostic information.

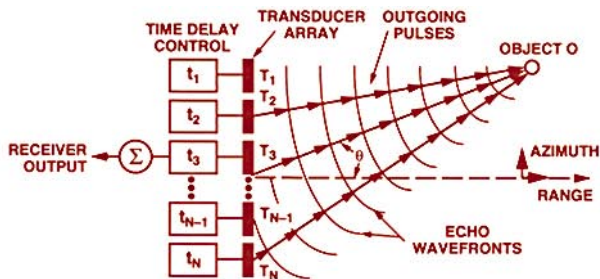The system frame rate and spatial resolution, and the gray-scale or color-video display parameters, establish the boundaries for the rate at which signals must be transmitted, received and processed. A rule-of-thumb is that sound waves travel at 1540 m/s in soft tissue. For example, an ultrasound signal that has to travel a total of 20 cm (10 cm into the body and 10 cm return) will take approximately 130 μs. The total time required to generate 128 scan lines (a typical number for a "fan" type of display) would be 130 μs $\times$ 128 = 16 ms, for a maximum update rate of 60 frames per second (fps). Also, if each scan line has multiple focal zones, the components used for transmitting and receiving must have fast slew rates, settling times, and conversion rates.

A rule-of-thumb for attenuation of ultrasound signals in soft tissue is 1 dB/cm/MHz. For example, a 5-MHz signal will have an attenuation factor of 5 dB/cm. If the target is at a depth of 10 cm, the reflected signal will be attenuated by 100 dB. This suggests that frequencies lower than 5 MHz are usually used when imaging deeper into the body.

Another important feature of an ultrasound system is that it must be portable, yet operate under power supplied by a standard 120 V/220 V outlet. So low power is a critical requirement for all the high speed signal processing components. Low power per-channel becomes especially critical as the number of Transmit and Receive channels increases.

These "hurdles" illustrates the need for high speed, low distortion, wide dynamic range and low power signal chain components.

Market Trends

Analog beam-forming (ABF) ultrasound systems have multiple analog front end (AFE) channels (See Figure 2). The variable-gain amplifier is needed to compensate for attenuation in the medium being penetrated. The time delay element is used to maximize the signal-to-noise ratio of the reflected signal from a predetermined point source (focal zone). Corresponding points on the time-delayed signals from each channel are summed, compressed and amplitude detected (rectified). Analog-to-digital
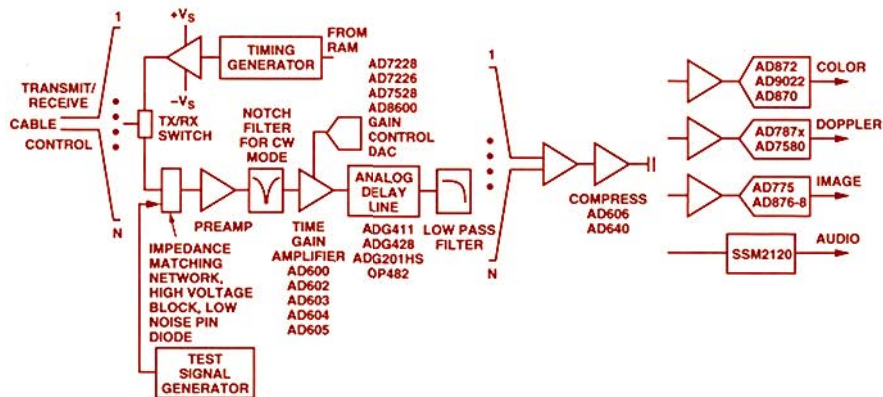

Figure 2. Front-end signal electronics for analog beam-forming system.

converters (ADCs) process *image* (8-10 bits, 20 MHz), *audio* (baseband 12 and more bits at audio sample rates) and color *Doppler* information (up to 12 bits at up to 10 MHz).

Digital data is processed with the use of FPGA, fixed-function off-the-shelf digital components, and digital signal processors (DSPs). The real-time capability of ultrasound requires optimization by digital processing (which includes FIR, IIR filters and FFT processing). The digitized data—in polar coordinates—must then be processed and mapped into rectangular coordinates, stored in buffer memory, and sent to the video and audio encoders.

Digital beam forming (DBF) systems replace the time delay element per channel with an ADC per channel and storage of successive signal elements in buffer memory (See Figure 3). The converter will typically be clocked at 40 MHz and will require 10-bits of resolution.

HIGH-SPEED IC COMPONENTS FOR ULTRASOUND*

Switching: In ABF systems high-speed multiplexers are used to create a cross-point switch. The switch is used to choose a predetermined time delay per channel by connecting each receive channel to a lumped passive LC element or active circuit element. Multiplexers must exhibit low R_{OD} and fast T_{on}/T_{off} switching characteristics. Switch settling times >100+ ns are not fast enough for multiple measurement points (gates) during a single scan line. Quad high speed switches like the ADG201HS, ADG411 and ADG441/2/4 offer fast T_{on}/T_{off} switching speeds.

	T_{on} max	T_{off} max	Faxcode*
ADG210HS	50 ns	50 ns	1493
ADG411	175 ns	145 ns	1503
ADG441/2/4	110 ns	60 ns	1513/4/5

Time gain-control: The time-dependent variable-gain, or time-gain-control (TGC), amplifiers are critical receiver components for both ABF and DBF architectures. Since the magnitude of the reflected ultrasound signal depends on the depth of penetration and is much greater close to the receiver, the gain must be increased as time increases. The 1 dB/cm/MHz rule-of-thumb attenuation figure requires that the TGC gain must be a linear function of the control voltage or "linear in dB". Also, the bandwidth, group delay and distortion should be independent of the gain. Three first-generation wide-bandwidth (up to 90 MHz), low-noise (<1.7 nV/√Hz), low-distortion TGC amplifiers have been available for this function. The second generation types, (AD604 and AD605) available in sample quantities, offer wider gain control, increased integration, lower power and cost.

	Channels	Input Voltage Noise nv/√Hz	Gain Range	Faxcode*
AD600	2	1.2	0 dB to +40 dB	1193
AD602	2	1.22	–10 dB to +30 dB	1194
AD603	1	1.5	Programmable from –11 dB to +51 dB with 40-dB gain range	1195
AD604	2	0.75	Programmable 14-20 dB preamp, 0 to +48 dB, +6 to +54 dB	Call ADI Sales
AD605	2	1.7	Single-supply, 48-dB gain range Programmable –14 dB to +48 dB	Call ADI Sales

The TGC control DAC provides the voltage controlling the TGC gain with 8-bit resolution. Its output slew rate and settling time must be fast enough to perform the "linear in dB" voltage control. The data must be loaded fast enough to update each control DAC for each new measurement point. Since multiple receiver channels are used in both ABF and DBF, multichannel DACs such as the AD8600, AD7228 and AD7528 are desirable.

	Channels	Slew Rate (min)	Data Setup (min)	Faxcode*
AD8600	16 (V-Out)	4 V/μs	40 ns	1429
AD7228A	8 (V-Out)	2 V/μs	90 ns	1261
AD7528	2 (I-Out)		130 ns	1298

Amplifiers: Throughout the system, analog signals need to be buffered, scaled, amplified and filtered. High speed buffers are used to drive analog to digital converters or used to drive high speed signals over long or short lengths of cables (e.g., from the system to the transducer head). They are also used to drive signals from one pc board to another through connectors or along the etches of a pc board.

Compression and detection of high-frequency signals is used to boost the effective range of the converter and to improve system performance. The AD606 and AD640 are two wideband logarithmic amplifiers which provide the necessary compression and have the signal bandwidth required for analog beam forming ultrasound. The AD606 provides 80 dB of dynamic range with frequencies up to 50 MHz; the AD640 offers 50 dB of dynamic range up to 120 MHz, and two devices can be cascaded for 95 dB. In some modes of operation the compressed output will overrange and saturate the next component in the signal chain. Wideband clamp amplifiers like the AD8036/8037 are ideal buffers for this application; they can also be used to limit the analog input voltage and to drive high speed ADCs, preventing the analog input from saturating the ADC input sample-and-hold.

Besides having wide bandwidth and economy of power, amplifiers used in the receiver signal chain (many per system) must also have low distortion. Amplifiers like the AD8011, AD8001, AD8047
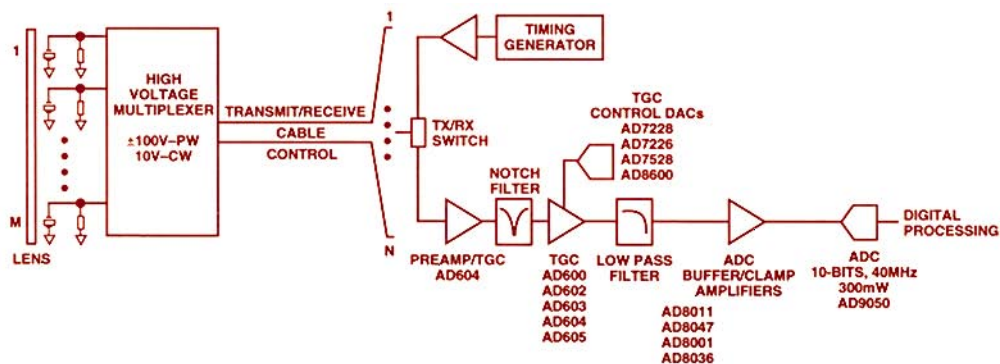

Figure 3. Front end signal electronics for digital beam system.

*For data on these products, call ADI's AnalogFax™ line, 1-800-446-6212, and enter the appropriate Faxcodes.

and AD9631/32 offer the speed and performance required in many ultrasound applications.

High speed video amplifiers are also used for driving cables to monitors and video capture devices. Video amplifiers like the AD817/AD818 and AD826 and AD828 offer good video performance, such as differential phase and gain specs.

	Principal Function	Faxcode*
AD8001	800 MHz, 50 mW	1396
AD8011	300 MHz, 1 mA	1863
AD8047/48	250 MHz, general purpose	1868
AD9631/32	High-speed, low distortion	1468
AD8036/37	Wideband, clamp	1836
AD812	Dual 65-MHz, 40 mW	1402
AD817/818	Video	1404/05
AD813	Triple video amp, power down	1403
AD826/828	Video, 2-channel AD817/AD818	1408/10

A/D converters: The ongoing shift to DBF is increasing the number of ADCs used per system. As lower-power, lower-cost, and higher-performance ADCs become available, ultrasound designers are incorporating a single ADC for each transducer element. This allows beam forming to be accomplished in the digital domain, which offers inherent stability and increased accuracy. DBF eliminates the bulky LC delay elements and replaces each with a high speed ADC. The typical number of channels per system ranges from 64 up to 256, determined by the number of transducer elements and signal-to-noise ratio target.

The AD9050 (10-bit, 40-MSPS ADC) is designed to meet the demanding requirements of DBF ultrasound systems. First in importance is low power. With up to 256 ADCs per system, even small increases in ADC power significantly increase overall system power. The AD9050 uses only 300 mW operating from a single supply (+5 V); it utilizes an innovative architecture and is fabricated on a state-of-the-art BiCMOS process.

ADC performance is critical for image quality. The key requirement of the DBF system designer is to provide the best quality image at the lowest power and cost. The key ADC parameter used to quantify image quality is effective number of bits (ENOBs). The closer the ADC's ENOBs are to theoretical resolution, the more faithful the image reproduction. The image bandwidth is determined by the transducer frequency, which typically ranges from 1 to 10 MHz. The ADC's ENOB vs. frequency plot should be flat over the bandwidth of interest.

The sample rate for the ADC is chosen judiciously for optimal system performance. High clock rates provide the ability to resolve small time delays, which improves focus in the digital beam former. High clock rates also allow 4× oversampling of the transducer frequency to permit efficient detection for color flow applications. Most DBF systems operate with clock rates in the range of 30 to 40 MSPS. The AD9050 samples up to 40 MSPS, and its clock input and digital outputs can be configured for 5-V or 3-V operation. The use of 3-V ASICs to process the ADC's digital output is becoming increasingly common as designers seek to minimize system power.

Another key ADC parameter for ultrasound systems is recovery time from input overdrive. In Doppler modes, gain is set to the maximum because the measured phenomenon is very small (blood velocity). In this case, the reflected signal from a vessel wall will overdrive the ADC input; then upon recovery valid measurements of blood flow are made. With only 10 bits of ADC resolution,

multiple data records must be averaged to achieve accurate blood flow measurements. If overdrive recovery is not consistent then lack of correlation between records will cause flow measurement errors.

The analog input section of the AD9050 is designed to prevent damage and corruption of data when the input is overdriven. The nominal input range is +2.8 V to +3.8 V (1 V p-p, centered at 3.3 V). "Out-of-range" comparators detect when the analog input signal is beyond this range and shut off the input track-hold. The digital outputs are locked at their maximum or minimum value (i.e., all "0" or all "1"). This prevents them from changing to an invalid value when the analog input is out of range. The input is protected for up to 0.7 V beyond the power supply rails; i.e., for nominal power (+5 V and ground), the analog input will not be damaged with signals from +5.7 V to –0.7 V.

When the analog input signal returns to the nominal range, the out-of-range comparators switch the track-hold back to the active mode and the device recovers in approximately 10 ns.

Here's a quick summary of suitable converters available:

	Resolution (bits)	Sample Rate (MHz)	Faxcode*
Imaging			
AD775	8	20	1345
AD876/8	8	20	1375/6
AD9058	8	40	1455
AD876	10	20	1838
AD9050	10	40	1843
Color Flow			
AD1672	12	3	1880
AD870	12	10	Call ADI sales
AD872	12	10	1431
AD9022	12	20	1840
AD9026	12	25	1842
AD9042	12	41	1922
Audio			
AD7870A, 75/76	12	100 kHz	1898, 1374/5
AD7871/72	14	83 kSPS	1371/2
AD7874	12 (4-channel)	8 μs/channel	1373
AD7878	12 (8-word FIFO)	100 kHz	1376

Digital signal processors: The number of measurement points, speed, and wide dynamic range of the data that has to be processed requires the use of high-speed digital processors. DSPs perform such tasks as FIR/IIR filtering and computing the AFE time delay variables. The ADSP-21060 (32-bit floating point, 40-MIPS) SHARC DSP processor, with its 4 Mbits of on-chip memory, offers the performance needed in such demanding applications as ultrasound and many other medical imaging applications. If cumulative roundoff errors over many computations don't pose a serious problem for a given system, cost-effective 16-bit fixed-point processors like the ADSP-2171 and ADSP-2181 with on-chip memory and high speed operation offer versatile I/O and up to 33-MIPS performance.

		Faxcode
ADSP-21060	32 bits, 40 MIPS, 4-Mbit internal RAM	1870
ADSP-2171	16 bits, 33 MIPS, on-chip Memory, PROM	1869 (52 pgs)
ADSP-2181	16 bits, enhanced 2171	1927

The processed data is sent to the video display and audio encoder. Triple 8- to 10-bit RAM-DACs, i.e., the ADV family of products, are used to convert digital words to analog for color display. The AD720/721/722 family of analog RGB to NTSC/PAL encoders, combined with video amplifiers like the AD813, AD817/818 and AD826/828 (low cost, good video performance industry standard amplifiers) are used to accommodate the various video standards for display and recording. ▶

***For data on these products, call ADI's AnalogFax™ line, 1-800-446-6212, and enter the appropriate Faxcodes.**

Ask the Applications Engineer—18

SETTLING TIME

by Peter Checkovich

Q. *Why is settling time important?*

A. Op amp settling time is a key parameter for guaranteeing the performance of data acquisition systems. For accurate data acquisition, the op amp output must settle before the A/D converter can accurately digitize the data. However, settling time is generally not an easy parameter to measure.

Over the years, the techniques and equipment used to measure the settling time of op amps have been barely able to keep up with the performance of the devices themselves. As each new generation of op amps settles to better accuracy in shorter time, greater demands have been placed on test equipment, its designers, and its users. A major dilemma, often causing disagreement among engineers, is whether some combination of techniques and equipment actually measures the device under test (DUT) or just some limiting property of the test setup. So there is continual development of new test equipment and techniques in an effort to specify this ever-demanding parameter.

In a data-acquisition system, the output of an op amp should settle to within 1 LSB [i.e., $2^{-n}FS$] of final value of the A/D that it drives within a time period dictated by the sampling rate of the system. To settle within 1 LSB of full scale implies the settling accuracy of the A/D is ±1/2 LSB. Thus, a 10-bit system will require the op amp to settle to half of one part in 1024, or approximately 0.05%. A 12-bit system will require settling to half of one part in 4096 (0.01%). The requirements for 14-bits and greater are yet more demanding. Settling-time values such as 0.1% and 0.01% are the most widely specified.

Although a larger full-scale signal range will increase the size of the LSB, easing the problem somewhat, it is not a feasible approach for high-frequency systems. Most high frequency A/Ds have a full-scale span of 1 V or, at most, 2 V. For a 10-bit system with a 1-V full scale signal, an LSB is about 1 mV. For a 12-bit system, an LSB is approximately 250 µV. To resolve the settling characteristics for a full-scale transition, dynamic ranges approaching four orders of magnitude must be handled. With settling times of new op amps [e.g., the AD9631 and AD9632*] dropping to the 20 ns to 10 ns range, the measurement of settling time presents quite a challenge.

Q. *How is settling time measured?*

A. A key requirement over the years has been the need to drive the input of the op amp with a fast, precise signal source, often referred to as a flat-top generator. As the name implies, such a generator would have a sharp transition between two levels of known amplitude at time, t_0, should have minimal overshoot (or undershoot) and then remain flat for the remainder of the measurement time. In this case "flat" means significantly flatter than the error to be measured in the amplifier.

The great accuracy is required to be certain that any output signal from the op amp is entirely due to its settling response and not its response to a signal that is present at the input after the step transition. Any active device in the path of this signal would require better settling characteristics than the DUT.

Such generators are in practice very difficult to develop. A rather "low-tech" device has served for quite some time as a means for generating a flat-top transition; the contact opening of a mercury-wetted-contact relay connected to a stable low-impedance voltage source can be used to produce a rather clean (and surprisingly fast) flat-topped pulse. The figure shows a simple circuit that performs this function. For a negative-going transition, with the relay closed, a dc voltage, VSTEP, is applied to the input of the DUT and a 50-Ω resistor to ground. When the relay opens, the input node rapidly discharges to ground, creating the input transition. The open relay contact ensures that all other elements are totally isolated from the amplifier input; the input level is held constant (grounded through 50 Ω) for as long as the relay remains open.
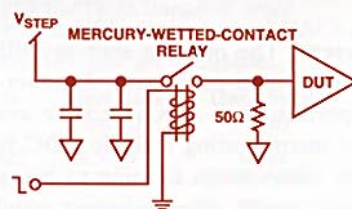
Next problem: directly measuring the output requires handling a large dynamic range. If the DUT is configured as an inverter, a subtractor circuit can be created that only looks at the error signal and does not have to handle the entire dynamic range of the output. This figure shows a circuit used for measuring the 16-bit settling time of the AD797*—800 ns typical to 0.0015%.
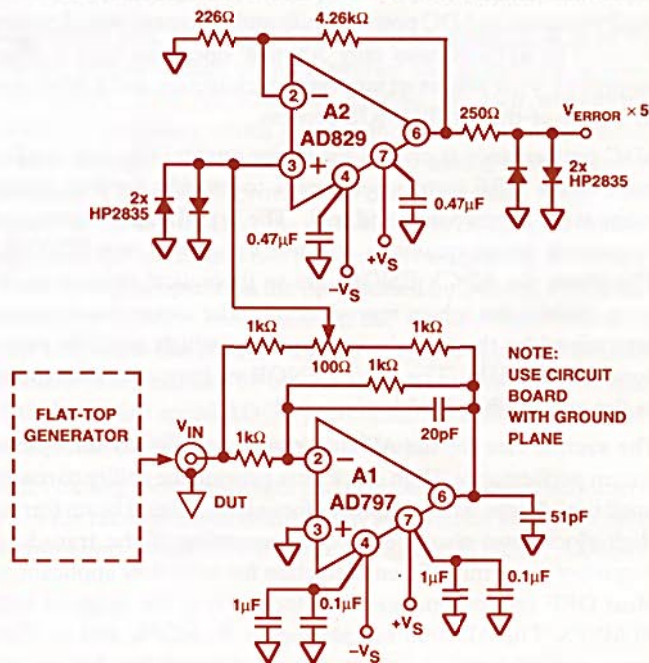
A1, the DUT in this circuit, is configured for a gain of –1. The voltage divider from input to output forms a second "false" summing node that will replicate the signal at the amplifier's summing node. The 100-Ω potentiometer is used to null the dc voltage. The wiper of the potentiometer is clamped by the diodes at the input of A2 to limit saturation effects in this amplifier. The output is also similarly clamped.

Since the pre- and post-transition voltages at the output of A2 will be the same (i.e., the difference will be zero), the settling

characteristics of this amplifier due to a step change are not important for measuring A1. Thus, the output of A2 can be measured to find the settling time of A1.

This technique requires that the DUT be configured as an inverting amplifier. The circuit can be made to work at other gains, but the resistor values and setting of the dc balance potentiometer will have more influence on the measurement.

Q. Any other techniques?

A. Another technique for measuring settling time uses the computing power of a digital oscilloscope. It calculates a waveform that represents the settling error as the instantaneous difference between the acquired input and output signals of the DUT and compares them with the values for an ideally settling device. The resulting waveform is the error of the DUT.

If there is a gain error in this system, it will show up as a dc offset in the error waveform. The calculation can be adapted for a DUT with any gain, either inverting or non inverting. It also can compensate for a signal generator that itself has a low frequency settling tail. The DUT response to a low frequency input will not be influenced by that settling time.

Because such oscilloscopes are designed primarily for speed, in order to determine errors at higher resolutions, averaging must be used. For example, if the A/D used in the oscilloscope has only 8 bit resolution, but accuracy better than 8 bits, a number of cycles can be averaged to increase the effective resolution of the measurement.

Q. Any more?

A. Yet a third way to measure settling time is to look at the output directly. A Data Precision Data 6000 can directly digitize signals of up to 5 V with 16-bit accuracy and 10-ps resolution. The only fly in the ointment is that the instrument relies on repetitive sampling with a comparator probe. The waveform is built up one bit at a time for each of the sample points. As a result, obtaining a settling characteristic can be very time consuming. This is especially so when using a relay-type flat top generator with a 1-kHz upper frequency.

Q. Why do data sheets sometimes define short term and long term settling characteristics?

A. The traditional definition of settling time is the time from the input transition to the time when the amplifier output enters the specified error zone and does not leave again. This concept is relatively uncomplicated and straightforward. However, there are some cases where the initial settling is fast, followed by an extended period of settling to the final value. Single-supply amplifiers may exhibit this characteristic in the vicinity of the lower rail. Of greater prevalence for large transients, a "thermal tail" is a slow drift that continues for a relatively long time after rapid settling to apparently excellent initial accuracy.

Thermal tails are produced when voltage level changes within the op amp caused by a step transition create temperature gradients among the transistors. Matched transistors will not track well while they are at temporarily different temperatures. The thermal time constant of the chip determines how long it takes for equilibrium to return. Op amps are designed to prevent or reduce these effects by careful placement of devices and strategies to produce thermal symmetry, but this is easier for low-level high-precision devices than those designed for high-speed, because of the large, rapid swings of power that occur.

In particular, the new dielectrically isolated processes (like XFCB) that have worked wonders for improving the raw speed of the op amps can have some difficulty in minimizing the presence of thermal tails. This is because the process provides each transistor a separate dielectric "tub." While this dielectric isolation reduces the parasitic capacitance and greatly speeds up electrical performance, it also provides thermal insulation that slows the dissipation of heat to the substrate.

The seriousness of long tails depends on the application. For example, some systems sample at rates compatible with the initial short-term settling time and are not seriously affected by longer term drifts. Communication systems and others, where the frequency domain properties of the converted signal are most important, are examples of such systems. Although long-term settling errors can produce variations in gain and offset, the long-term thermal tails will have minimal contribution to the distortion products of the digitized signal. For these systems, frequency domain measurements—such as distortion products—are more important than time domain measurements, such as settling time.

On the other hand, systems such as video and scanners might produce a step input, followed by a long-duration plateau of constant value. During this time, repetitive A/D conversions of the op amp output signal will track the long-term settling characteristic. For these systems it is important to understand the long term settling characteristics of the op amp.

The figures below illustrate the long- and short-term settling patterns for the AD8036*, a unity-gain-stable high-speed clamp amp that is a good candidate for an A/D driver in high speed systems. The figure at left shows that after the initial large transition, the output is still about 0.09% from its long-term final value. However, the right-hand figure shows, on a 300× faster scale, that after about 16 ns the output has entered a local 0.01% short-term settling region which can be usefully sampled by some systems. The distortion of the AD8036 is extremely low (2nd and 3rd harmonics down by more than 65 dB with 500-Ω load) so it would be a good candidate in systems where this kind of performance is critical. ▶
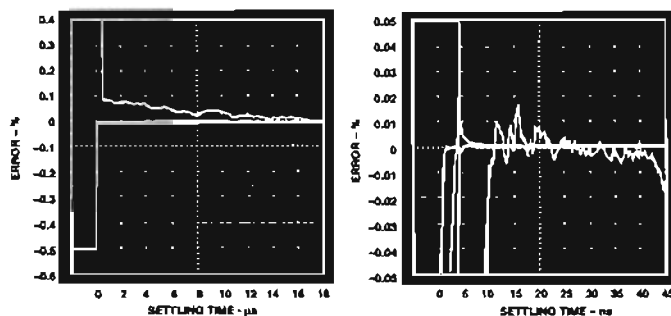
Reference: Demrow, Robert, "Settling time of operational amplifiers," in *The Best of Analog Dialogue*, 1967 to 1991, pages 32–42. **Circle 34**

Analog-Digital Conversion Handbook. Norwood, MA; Analog Devices, 1986, pp. 312–317 and 436–439 (DAC settling time). [Use book purchase card]

A/D Converters and Multiplexers

3, 5, ±5-V Muxes
8-channel ADG608, 2×4-channel ADG609

The ADG608/609 multiplexers are designed for use on low supply voltage common in battery and portable operation. The **ADG608** chooses one of 8 inputs, controlled by 3 address lines and an Enable input. The **ADG609** switches one of four differential inputs to a differential output (2 address lines and Enable).

Both devices are specified for operation on +5-V and +3.3-V single supplies, and ±5-V dual supplies. Maximum on-resistance is 35 Ω (–40 to +85°C, dual supplies). Features include an analog signal range extending to the supply rails, fast break-before-make switching (75 ns t_{ON} max and 45 ns t_{OFF} max), low dissipation (1.5 µW max) TTL/CMOS compatibility, and ESD > 5000 V (MIL-STD 3015.7). Operation is from –40 to +85°C and –55 to +125°C; packaging is in 16-pin plastic DIP and TSSOP. Prices (100s) start at $3.85. **Circle 6** ▶

Dual 6-Bit 60-MSPS A/D Converter
AD9066 is designed for I & Q demodulators
Meets data rate requirements of DBS receivers

The AD9066 is a low-cost dual 6-bit, 60-MSPS A/D converter designed for quadrature demodulators used in high-data-rate digital communications. It was designed specifically for the high data-rate requirements of direct-broadcast satellite (DBS) receivers—consumer set-top boxes that demodulate digitally compressed video signals using quadrature phase-shift keying (QPSK) modulation for data rates from 40 to 60 Mb/s. More applications exist in wireless LAN and digital radio receivers, as well as other receivers for spread spectrum and instrumentation.

The AD9066's digital outputs are CMOS compatible; the ENCODE input uses a CMOS stage with a TTL-compatible (1.4-V) threshold. Specifications (60-MSPS encode rate, 15.5-MHz signal) include 34-dB min SINAD, 5.3 min effective bits (ENOB), –40-dB max THD.
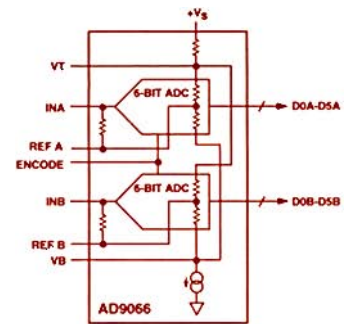
The AD9066 includes two matched 6-bit ADCs, an on-chip voltage reference, and biasing circuits to simplify ac-coupled operations. It operates on a single +5-volt supply, dissipating only 400 mW, is housed in a 28-lead SOIC ("R" package), and is available for commercial (0 to +70°C) and industrial (–40 to +85°C) temperature ranges. An evaluation board is available. Prices for the AD9066 start at $4.59 (1000s). **Circle 7** ▶

Serial 12-Bit ADCs
Lowest power +3-V or +5-V: 1/8-channel AD7853/7858

These flexible low-power 12-bit A/D converters, operating on single +3 or +5-volt supplies, have on-chip voltage references and throughput rates of 200 ksps or 100 ksps (L versions). They have facilities for self- and system calibration, as well as power-down options to conserve power.

The **AD7853** and **AD7853L** are single-channel converters, while the **AD7858** and **AD7858L** convert up to either 8 single-ended or 4 differential channels. The L versions trade off speed and power, having about 1/2 the speed and 1/3 the dissipation (5.5 mW vs. 15 mW). Automatic power-down after conversion (25 µW) and a 3.6-µW "sleep" mode further conserve power. All devices are available for the –40 to +85°C range, and 24-lead packages include plastic DIPs, SOICs, and SSOPs. Prices start at $6.42 (1000s). **Circle 8** ▶

16-Bit Analog ADC Front End with PGA
AD7715 uses only 1.49 mW max (15 µW in standby)

The AD7715 is a complete single-supply (+3 or +5-V) analog front end for low-frequency measurement applications. It can accept low-level differential input signals directly from a transducer (for example, RTD, thermocouple, pressure transducer), and its output is a serial digital word. Its Σ-Δ conversion technique provides 16 bit output with no missing codes. A digital filter has programmable cutoff frequency and output update rate.

A programmable-gain amplifier provides four software-programmed gains: ×1, ×2, ×32, ×128, to handle unipolar signal ranges of 0 to +20 mV, +80 mV, +1.25 V, +2.5 V, or bipolar ranges ±20 mV, ±80 mV, ±1.25 V, ±2.5 V. Calibration (self- or system) is provided to eliminate gain & offset errors. The output is available via a 3-wire serial interface.

The AD7715 is suitable for any application requiring high-resolution measurement of
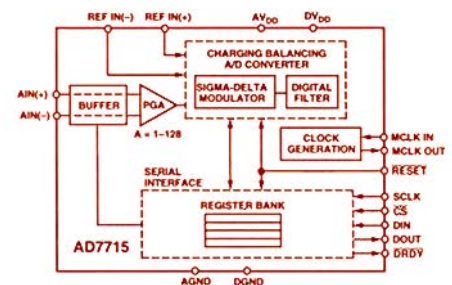
low-frequency signals. Examples include weigh scales, temperature, liquid and gas flow. Its single-supply operation and low power dissipation are especially attractive for smart loop-powered transmitters and portable, battery-powered equipment.

3- and 5-volt versions of the AD7715 are available in 16-lead plastic DIPs and SOICs for –40 to +85°C. Evaluation boards are available. Price of the AD7715 is $6 (1000s). **Circle 9** ▶

D/A Converters

16-18-Bit Self-Calibrating DACPORT
AD760 is complete, includes 10-V precision reference
Interfacing is serial: (16/18 bits) or byte (2 × 8 bits)

The AD760 DACPORT®, a complete 16-
or 18-bit self-calibrating voltage-output
DAC, is the most accurate monolithic DAC
available on the market today. It includes a
precision buried-Zener voltage reference,
double-buffered latches, and an output
amplifier, fabricated on the Analog Devices
BiCMOS II process.

Data can be loaded in as straight binary serial
data or as two 8-bit bytes. In serial mode,
16- or 18-bit data can be accepted, MSB or
LSB first. With calibration, the AD760 is 17-
bit monotonic over the entire –40 to +85°C
range, with ±0.75 LSB maximum (16-bit)
integral nonlinearity.

With its maximum 20-volt settling time of
13 µs (8 µs typical) to within 8 ppm, the
AD760 is suitable for use anywhere a high-
precision programmable voltage or signal
source is required. It is ideal for medical and
scientific instrumentation, high-end data
acquisition, industrial control, and ATE.
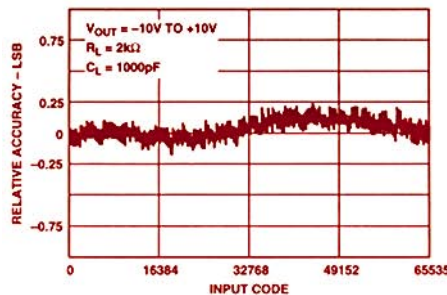
AC specifications include 94-dB minimum
signal-to-noise, and maximum harmonic
distortion of 0.005% for 0 dB, 0.03% for
–20 dB, and 3% for –60 dB 1001-Hz signals
sampled at 100 kHz. Output noise voltage
spectral density is 120 nV/√Hz, 1 kHz to
1 MHz (excluding reference).

The AD760 requires ±15-volt supplies, plus
a 5-volt logic supply. It is housed in a 28-
pin cerdip package. Its price is $50 in 1000s.
Circle 10

Quad 14-Bit DACs
Vout, serial & parallel
AD7834 & AD7835

The AD7834 and AD7835 comprise four
channels of voltage-output multiplying D/A
conversion with ±8.192-V full-scale output.
They feature power-on and Clear to a user-
defined voltage. Excellent DNL/INL specs
(±0.9 LSB, ±1 LSB) are useful in ATE,
process control, instrumentation, and 12-bit
upgrades. Both types need ±15-V & +5-V
supplies.

The serial AD7834, available in 28-lead
SOIC and plastic DIP (both A & B grades,
–40 to +85°C), and cerdip (S, –55 to
+125°C), includes 5 package-address pins
that can be wired to allow up to 32 devices
(128 channels) to be addressed in one
system. Prices (1000s) start at $21.25.

The AD7835 can be loaded either in 14-bit
parallel, or 8- and 6-bit bytes. Pairs of DACs
can use separate references. A and B versions
are available in 44-lead PQFP, and the A
version is available in PLCC. Prices start at
$22.35. **Circle 11**

8-Channel TrimDAC
8-bit AD8801/AD8803
Replace 8 potentiometers

The AD8801 and AD8803, 8-channel
single-supply (+3 V to +5 V) voltage-output
TrimDACs®, replace voltage-divider poten-
tiometers for all-electronic "hands-off" digital
control of gain and offset, signal levels,
brightness and contrast of displays, and other
kinds of parameters for (especially portable)
audio, video, and instrumentation systems.

The AD8801 has an $\overline{RS}$ terminal; when
asserted, it presets the outputs on startup to
provide a mid-scale nominal initial value
(instead of zero or full-scale). In the
AD8803, the low reference lead (V_{REFL}) is
brought out (not grounded) for a flexible
range of adjustment. Both accept 3-wire
serial data, have 8 individually program-
mable analog outputs, and save power in
shutdown, drawing ≤ 25 µW. They are
housed in 16-pin plastic DIPs & narrow-
body SOICs for –40 to +85°C. Price (1000s)
is $3.49. **Circle 12**

Serial 16-Bit M-DAC
Voltage-output AD7849 is
17-bit monotonic, T_{MIN}-T_{MAX}

The AD7849 is a serial-input multiplying
D/A converter with two 16-bit grades
(B & C) and a 14-bit grade (A) for –40 to
+85°C. A 16-bit "T" grade is also available
for –55 to +125°C. A unique feature,
clamped-to-zero analog output during
power-up & power-down, is useful in
industrial control applications; this state can
also be driven by a supervisory chip detecting
brownout conditions. A Clear (to analog
zero) state (binary or twos complement) is
also available.

The device will accept reference voltages of
up to ±6 V at its two reference input
terminals, and its output will swing to ±10 V.
Settling time to 0.006% is 7 µs typical.
Required supplies are ±15 V at 5 mA max and
+5 V at 2.5 mA max. Packaging is in 20-pin
plastic DIP or SOP, and in cerdip (T version).
Prices (1000s) start at $8.93 (14-bit A
version) & $11.10 (16-bit B). **Circle 13**

220-MHz RAM-DACs
ADV7160/7162: 96-bit data,
10-bit DACs, PLL, cursor

The ADV7160 and ADV7162 are low-cost
integrated high-performance color RAM-
DACs featuring 96-bit pixel port (24-bit true
color), "color-enhanced" 10-bit DAC
technology, with the capability of delivering
24-bit color at 220 MHz. They include on-
board PLL and hardware cursor. The low-
cost ADV7162 is packaged in a 160-pin
QFP; and the high-performance ADV7160
is packaged in a plastic 160-pin power quad
flatpack (PQUAD). Prices (1000s) start
at $26.

Designed for Windows accelerators and
workstation graphics these parts deliver the
ultimate in picture resolution, in both size
and color. They can deliver 24-bit true color
at resolutions up to 1,600 × 1,280 pixels at
ergonomic refresh rates of up to 85 Hz. They
include an on-board multi-plexer, lookup
table, cursor, and PLL. The DACs are
matched to within 2% max. **Circle 14**

All brand or product names mentioned are trademarks or registered trademarks of their respective holders.

"A Mixed Bag"

Lo-Dropout Regulator
75 mV max for I_L = 100 µA
350 mV max at I_L = 200 mA

The ADP667 is a complete low-dropout linear voltage regulator that can supply up to 250 mA of output at +5 V. With two external resistors, it can alternatively furnish an adjustable 1.3-to-16-V. It can directly replace (pin-for-pin, spec-for-spec) existing 667-type regulators.

Its features include a low-battery indicator to monitor input supply voltage and a dropout detector to signal loss of regulation. A low-power CMOS device, it draws only 30-µA max of quiescent current (0.1 mA load), and only 1 µA max in the Shutdown mode (significantly extending battery life). Typical applications include handheld instruments, battery-operated systems, remote data-acquisition systems, cellular phones, etc.

It is available in 8-lead plastic DIP and SO packages for a temperature range of –40 to +85°C. Prices start at $2.00 in 1000s. Circle 15 ▶

Accelerometer Evaluation Modules
ADXL05EM-1 & 3: ±4-*g* single and tri-axis
ADXL50EM-1: ±25-*g* single axis

This family of low-cost, pre-packaged accelerometer modules make it quick and easy to evaluate the ADXL50 and ADXL05 micromachined accelerometers. The EMs are fully assembled, trimmed, and packaged inside a small, rugged case. All of the electrical and mechanical design has been done; to measure acceleration, screw the device down and connect up a +5-V supply and a voltmeter.

Characteristics of the ADXL50EM-1 include 80 mV/*g* with ±25-*g* full scale and 400-Hz bandwidth, 130 m*g* rms noise, 0.2%FS nonlinearity. The ADXL05 EMs have 500 mV/*g* with ±4-*g* span, 100-Hz bandwidth, 5 m*g* rms noise. Both types have 0.2% FS nonlinearity, and ±2° alignment error. Output of all devices is 2.5 V at 0 *g* with ±2.0 V span. Supply voltage is +5 V, at current from 8 mA (1 axis) to 24 mA (triaxial).

The packages measure 1.875"L × 1"W × 0.75"H (47.6 × 25.4 × 19 mm) with mounting holes on 1.375" (34.93 mm) centers. A 5-lead 36" (0.91-m) connecting cable is included. Temperature range is –40 to +85°C. Single-unit prices are $99.95 for single-axis modules and $220 for tri-axis modules. Circle 16 ▶

RGB→NTSC/PAL
Single-supply AD722
Easy to use, lowest cost

The AD722 is a low-cost, single-supply (+5 V) fully integrated RGB-to-NTSC/PAL video encoder, packaged in a 16-pin SOIC, for 0 to 70°C. It encodes red, green, blue (RGB) component signals into National Television Standards Committee (NTSC) or phase-alternating line (PAL) luminance (brightness), chrominance (color), and composite baseband video signals. It provides the lowest-cost encoding solution available, due to an on-chip delay line and an on-chip PLL that enables use of a low-cost FSC crystal for generating all timing. (It can also accept FSC or Σ4 FSC clocks—and CSYNC or HSYNC/VSYNC.)

It can be used in a wide range of video, from multimedia PCs, video games, and set-top boxes to virtual-reality headsets and MPEG video CD players. Its outputs will drive three 75-Ω reverse-terminated cables simul-taneously. Price in 10,000s starts at $3.55. Circle 17 ▶

3-V IF Subsystem
AD608 has mixer, log/limit amp, RSSI output

The AD608 is a 3-volt IF subsystem in a 16-lead SOIC. It consists of a mixer plus a log/limiting amplifier; and it provides a received-signal-strength-indicator (RSSI) output and a hard-limited output. It can operate on supplies from 2.7 V to 5.5 V at 7.3 mA.

In PM or FM systems (such as the Japanese Personal Handyphone system) the AD608 converts a signal from a high IF (typically 240 MHz) to a lower IF (typically 10.7 MHz), amplifies it, and provides limiter & RSSI outputs. Key characteristics include low power—21 mW at 3 V, wide bandwidth—500 MHz mixer and LO, 80-dB RSSI range for ±1-dB accuracy, –15 dBm 1-dB compression point for strong signals, and –5 dBm 3rd-order intercept for low IMD. Temperature range is –25°C to +85°C with 2.7-5.5 V supplies (–40°C to +85°C for 4.5 to 5.5 V supplies). Price is $4.95 (1000s) Circle 18 ▶

Reset Generator
ADM709 monitors supplies: +5 V, +3.3 V, and +3 V

The ADM709 is a precision power-supply voltage monitor for microprocessor systems, computers, controllers, intelligent systems, etc. It generates a system Reset during power-up, power-down, and brownout conditions. For example, when V_{CC} falls below the reset threshold, $\overline{RESET}$ goes low and holds the µP in Reset. Quiescent current is 35 µA. Power-on reset pulse is 140 ms (min).

The ADM709 is a direct pin-for-pin, spec for spec replacement/upgrade for industry-standard 709 power-supply monitors. Five grades are available, distinguished by their nominal Reset threshold levels: L (4.65 V), M (4.40 V), T (3.08 V), S (2.93 V), and R (2.63 V). The operating temperature range is –40 to +85°C for all grades, and a choice of 8-lead plastic DIP and SOIC packaging is available. Price is $0.70 (70¢) in 1000s. Circle 19 ▶

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Amplifiers—Four New Duals

Dual 16-MHz Rail-to-Rail FET
AD823 can operate on single supplies, +3 to +36 V
Settles to 0.01% in 350 ns; Drives 500 pF

The AD823 is a dual 16-MHz, single-supply FET-input op amp with an output that can swing to within 25 mV of both supply rails. The input can swing below ground and exhibits no phase reversal when the input reaches the supply rail. The device can operate from a single supply (+3 to +36 V), or dual supplies (±1.5 to ±18 V).

The FET input means low bias current, in fact: 25 pA max at +25°C. Input offset voltage is low, at 800 µV, with 2 µV/°C drift. And speed is high—a 16-MHz bandwidth at G=+1, with fast settling: 350 ns to 0.01%, and a 22 V/µs slew rate. Distortion is low: –108 dBc worst harmonic at 20 kHz. It can furnish output currents of ±15 mA with only 0.5-V drop from supplies, and drive capacitive loads as high as 500 pF stably. The data sheet includes published specifications for operation at +3.3, +5, and ±15-volts.
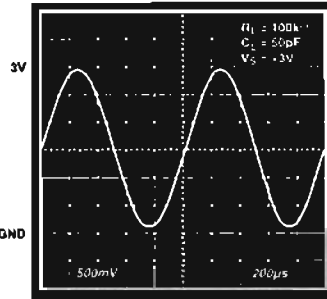
Applications include battery-operated portable instrumentation, photodiode preamplification, active filters, and buffering for A/D converters.

The AD823 is available for operation over the extended industrial temperature range, from –40 to +85°C, and is packaged in 8-lead plastic mini-DIPs and SOICs. Price (1000s) is $2.25. **Circle 20** ▶

Rail-Rail Dual 'OP27'
OP284: Low drift & noise
Works on +3 to ±18 V

The OP284 is a dual precision operational amplifier housed in 8-lead epoxy DIP and SOIC packages. It has rail-to-rail inputs and output and features high accuracy, low noise, and up to 4-MHz bandwidth. It can operate with supplies as low as +3 and as high as ±18 volts. It is used wherever low voltages must be handled or wide dynamic range is required, for example, in processing sensor signals. Its input common-mode range is equal to the supply voltage, and with 3-5-V supplies, the output swings to within 150 mV of V_S and 125 mV of ground (1-mA load).

It has low offset (≤ 65 µV, E grade, 3-to-5-V supplies) and drift (165 µV over temperature), as well as low noise (3.9 nV/√Hz). Its slew rate is 2.4 V/µs, and it settles to 0.01% in 2.5 µs (1-V step). The operating temperature range (E & F grades) is –40 to +85°C. Prices start at $2.93 (1000s). **Circle 21** ▶

Dual 600-MHz, 50-mW I-Feedback OA
AD8002 is a dual version of AD8001 in 8-pin plastic
Excellent differential gain & phase: 0.01% & 0.02°

The AD8002 is a dual version of the popular AD8001 (*Analog Dialogue* 28-2, page 11); it can be used to amplify, buffer, and drive cables for high-speed signals. Typical applications demonstrating its increased "productivity" include driving differential loads with a single AD8002 and increased performance vs. power without cost increases in video circuits such as cameras and switchers. Its low distortion and fast settling make it ideal for buffering high-speed ADCs.

Typical features include: 600-MHz –3-dB bandwidth (G=+1), 60-MHz 0.1-dB gain flatness, low quiescent current (5 mA/channel), high output current (to 70 mA), low distortion (–65 dBc at 5 MHz) and 16-ns settling time to 0.1%. Proprietary transimpedance-linearization circuitry for this current-feedback device allows the AD8002 to drive video loads (for example,
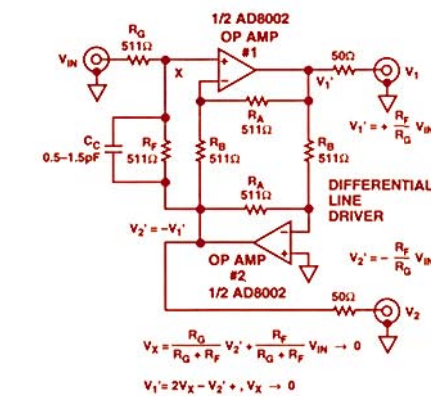
up to 8 back-terminated 75-Ω loads) with excellent differential gain and phase performance on 50 mW/channel.

The AD8002 operates on ±5-volt supplies and is available in 8-pin plastic mini-DIPs and SOICs for the –40 to +85°C operating temperature range. It is priced at only $3.50 (1000s), i.e., $1.75/channel. **Circle 22** ▶

Precision Low Power
OP293 dual: 45 µW/channel;
2.0-V performance specified

The OP293, a dual, precision low-power op amp, will work on voltages from +1.7 V (or ±0.85 V) to ±18 V. It is used wherever high accuracy is required at the lowest possible power. Examples include temperature-transducer amplification, portable consumer electronics, battery monitoring, medical instrumentation, process control, and safety monitoring. Key features include guaranteed performance specs at +2, +3, +5, and ±15 V, 100-µV V_{OS} with low drift, ability to sink and source 8 mA at outputs, and no-phase-reversal on overdrive.

The AD293 is unity-gain stable. In single-supply operation, its input and output ranges include ground, and the outputs swing from the negative rail to within 600 mV of V_S. It is designed for the –40 to +85° temperature range and is packaged in 8-pin plastic DIPs and SOICs. Prices (1000s) start at $2.07. **Circle 23** ▶

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Worth Reading

SERIAL PUBLICATION

DSPatch—The DSP Applications Newsletter: Number 33 (Spring/Summer, 1995) features the ADSP-21xx EZ-KIT Lite, a development system for ADSP-2181 et al, light on price, heavy on performance. Also featured: preview of the May DSPx show, and several customer systems, including RealTime Systems, Inc.'s Talisman line of ISA development boards; Cresta Systems, Inc.'s MediaModem™ conferencing, telephony, and signal processing add-in card; Signal Processing Associates' full-duplex version of G.728, or LD-CELP; Lewis Electronics' E5 series of development systems and DSP05 cards; Hyperception, Inc.'s Hypersignal® for Windows™ Block Diagram DSP software design tool; and Barco's NICAM digital audio coder; plus an article on DMA & memory overlays on the ADSP-2181, and regular features: Q&A, Up To Date, Workshop schedule, Current software releases, and Available literature. **FREE, Circle 24**

BROCHURES AND SUMMARIES

- **CMOS Switches and Multiplexers,** a 10-page guide, including tables, block diagrams, and cross-reference guides. **Circle 25**

- **Digitally Controlled Resistors,** a 4-page family summary guide to the AD8402/03 variable resistance DACs and TrimDACs. **Circle 26**

- **SHARC Processors and SHARC EZ-Kit,** 4- and 2-page product highlights. **Circle 27**

- **EZ-KIT Lite product highlights** (4 pp.). **Circle 28**

- **Three Highlights brochures for systems-level solutions using ADI DSP products: Circle 29**

    VideoCon H.320 video conferencing, 4 pp.
    ADAM 100 digital telephone answering machines, 2 pp.
    Variable speed motor control solution, 4 pp.

APPLICATION NOTES

Circuit design and applications of the ADM663A/ADM666A micropower linear regulators, by Khy Vijeh and Matt Smith. [8 pp., AN-392]. **Circle 30**

Understanding accelerometer scale factor and offset adjustments, by Charles Kitchin. [4 pp., AN-396]. **Circle 31**

Evaluation boards for single, dual, and quad op amps, by Adolfo A. Garcia. [6 pp., AN-398]. **Circle 32**

Considerations for selecting a DSP processor—Why buy the ADSP-2181 (vs. competitive fixed-point DSPs). [6 pp., AN-400]. **Circle 33** ▶

MORE AUTHORS [*Continued from page 2*]

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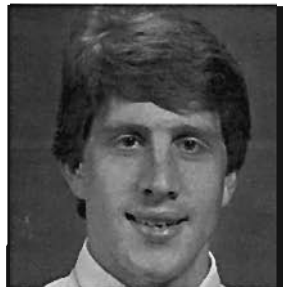
Bob Clarke (p. 9) is Senior Product Marketing Engineer in ADI's Communications Division at Wilmington, MA. His photo and a biographical sketch appear in *Analog Dialogue* 28-2.

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Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS—NEW PRODUCTS

Amplifier, voltage feedback, 160-MHz rail-to-rail, specified for +3, +5, and ±5 V, with Disable, saves power. **AD8041. Circle 36**

Quad precision low-power op amp. **OP493. Circle 37**

Quad rail-to-rail op amp with OP-27 performance. **OP484. Circle 38**

Complete 10-bit 40-MSPS sampling ADC. **AD9050. Circle 39**

12-Bit, 3-MSPS ADC (upgrade of AD1671): **AD1672, Circle 40**

High-output-current differential driver. **AD815. Circle 41**

Laser-diode driver, 1.5 ns rise time, 2.0 ns fall time, 200-MHz switching, 200-mA output current **AD9660. Circle 42**

NEW LITERATURE

Practical Analog Design Techniques (New book made available during the recent seminar series, 428 pages). **Use the book-purchase card.**

"Solutions for GSM/DCS-1800/PCS-1900" (12-page brochure describing chipsets and future plans for wireless market). FREE. **Circle 43**

Slide guide: standards & products for wireless. FREE. **Circle 44**

DATA SHEETS, ERRATA • • • The OP295/495 amplifier has a new data sheet (Rev. B), including correct dimensions for SOL-16 package and improved noise specs. **Circle 45 • • •** There's an errata sheet for the Rev. 0 AD608 mixer/limiter/RSSI data sheet. It adds a LO spec: –16 dBm, with 50-Ω input termination—and corrects Figure 22 (pin 14 connects directly to VPOS only, and R4 connects pin 15 to Powerup 3V CMOS). If you have the Rev. 0 data sheet, but no errata information, **Circle 46 • • • AD1845 data sheet has an erroneous functional block diagram.** A "Rev A" sticker is available until the new data sheet becomes available. **Circle 47 • • • ADG608/609 Multiplexer data sheet, Rev. 0, as originally printed, has an incorrect TSSOP package diagram,** page 11. All data sheets now furnished cover it with a sticker having the correct information. If yours doesn't, **circle 48 • • •** A new **AD2S99 Programmable Oscillator data sheet (Rev. B)** is now available. **Circle 49**

PRODUCT NOTES • • • Evaluation boards are available—at reasonable prices—for many new Analog Devices ICs. They will help you with the speedy evaluation and design-in of a product. Consult the Sales force • • • Analog Devices offers a large number of **products in tape and reel** packaging in conformance with EIA Standard 481-A, "Taping of surface-mount components for automatic placement." For information on our tape and reel devices, consult the Sales force • • • The number and variety of ADI **products suitable for PCM (a.k.a. PCMCIA) card designs** continues to increase. For current information, consult the Sales force • • • Likewise, the number and variety of **products for 3-V operation** is growing. Consult the Sales force • • • **Single-supply op amp "Sample Packs"** offer five 3-V products per pack. Contact your local sales office or distributor while supplies last • • • The excellent performance, lower cost, and ready availability of the **AD1877 single-supply 16-bit stereo ADC** may make it an interesting design option when AD776-like performance is required. An extended-temperature-range (–55 to +105°C) version of the AD1877 is also available.

STANDARDS AND MILITARY • • • Analog Devices manufacturing facilities in Limerick, Ireland; Wilmington, MA; and Santa Clara, CA have received **ISO-9001 certification**—and our manufacturing facilities in Norwood, MA, and Greensboro, NC are likely to have received theirs by the time you read this. Our manufacturing facilities in Walton, England; Manila, Philippines; and Taiwan have received **ISO-9002 certification.** For information, consult the Sales force • • • Analog Devices maintains its commitment to long-term support of the military market. To help customers who may be in doubt of availability of MIL-grade parts from other suppliers, **a cross-reference guide of recommended Analog Devices military-grade parts is available. Circle 50**

PATENTS • • • 5,394,078 to A. Paul Brokaw for **Two-terminal temperature transducer having circuitry which controls the entire operating current to be linearly proportional with temperature • • •** 5,396,608 to Douglas Garde for **Method and apparatus for accessing variable length words in a memory array • • •** 5,398,048 to Denis O'Mahony for **Integrated-circuit chip and system for developing timing reference signals for use in high-resolution CRT display equipment • • •** 5,404,142 to Robert Adams and Tom Kwan for **Data-directed scrambler for multi-bit noise shaping D/A converters • • •** 5,406,222 to A. Paul Brokaw for **High-gain transistor amplifier • • •** 5,409,845 to Derek Robinson, William Krieger, Andre Martinez, and Marion McDevitt for **Method of making complementary bipolar polysilicon emitter devices • • •** 5,412,385 to Christopher Mangelsdorf for **Error correction testing system and method for a multistage A/D converter • • •** 5,412,387 to Scott Vincelette, Paul F. Ferguson, Jr., and Robert Adams for **Error reduction in switched capacitor digital-to-analog converter systems by balanced sampling • • •** 5,414,390 to Janos Kovacs and Ronald Kroesen for **Center frequency controlled phase locked loop system • • •** 5,416,691 to Rosamaria Croughwell for **Charge pump circuit • • •** 5,417,111 to Steven J. Sherman, Robert W. K. Tsang, Theresa A. Core, and A. Paul Brokaw for **Monolithic chip containing integrated circuitry and suspended microstructure • • •** 5, 418,386 to Francisco Dos Santos, Jr., and Larry M. DeVito for **Circuit construction for controlling saturation of a transistor • • •** 5,418,491 to Derek F. Bowers for **Operational amplifier compensation circuit for preventing phase reversal and maintaining performance for inputs outside the common-mode range • • •** 5,418,498 to Lawrence DeVito and John McNeill for **Low jitter ring oscillators • • •** 5,420,540 to James R. Butler for **Double-folded cascode operational amplifier • • •** 5,422,510 to Brad Scharf, Faran Nouri, and Shaheen Mohamedi for **MOS transistor with non-uniform channel dopant profile • • •** 5,422,583 to John Blake, Anthony Gribben, and Colin Price for **Back gate switched sample and hold circuit • • •** 5,422,588 to John Wynne for **Low-distortion CMOS switch system • • •** 5,422,601 to Janos Kovacs, Steven Robinson, and Wyn Palmer for **Hybrid analog digital automatic gain control gain recovery system • • •** 5,424,510 to Alex Gusinov, A. Paul Brokaw, Douglas Babcock, Lewis Counts, Lawrence DeVito, Robert Duris, and Scott Wurcer for **Circuit and method of providing thermal compensation for a transistor to minimize offset voltage due to self-heating of associated devices • • •** 5,424,670 to Howard Samuels and Scott Wayne for **Precision switched capacitor ratio system • • •** 5,436,629 to Christopher W. Mangelsdorf for **Multi-stage A/D converter • • •** 5,438,373 to Timothy J. Cummins for **System for developing CRT color-intensity control signals in high-resolution CRT display equipment.**

HOW TO GET HELP FROM ANALOG DEVICES

Customer assistance help line:	**1-800-262-5643**	(1-800-ANALOG-D) (U.S.A.)
Literature Center: Phone	617-461-3392	Data sheets, books, application
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Analog Dialogue, Volume 29, No. 2, 1995

PRINTED IN U.S.A.

AD29.2-8/95