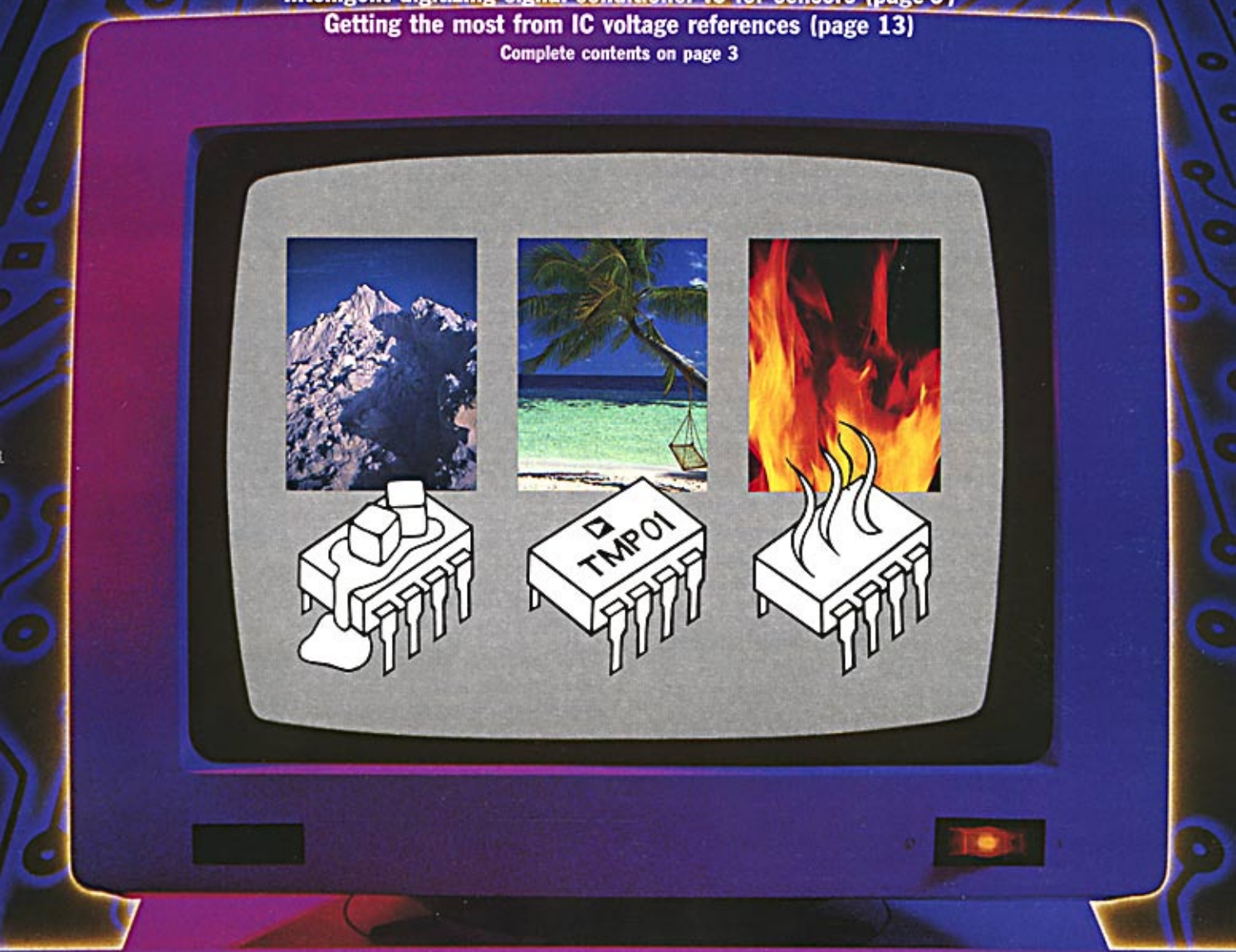
Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 28, Number 1, 1994

ANALOG DEVICES

Editor's Notes

A QUARTER CENTURY OF EDITOR'S NOTES

Three years ago, we celebrated 25 years of publication of *Analog Dialogue*. Recently the realization came that the undersigned has passed a quarter-century as editor, having entered the scene with volume 3. In those early days, we decided to include this column as a channel for saying some things that didn't quite fit into the publication's mission of straightforward technical communication about technologies, principles, products and applications—but might nevertheless be useful or of interest.

Over the years, we have commented on: new technologies and products introduced in the following pages; progress of technology at Analog Devices; milestones for the company, the industry, this publication, and its editor; things we have learned lately or during our career; major honors received by Analog Devices technologists.

New technologies and products we have heralded included analog CMOS (7-2,1973) and the first CMOS 10-bit DAC (AD7520—8-1,1974); digital signal processing chips (17–1,1983) and the highly parallel ADSP-2100 processor (20–2,1986). In fairness, there were, of course, others with a somewhat less glowing track record (but let them R.I.P!)

Company milestones commented on included our acquisitions of Nova Devices (which became Analog Devices Semiconductor, 6–1,1972), of Computer Labs (13-1,1979), and of Precision Monolithics, Inc. (24-3,1990). Industry milestones included celebration of the 30th anniversary of the commercial introduction of the differential op amp in 1952 (16-3,1982), the passing of analog pioneer George Philbrick (9-1,1975)—and of Teledyne Components, the final descendant of the company he founded (26-1,1992).

Colleagues whose honors have been noted include Barrie Gilbert (by IEEE, 18–3,1984 and 26-1,1992), Richie Payne (by IEEE, 24–1,1990 and 27-1,1993), Paul Brokaw (by IEEE, 25-1,1991), Bob Adams (by AES, 25–2,1991), and Ray Stata (by NAE, 26–2,1992).

Our own personal favorites included "Multiplier Memories and Meanderings" (5-1,1971), the reaction of an analog engineer (who knew at first hand the monster multipliers used in analog computers) to the single-chip AD530, the first complete monolithic analog multiplier—and the sequel, "Multiplier Meaderings—Revisited" (23-1,1989), celebrating the arrival of the 500-MHz AD834.

Another was the confession, "Personal analog-to-digital conversion" (11-1,1977). No, this was not about ADCs for personal computers. It was a chronicle of guilt that had to do with the fall from (analog) grace to the temptations of the digital world: for example, the abandonment of the slide rule (a faithful companion of some 32 years) in favor of the scientific pocket calculator.

Yet another was "DSP Microprocessor?" which accompanied the introduction of our ADSP-2100 (20-2,1986). It sought to answer the question, "Isn't it somewhat unseemly for a nice 'Analog IC' company to be designing a microprocessor?". ▶

Dan Sheingold

[Note: For a copy of any of the above, send a message to Dan Sheingold c/o our Literature Center or a direct e-mail (dan.sheingold@analog.com).]

THE AUTHORS *(More authors on page 30)*

Joe Buxton (page 3), a Senior Application Engineer for the PMI Division of Analog Devices, has worked extensively on the development of SPICE op amp models; he writes application notes and articles for publication and also helps customers resolve their circuit and design problems. In 1988, Joe received a BSEE from the University of California, Berkeley. In his leisure time, he enjoys bicycling, hiking, skiing, and listening to music.

Dan Williams (pp. 6 & 8), a Technical Publicity Specialist in Norwood, writes technical articles and is responsible for press releases and press relations. Earlier in his 10 years at ADI, he was a Product Engineering Technician on IC V/Fs, then worked with a variety of hybrids. His interests include concert sound reinforcement, motorcycle observed trials, and photography.

Bob Adams (page 9) has been Manager of Audio Technology at ADI since 1989, designing sigma-delta ADCs and DACs; most recently, he led the AD1890 design team. He has a BSEE degree from Tufts U. (1976). Before joining ADI, Bob was Director of Audio Research at dbx; among his designs was an 18-bit Σ-Δ ADC. A Fellow of AES, he holds many audio signal processing patents. In spare time, he plays the sax in jazz bands; at home, he and his wife, Susan, are kept very busy with their two children.

Walt Jung (page 13) is a Corporate Staff Applications Engineer at ADI. Earlier he consulted on applications projects, and wrote a variety of application notes and articles for *Analog Dialogue* and the trade press. He has authored ten books (e.g., *IC Op Amp Cookbook*) and hundreds of articles on linear-IC applications. Walt attended Drexel Institute of Technology, is a member of IEEE and a Fellow of the AES. He enjoys live & recorded music—and designing circuits for the latter.

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Dual Set-Point Single-Chip Temperature Controller

TMP01 provides precision temperature sensing and on/off control in a single device

by Joe Buxton

The TMP01* is a new type of monolithic temperature sensor that not only measures temperature; it also includes a voltage reference and two comparators for use in temperature control. The temperature-dependent output, 5 mV/K, provides straightforward readings of the device's ambient temperature (hence the local temperature of the entity being measured) for operating temperature ranges up to $-55°C \leq T_A \leq +150°C$.

The two comparators, which can be used for making decisions based on the difference between the measured temperature and a reference value, provide considerable utility and flexibility. Their outputs, open-collector transistors, can directly control the switching of external temperature-control elements for such functions as turning on fans or heaters, giving out-of-range warnings, or signalling thermal shutdown. With only three external resistors, the comparators' input thresholds can be adjusted to any temperature within the device's operating range.

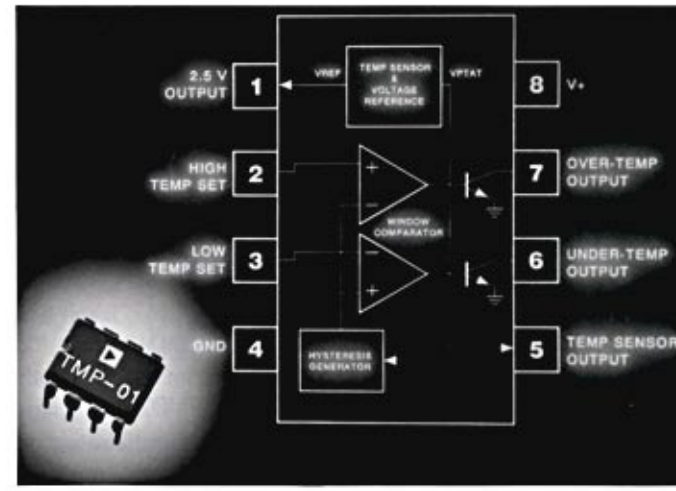
A significant advantage of a monolithic temperature sensor using the TMP01's principle is that the output is inherently linear, with constant sensitivity of 5 mV/K over the chip's entire operating temperature range. Most traditional temperature sensor devices, such as thermocouples, thermistors, and RTDs, have inherent non-linearities and require additional linearizing hardware or software to measure the temperature accurately. In contrast, the temperature output of the TMP01 can be used directly without additional circuitry, simplifying system design.

In addition to linearity, the device has substantial sensitivity—5 millivolts of output per degree. Such a change is 100× easier to deal with than, for example, the 51-μV/°C of a J-type thermocouple when used over a comparable range.

The easiest way to visualize the function of the two comparators is to think of a thermostat, which controls the heating and cooling of a room. When the temperature drops below a certain set-point, the thermostat turns a heater on to bring the temperature up. Likewise, if the temperature rises above a preset level, the thermostat turns on a cooling system to bring the temperature back down. When the temperature is between the low set-point and the high set-point, neither the heating nor the cooling system is activated. The TMP01's comparators behave similarly. One comparator, labeled "SET HIGH", signals when the temperature rises above its set point, and the other comparator, "SET LOW", switches when the temperature drops below its threshold.

The TMP01's comparator outputs can be configured to control a variety of functions; the thermostat is just one example. Each

*Use the reply card for technical data. Circle 1



output, an open-collector transistor, pulls low when its comparator trip point is reached. With low supply voltage (for minimal incremental heating) and a current-sink rating of 20 mA, the outputs cannot directly control high voltages and currents; they can nevertheless provide substantial currents for relays, triac drivers, and various high-power discrete transistors.

Another excellent example of the TMP01's usefulness is as a thermal watchdog in a system. When a temperature being monitored, perhaps of a pc board or a component on that board, reaches a pre-determined (possibly dangerous) level, the TMP01's "SET HIGH" comparator switches low, signaling a shutdown circuit to reduce the power level. Once the temperature has fallen by a given amount to a safe level, the output returns high, allowing the system to return to normal operation.

As with any contact sensor, to ensure proper results, the TMP01 package needs a good thermal connection so as to be at the same temperature as the entity being monitored. Any temperature gradient between the measurement subject and the TMP01 can result in inaccuracies, delays, and even control instabilities.

HOW THE TMP01 WORKS

To understand how the TMP01 functions, look at Figure 1. The basic voltage reference and temperature sensor is a bandgap circuit not unlike those described in the article starting on page 13. It produces a dc voltage proportional to absolute temperature (PTAT). In a reference circuit, the PTAT voltage is used to compensate for the complementary temperature variation of a

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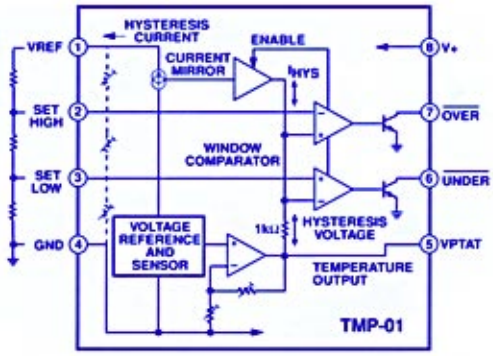


Figure 1. Block diagram of the TMP01

junction and produce an essentially invariant version of the bandgap voltage. In this case, the PTAT voltage is used for temperature measurement (with the associated constant reference as a bonus for accurately scaling the decision points. The PTAT voltage is scaled to 5 mV/K, which means that at 25°C (298 K), the output is 1.49 V, ranging from 1.09 V at −55°C to 2.115 V at +150°C. VPTAT is buffered by an internal amplifier to provide a low-impedance output at pin 5.

Briefly, the TMP01, like other solid-state temperature sensors, relies on a fundamental property of silicon transistors: if two identical transistors are operated at a constant ratio of collector current densities, R, then the difference in their base-emitter voltages will be (kT/q) ln R. In this equation, Boltzmann's constant, k, and the electron charge, q, are constants; and, assuming a well-designed circuit, the ratio of the current densities, R, is also constant. The absolute temperature, T, is the only variable. Thus the voltage is directly proportional to temperature, with excellent linearity over the TMP01's operating temperature range. Nonlinearity or inaccuracies are due to minor residual curvature and other temperature drifts of such entities as the output buffer, internal impedances, and the collector current ratio, R. Because the entire circuit is fabricated on a single die, the characteristics of the transistors and resistors are well matched to each other, minimizing any temperature-related drifts.

The bandgap voltage in the TMP01 produces a stable +2.5-V reference output, which is handily available for setting accurate set-points on the inputs of the comparators. The reference voltage was designed to be stable over the operating temperature range of the device, with a drift of only 10 ppm/°C.

As Figure 1 shows, the output of the reference is connected to an external resistance ladder; it has two functions. The *division ratios* of the resistors connected to the reference voltage set the inputs of the comparators to the precalculated switching voltages—corresponding to the temperatures at which the comparators should trip. In addition, the *magnitude* of the current drawn by the divider (= 2.5 V/ΣR) sets the comparators' hysteresis.

For example, to set one of the comparators to trip at +40°C, the voltage on its input (pin 2 or pin 3) should be set to (273 K + 40°C) × 5 mV/K = 1.565 V, which means a divider ratio of 1.565 V/2.5 V = 0.626 at the appropriate pin (complete resistor-programming information is available in the data sheet.)

The second important function of the resistor chain is to set the hysteresis on the comparators. If the voltages on both inputs of any comparator are approximately equal, it can be turned on and off rapidly by input noise, resulting in an undesirable "rattling" effect, for example, cycling a heater rapidly. This problem is exacerbated in temperature-sensing applications, where input voltages change relatively slowly. To avoid noise-caused "oscillations", hysteresis is needed. Figure 2, a plot of hysteresis outputs vs. input, shows how hysteresis affects the set-points. When either comparator trips, a hysteresis current flows through a 1-kΩ resistor. The voltage drop across the resistor adds to the VPTAT voltage, thus offsetting the voltage (and hence temperature) at which the comparators will switch back.

Take the example of TSETHIGH = 70°C and a hysteresis of 5°C (25 mV). When the temperature increases to 70°C, the output of the comparator turns-on the output transistor, pulling the collector low. At the same time, the hysteresis is activated by causing 25 μA to flow through the 1-kΩ resistor, shifting the trip point to 65°C. Thus, the temperature needs to fall below 65°C before the output returns high.

Where does the hysteresis current come from? A current mirror reflects the reference output current (plus a fixed 7-μA bias) back through the 1-kΩ resistor, thus determining the hysteresis voltage after a comparator switches. Hysteresis is set by appropriately choosing the total resistance of the resistor chain between pin 1 and ground. When resistance is high enough to produce a current ≤ 7-μA fixed bias, the hysteresis goes to zero. Because the output current of the device is used to set the hysteresis, the reference should not drive any unknown loads directly. If the precise 2.5 V is needed elsewhere, the VREF output should be buffered by an amplifier with high input impedance.

APPLICATION

Pulsewidth-modulation control of a cooling fan: Many systems require a cooling fan to ensure that components do not overheat. In most cases, the fan is hard-wired to 12 V dc (or other appropriate supply), consuming a large amount of power and producing excessive noise. However, constant power may be unnecessary because maximum cooling is not always needed. By using a TMP01 in combination with a triangular-wave dither generator, a simple pulse-width-modulated fan controller is developed that varies the speed of the fan versus temperature, so the fan is off at low temperature and smoothly ramps up to full speed at a user-determined high temperature. The result is reduced power and noise.

The circuit to perform this function is shown in Figure 3. Note that only one of the comparators of the TMP01 is used; the unused comparator is disabled (good practice) by tying its input to +5 V. The output of the "SET LOW" comparator controls the gate voltage of a high-power MOSFET. Normally, the "SET LOW" comparator controls heating and the "SET HIGH" comparator controls cooling, so it may appear counter-intuitive to use the "SET LOW" comparator to control the cooling of a system. However, in this case, the polarity of the MOSFET's gate control is the key, as explained below.

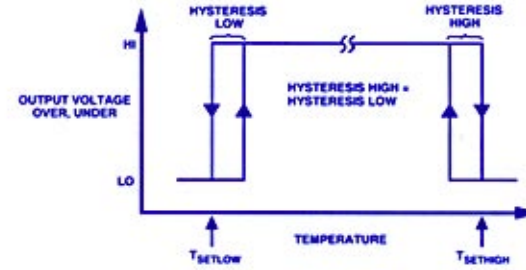


Figure 2. TMP01 hysteresis profile.

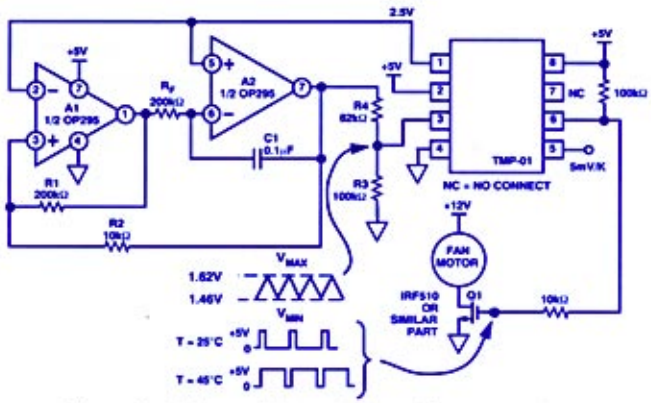


Figure 3. Pulse-width-modulated fan controller.

The OP295 rail-to-rail dual op amp is used to generate an accurate triangle wave from a single +5-V supply, and the voltage reference of the TMP01 biases the generator midway between the supplies at +2.5 V. Since the voltage reference is driving only their high-impedance inputs, no output current flows—thus no hysteresis is generated within the TMP01.

Amplifiers A1 and A2 form a conventional comparator-integrator triangular-wave generator. A1 is configured with positive feedback to form a comparator with hysteresis. When the voltage at its + input becomes greater than 2.5 V, its output switches to +5 V and pulls its + input up by an amount determined by the ratio of R_1 and R_2. Its output is integrated with negative polarity by A2, causing the input to A1 to decrease linearly until its + input drops below 2.5 V, causing its output voltage to drop to ground, and its + input to be pulled down by an amount determined by the ratio of R_1 and R_2. A2 integrates back up, and the cycle repeats. For the values of R_1 and R_2 shown, the output of A2 is a triangular wave that swings from 2.37 V to 2.63 V.

The frequency of the triangular wave is determined by A2's integration time constant, R_FC_1, which determines the rate at which the output of A2 ramps. For this circuit, these components are set to give an oscillation frequency of 240 Hz. A significant advantage of using the OP295 is its rail-to-rail output swing, mentioned above. This gives a symmetrical triangular wave about 2.5 V, with accuracy depending only on that of the +5-V power supply. When necessary, a stable voltage source, such as a 5-V reference, should be used to supply the small amount of power required (a little more than 1 mA total for both devices)

The triangular wave is attenuated by R3 and R4 to bring it within the operating region of the TMP01. In this case, the signal is scaled to swing from 1.46 V to 1.62 V on the input to the TMP01's comparator, as shown in the figure. These voltages correspond to 20°C and 50°C, respectively. The comparator compares the triangular wave on its positive input with the TMP01's 5 mV/K on its negative input.

When the temperature is < 20°C, the TMP01's voltage is less than (293 K) × (5 mV/K) = 1.46 V; hence the comparator's negative input is always below the triangular-wave voltage on the positive input. Thus, the comparator's output is high, which turns the open-collector output transistor on and pulls the gate of the *n*-channel FET low. In this state, the gate-to-source voltage is essentially zero, turning off the MOSFET, Q1, and no power is applied to the fan. As the temperature rises above 20°C, the TMP01's voltage rises above 1.46 V and the comparator switches, turning off the open collector output. The 100-kΩ pull-up resistor brings the gate of Q1 high, turning it on and current flows briefly through the fan motor. As the temperature increases further, the open-collector output's duty cycle increases and remains high for a longer interval in each period of the triangular wave, resulting in more power applied to the fan.

Typical waveforms showing the gate drive of the MOSFET are included in the figure to illustrate the change with temperature. As the power to the fan increases, its speed increases, providing additional cooling to the circuitry. If the temperature rises above 50°C, the TMP01's voltage will increase to above 1.62 V, causing the open collector output to remain high for the entire period of the triangular wave. In this case, the fan receives maximum power and spins at its top speed.

To determine the resistance values for other temperature settings follow these steps: First the maximum and minimum temperatures for fan operation need to be converted to voltage:

$$V_{MAX} = (T_{MAX}(°C) + 273°) \times 5\ mV/°C$$

$$V_{MIN} = (T_{MIN}(°C) + 273°) \times 5\ mV/°C$$

The values of R_3 and R_4 are determined next. R_3 should be relatively large to minimize power dissipation; it is 100 kΩ in this case. R_4 is then calculated to scale the triangle-wave generator's center voltage (2.5 V) to the average voltage of V_{MIN} and V_{MAX}, according to the following equation:

$$R_4 = \frac{5\ V - (V_{MIN} + V_{MAX})}{V_{MIN} + V_{MAX}} R_3$$

R_2 is arbitrarily chosen as 10 kΩ to provide an adequate impedance level. R_1 is then calculated to produce enough hysteresis such that amplifier A1 switches at the desired maximum voltage. This voltage is simply V_{MAX} divided by the attenuation of the resistor divider formed by R_3 and R_4. A computation based on V_{MIN} could also be used because the triangle wave is symmetrical around the center point.

$$R_1 = \frac{2.5\ V}{V_{MAX}\dfrac{R_3 + R_4}{R_3} - 2.5\ V} R_2$$

Finally, the frequency of oscillation is based on the signal swing of the triangular wave and the integration time constant:

$$Frequency = \frac{2.5\ V}{2\ R_FC_1\ (V_{MAX} - V_{MIN})\dfrac{R_3+R_4}{R_3}}$$

With the above set of design equations, a pulse-width-modulated fan controller can be designed for a variety of temperature ranges using only 2 ICs, a power MOSFET, and a handful of discrete components.

This example is just one of a wide range of applications for which the TMP01 is well-suited. Whether it is to monitor the temperature of a system via the voltage output, to control the switching of heating and cooling elements, or to ensure long term reliability of components by initiating a thermal shut-down, the TMP01 provides a high level of functionality in a very easy-to-use part. The TMP01 is available in versions for −40 to +85°C and −55 to +150°C and is packaged in 8-pin DIPs, SOICs, and TO-99 cans. Prices begin at $2.75 (100s).

The TMP01 was designed by Jonathan Audy at Analog's PMI Division, Santa Clara, California.

Intelligent Digitizing Signal Conditioner IC for Sensors

AD1B60 provides excitation, conditioning, compensation, linearization, and a/d conversion

by Dan Williams

The AD1B60 is the first of a new generation of intelligent, sensor-interface ICs to greatly simplify the design of multi-sensor systems. The AD1B60 provides a flexible, accurate, complete interface to a wide variety of sensors. With it, the interface for a new sensor can be designed in minutes rather than weeks. Industrial OEMs need no longer design, manufacture and stock many sensor interfaces; the AD1B60's intelligence and versatility can make sensor selection as simple as clicking on an icon.

What is the AD1B60* The AD1B60 is a complete, configurable, sensor-to-digital signal-conditioning subsystem IC for the process industry (Figure 1). Accepting input directly from thermocouples (TCs), RTDs, and volt- or millivolt sources, it performs excitation, compensation, scaling, and linearization; and it outputs data in engineering units over a pair of serial interfaces.

Combining an embedded microcontroller and a proprietary mixed-signal ASIC, the AD1B60 data-acquisition subsystem can stand alone or be seamlessly integrated into larger systems. The mixed-signal ASIC at its heart contains a high-resolution, noise-rejecting integrating A/D converter, a multiplexer, programmable-gain amplifier, reference, and excitation sources. The µcontroller, with on-board RAM and EEPROM, provides compensation and linearization—and controls communication through 2 serial ports.

Why the AD1B60? Because the signals generated by most sensors are low-level, sensitive to interference, and often nonlinear, it's usually necessary to condition (amplify, filter, linearize) these signals before meaningful information can be extracted for use by the process-control system. In the past, this was done using signal conditioning modules, one for each type of TC, RTD, strain-gage and volt/millivolt source, as well as custom modules for non-standard transducers.

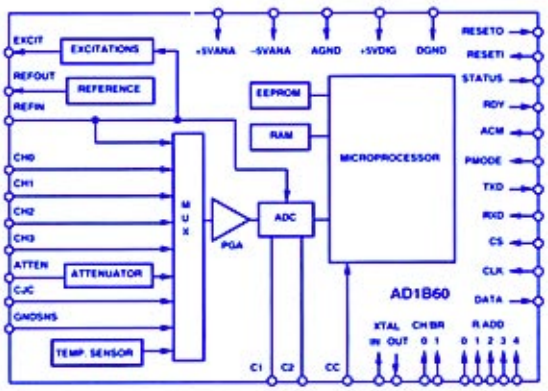


Figure 1. Functional block diagram of the AD1B60.

*Use the reply card for technical data. Circle 2

The AD1B60 teams sensors with the power of a microcomputer, continuing the trend of distributed processing and the migration of intelligence outward toward the sensor. Distributed processing has many advantages over core-computer processing:

- Virtually noise- and degradation-proof high-level digital signals can replace low-level analog signals in long cable runs.
- Wiring is greatly simplified; multiple channels of digital data can be carried by a single cable or optical fiber.
- Redundancy in the system allows system-wide fault tolerance.
- Local faults can be quickly detected without complex system diagnostics.
- Local parameters can be programmed remotely.
- Controllers can isolate and monitor non-related subsystems independently.
- Control software is reduced in complexity.

Thermocouples: These simple devices perform much of the sensing of temperature, the most widely measured parameter. Many kinds of TCs are in use today, optimized for temperature range and physical characteristics. They operate on the *Seebeck* principle: if two different conductors are joined in an open loop and the junctions are at different temperatures, a voltage will be generated roughly proportional to the difference in temperature. Fortunately the nonlinearities inherent in each type (junction pairs) are well known, and the output can be calibrated or compensated to provide a relatively accurate temperature reading.

But in practice the temperature at one junction must be known to determine temperature at the other. Before electronic methods of *cold-junction compensation* (CJC) were available to simulate the reference junction, calibration was often performed by immersing the reference junction in a 0°C ice bath, hence "cold junction".

The AD1B60 provides linearization and CJC for seven NIST-standard TC types (J, K, T, E, R, S and B) in ROM. Other TCs (e.g., type N) can be accommodated by downloading calibration and compensation parameters into the on-board EEPROM. Four modes of CJC can be employed: an external thermistor connected between the CJC-pin and analog ground; a silicon temperature sensor, such as the AD592; or a user-downloadable value stored in EEPROM. The internal CJC calculation can also be disabled and an analog CJC IC, such as the Analog Devices AC1226 (*Analog Dialogue* 23-4, p. 18) can be connected to the input.

Figure 2 shows the connections required for a single-channel TC input. Here, a thermistor CJC sensor is used; besides powering it, the AD1B60 also provides excitation current for open-circuit detection. Up to four different TCs, sharing a single CJC, can be measured by using the AD1B60's built in multiplexer.

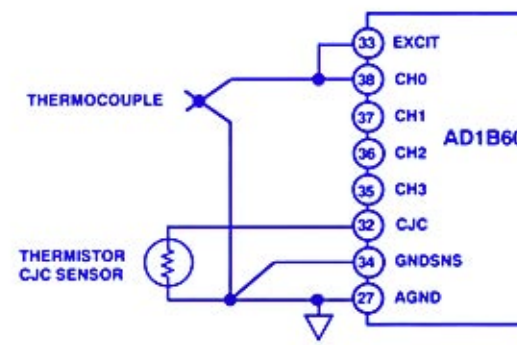


Figure 2. Typical single-channel thermocouple connection.

RTDs: Resistance thermal detectors (RTDs) use a conductor with a known temperature coefficient fabricated into a wound coil, film or foil grid. Because of platinum's insensitivity to contamination and ability to operate over a wide temperature range, it is the resistance element of choice for most RTDs. Figure 3 shows a typical connection for a single channel. The AD1B60 has built-in algorithms to linearize 100-Ω platinum RTDs (α=0.00385 and 0.00392). Lead compensation is provided for both 3- and 4-wire connections, and 200-μA excitation current.

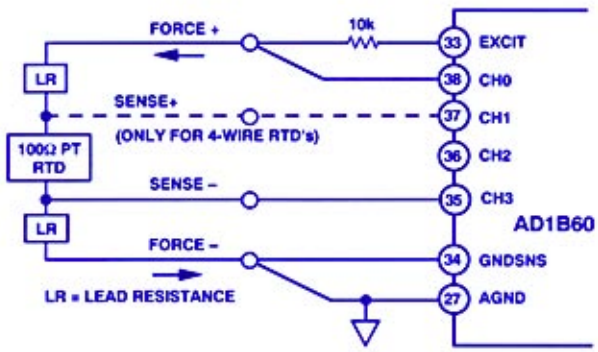


Figure 3. 1B60 with single-channel RTD input.

Volt and millivolt sources: The AD1B60 provides 10 ranges of accurate measurement for any voltage source—from ±10 mV to ±10 V. An input multiplexer provides four low-level channels for up to four sources with similar <±2 V ranges and sharing a common ground, plus one channel with built-in 5:1 attenuator for signals up to ±10 volts. The multiplexer output level is matched to the input range of the high-resolution A/D converter by a precision programmable-gain amplifier.

Accuracy (linearity, calibration): The AD1B60 is fully calibrated at the factory, with calibration coefficients stored in the on-board EEPROM. The serial interface allows them to be changed in the field or for unique measurement situations.

Automatic span compensation: maintains the AD1B60's accuracy. When a measurement is taken, both input and reference voltages are measured with respect to ground at the appropriate gain. The ratio of the two measurements is used to compensate for gain and offset drift of the ADC. Recalibration is not required when the range is changed. The AD1B60's charge-balancing A/D converter's continuous self-calibration provides overall accuracy to <0.2°C typical (0.005% in volt mode), with 0.15°C resolution.

Communication: Communication is provided by two serial-interface ports: An industry standard asynchronous bidirectional port and a high-speed three-wire synchronous output port. To recover from communications errors the AD1B60 will detect breaks sent from a host computer and reset its communications processes. Invalid address command code or CRC are ignored.

The asynchronous bidirectional port can be used to accept commands and to output data directly in engineering units (e.g., °C, mV), using single-precision IEEE floating-point format, operating in half-duplex mode, with 2400-bps to 19,200-bps programmable baud rate. A 16-bit integer format is also available.

The high-speed synchronous port, capable of data *read* rates as high as 5 Mbps, outputs integer data in 16 bit twos-complement or offset-binary formats. Both ports operate independently and can be accessed simultaneously. Serial data transmission greatly simplifies the task of isolation, required in many applications. With each conversion, the AD1B60 reports status information, input channel, and an overflow flag. The AD1B60 is addressable; ≤ 32 devices can be connected to a single communication port.

Programmability: Configuration parameters are programmable both prior to installation and in the application. For flexibility in system design, almost every parameter is accessible through the bidirectional port; a central computer can control many AD1B60s.

Besides the standard TC-voltage and platinum-RTD ranges, the 1B60 includes two software-programmable custom ranges, which can be downloaded and stored in EEPROM.

Table 1. Inputs and Hex Codes

Voltage input ranges:

mV:	±10	±20	±50	±100	±200	±500;	V:	±1	±2	±5	±10
Code:	00	01	02	03	04	05		06	07	08	09

Thermocouple and RTD inputs, type and range, code:

J: 0-760°C,	K: 0-1000°C,	T: – 100-+400°C,	E: 0-1000°C,	R: 500-750°C
0A (default)	0B	0C	0D	0E

S: 500-750°C,	B: 500-1800°C,	100-Ω Pt RTDs: – 200 to +800°C	
		α=0.00385	α=0.00392
0F	10	11	12

Not used	**User Range 1**	**User Range 2**
13 to 1D	1E	1F

Power-up configuration is determined by either pin-strapping or values stored in EEPROM. The pin-strapped input range, sensor type, integration time and device configuration allow the AD1B60 to act as a stand-alone sensor-to-digital subsystem in applications where central computer control is unnecessary or unavailable. Battery backups, trim resistors, or user-developed calibration software are eliminated by the availability of EEPROM to store default- and user-specified configuration and calibration values.

System Reliability: Great care was taken with the on-board microcontroller software to make the AD1B60 extremely fault tolerant and able to recover quickly from both local and system wide errors—a major concern in process control system design. The AD1B60 includes a brownout detector and watchdog monitor. If any supply drops below a prearranged threshold, or if the microcontroller fails to trigger the watchdog timer, a *reset* is generated to re-initialize to the last configuration. Configuration data stored in EEPROM eliminates a need for battery back-up.

Design Aids: Despite its internal complexity, the AD1B60 is a straightforward device to use. To help OEMs integrate it into their designs, an evaluation board is available. Included are a buffered RS-232 port, clock crystal, voltage reference, CJC thermistor, and configuration switches, plus a companion IBM PC™-compatible disk containing a demonstration program and library of additional ranges—and a comprehensive users' manual.

The AD1B60BJ is packaged in a 44-pin JLCC, specified for the industrial (–25 to +85°C) operating temperature range. It will also be available in a 64-pin PQFP. Prices begin at $39.30 (1,000s).

The 1B60 was designed at ADI's Transportation and Industrial Products Division by a team led by Howard Samuels.

IC Vector Processor for Motor Control

AD2S100 performs vector rotations of three-phase and two-phase 90° sine & cosine signals

by Dan Williams

Most of the power supplied to washing machines, conveyor belts, air conditioners, elevators and refrigerators is used to drive motors. In choosing a motor, reliability and performance must be balanced with cost and complexity of control.

Although it is one of the most widely used motors, the three-phase induction motor is not easily controlled. A technique called "field-oriented control" promises to provide precise control of torque, speed and position for ac induction motors—allowing these inexpensive workhorses to be used in precision servo applications. The AD2S100* ac vector processor, a mixed-signal IC, greatly simplifies the design of field-oriented induction motor systems.

Motor principles: To understand what the AD2S100 does, a basic understanding of motors is necessary. Conceptually simpler than the induction motor, the dc permanent-magnet synchronous motor (PMSM) provides a good starting point. The dc PMSM's input is commutated to produce a rotating magnetic field in the air gap between the stator and rotor. Permanent magnets attached to the rotor continually seek to line up with the stator's rotating field, turning the rotor with torque equal to the product of the magnetic force and the rotor's diameter. Figure 1 shows the relationship between rotor and stator flux. The rotor normally turns at the same speed as the stator field, with a phase lag that depends on load.

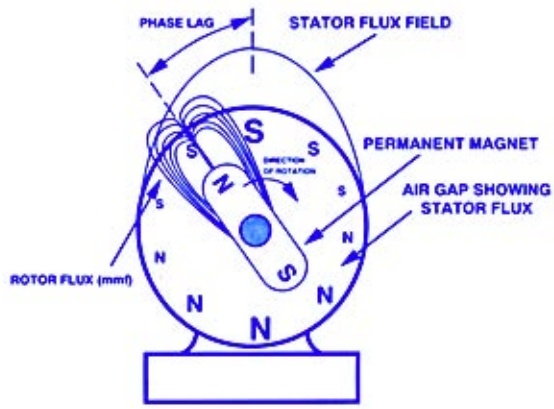


Figure 1. Relationship between rotor- and stator flux in the dc permanent-magnet synchronous motor.

AC induction motors: As in the PMSM, a rotating magnetic field is produced by stator windings. But the rotating stator field must also generate rotor flux, induced in the rotor by transformer action. Induction motors are not synchronous. To generate rotor current and provide torque, the rotor must spin more slowly than the stator field. This difference in rotational velocity is called slip—expressed as a frequency (typically of the order of 3 Hz). As slip frequency increases, so does phase lag of the rotor flux. Phase lag, caused by the rotor-time-constant, determines the rotor power factor and is closely related to the overall efficiency of the motor.

The rotor of an ac induction motor consists of two conductive rings with bars evenly spaced between them—often called a "squirrel cage", because of its resemblance to a rodent's treadwheel. Current in the rotor conductors can be modeled as a loop, which generates a flux field at 90° to the axis of current flow. Figure 2 shows the relationship between the stator field, rotor current and rotor flux.

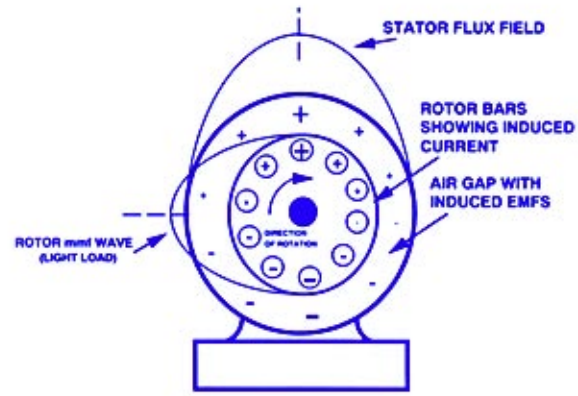


Figure 2. Relationship between rotor- and stator flux in an ac induction motor.

Although rotor flux rotates at the same speed as the stator field, the rotor doesn't, which points to the main difficulty of field control. Rotor flux is not fixed to rotor position. Seen in the rotor reference frame the transformer relationship becomes clear. If the stator field (primary winding) and rotor (secondary winding) rotate at the same speed, the frequency across the air gap is 0 Hz, no flux lines are cut, and no power is transferred to the rotor. When the rotor spins more slowly, the rotor bars see a sine wave across the air gap at the slip frequency, current is induced and power is transferred to the rotor.

Under load: With light loads, slip is almost negligible. As load is increased slip increases, generating increased rotor current and therefore greater flux and torque. The rotor-current/slip-frequency relationship is roughly linear for slip less than 10%. At higher loads, rotor time-constant and saturation characteristics increase in significance, and eventually the rotor can generate no more flux, regardless of slip frequency—and the motor will stall.

Field-oriented control: For ac-induction motors to provide dynamic performance comparable to a conventional dc motor, the vector (amplitude and angle) of rotor flux with respect to stator flux must be controlled. This requires decoupling the direct and quadrature currents from the magnitude of stator current (Clarke transform), and rotating them into the rotor coordinate frame (Park transform). There, the in-phase and torque currents can be compared with set points calculated for a specific motor and control scheme. The required current/voltage reference is calculated and transformed back to the stator frame of reference.

The AD2S100: In normal operation, the AD2S100, a mixed-signal processor, transforms three-phase 120° or two-phase 90° sine and cosine stator currents into representations of the direct (stator field) and quadrature (rotor) components. The Park transform rotates these signals into a reference frame determined by a rotor-position signal, from an absolute encoder or resolver-to-digital converter, appearing at the digital input port. Once the control response is calculated, an AD2S100 can perform the reverse transform back to the stator reference frame.

The AD2S100 is packaged in a 44-pin PLCC specified for operation over the extended industrial –40 to +85°C temperature range. Pricing begins at $15.39 (1,000s).

The AD2S100 was designed by Terry Searle at Newbury, England.

*Use the reply card for technical data. Circle 3

Asynchronous Sample-rate Converters

AD1890/AD1891 SamplePorts™ solve interfacing and compatibility problems in digital audio equipment

by Bob Adams

The CD player, an ideal storage medium for high-quality audio, has caused a once-revolutionary idea to be realized: that digital techniques are increasingly useful in the world of audio signals. Meanwhile, a less-well-known digital revolution is taking place: *all-digital interconnection between components*. The day is fast approaching when the rat's-nest of wires behind your preamp or receiver will be replaced by a few noise-immune fiberoptic cables carrying bits. The signal stays digital until the very end, when at last it encounters a D/A converter—either in the power amplifier or, indeed, the speaker itself. Manufacturers of audio equipment are already offering digital preamps, power amps, and speakers; and at least half of all CD players sold have digital outputs.

Problems do exist at present with the all-digital approach. For example, consider "interconnectivity", the convenience of easily connecting pieces of equipment together. When all cables carried analog signals, interconnect was a simple issue; you plugged the cable in, sound came out of the speaker. Sometimes the levels were wrong or the signal had hum on it, but at least recognizable audio came through. And if one wanted to mix two signals, any reasonably competent hobbyist could twist together two 10-kΩ resistors with a few cable leads and solder the connections.

But things are not quite so simple in the brave new digital world. The thorny issue of digital sample-rate synchronization can turn the simple task of mixing together two signals from different sources into a complex system solution with multiple DSPs programmed by a hard-to-find DSP expert.

The digital mixing problem: marching to the beat of the same drummer: Consider Figure 1. In this example, an all-digital mixer is receiving inputs from a variety or sources. These sources might also include external A/D boxes connected to microphone preamps, the digital outputs of outboard signal processing devices—such as digital reverbs or dynamics processing units, and possibly an external source coming from a remote site over a satellite feed or high-speed network connection. In an ideal world, all of these sources would generate their digital outputs at precisely the same sampling rates; on every tick of the clock, the input samples combine, each correctly weighted, to generate the desired mixed output signal. But what if one source produces samples slightly faster than the digital mixer's internal clock? The mixer may then occasionally miss a sample on that input. On the other hand, if the input is slightly slow, the mixer will occasionally repeat a sample. How often this happens depends on the sample-rate difference; a 0.1% sample-rate error would cause a data error at 22 ms, while a 10% error would cause a data error to occur every 220 μs.

Ideally, all equipment in a studio environment is fed from a common master-clock generator. But this ideal world is rarely achieved in practice; signals from outside sources that can't be synchronized to the internal reference standard pose a problem.

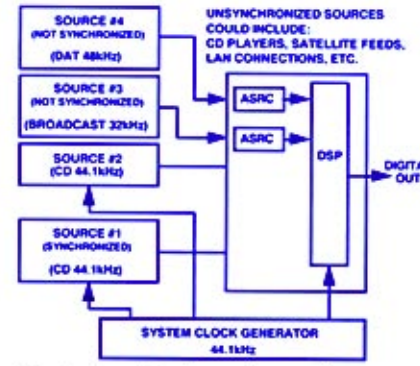


Figure 1. Typical application of sample-rate converter.

Synchronization problems are not limited to audio signals. They may occur in *any* situation where sampled data in digital form must be processed with other signals that cannot be synchronized to a common master clock. Examples include remote ADCs used in geophysical exploration systems, medical telemetry signals, satellite uplinks/downlinks, etc. One growing area where these situations may occur is when sampled-data signals are sent across a synchronous network. In this case, the network clock is the "master" clock; all signal sources must be capable of locking to it.

SRCs to the Rescue: A piece of equipment known as a "sample-rate converter" (SRC) can solve these problems. There are two types, synchronous and asynchronous (Figure 2). In *synchronous* converters (left), the input sample-rate is converted to a new rate at the output. The ratio between input and output sample-rates, specified by the user, is usually restricted to simple integer ratios like 3/2. This type of converter is of little practical use for solving real-world sample-rate conversion problems. For example, consider a 32-kHz input to a digital mixer running at 48 kHz. A synchronous sample-rate converter could convert by a ratio of 3/2 to give an output rate of 48 kHz. So far, so good. But what if the 32 kHz is actually 32.001 kHz, i.e., 32 kHz plus 1 Hz? This will always happen in practice; the resonant frequencies of even the best crystal oscillators are off by 10 ppm or so, and they usually drift over time and temperature. Then the output will not be 48 kHz, but 48.0015 kHz. The mixing console, running at 48 kHz, has no choice but to drop a sample every 1/1.5 = 0.66 of a second, resulting in audible errors.

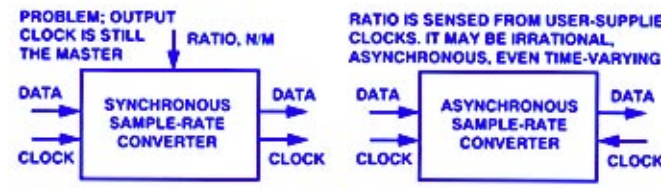


Figure 2. Synchronous and asynchronous sample-rate conversion.

This problem is readily solved (Figure 2 right) by the *asynchronous* sample-rate converter (ASRC). An analog scheme for such a device is shown in Figure 3. The digital input is converted to analog at the input sampling rate and smoothed, then converted back to digital at the rate required by the output clock. The clock for the output signal of the ASRC is an *input* to the sample-rate converter and can therefore be derived from the internal system clock of the digital mixer. With this device, slaved to both clocks, there is no longer a need for the user to tell the converter what the sample-rate ratio is. An ASRC automatically senses the required ratio from the clocks for the input *and output* signals.

Figure 3. Analog method of sample-rate conversion.

Its input and output clocks are not required to be related by some simple integer ratio. Even clock frequencies that are changing with time (as might be encountered in a vari-speed application) should ideally cause no audible errors.

An ideal all-digital ASRC should perform like an analog sample-rate converter, but without analog-type signal degradation. Until now, ASRCs in digital form have been available only as outboard signal-processing boxes, often costing from $4 000 to >$10 000. This high cost combines *hardware* cost (at least two full DSP chips are required for any decent implementation) and a highly complex algorithm, which requires a serious programming effort by a knowledgeable DSP expert.

For digital signals to interconnect as simply as analog, the sample-rate conversion must be reduced to a low-cost single-chip "jelly-bean" function—small, low-power, inexpensive, and with specs that remove any lingering doubts about sound quality. To meet this need, we have developed a single-chip all-digital solution: the Analog Devices AD1890 and AD1891* contain a complete high-quality ASRC. The AD1890 has specs that meet the demanding requirements of 18-to-20-bit professional audio; the AD1891 functions similarly at lower cost in 16-bit situations where large dynamic sample-rate changes are not encountered.

These ICs will be at the heart of future box-level solutions; and the longer-term implications are even more interesting. A mixing console is feasible where every input contains an ASRC. Such a console "looks" exactly like an analog console; any digital input signal could be plugged into any input, and the mixer's internal sample rate would be decoupled from the external sample rates.

Sample-rate conversion theory in a nutshell: The AD1890 is a very complex dedicated DSP chip with architecture specifically tailored for the task of sample-rate conversion. A comprehensive treatment of sample-rate conversion theory is well beyond the scope of this article, but a brief overview may give the reader an intuitive feel for what goes on inside the chip.

The simplest conceptual ASRC uses D/A and A/D converters, as shown in Figure 3. The digital signal is converted back to analog, filtered with a 20-kHz brick-wall analog filter (hopefully linear phase), then converted back to digital using an A/D converter. While this system would work, it's highly desirable to model it digitally to avoid the conversions and their associated errors.

The role of the filter in this diagram is complicated, because the input sample rates can be greater or less than the output sample rate. If the output sample rate is greater, the brick-wall filter serves to remove the DAC's output images, hence the cutoff frequency of this filter can be fixed at <1/2 of the input rate. But if the output sample rate is less than the input sample rate, the filter's cutoff frequency must be reduced to prevent frequencies >1/2 of the output sampling rate from appearing at the A/D input. The function of the filter changes from being an *anti-image* filter for the DAC (in the up-sampling case) to an *anti-alias* filter for the ADC (in the down-sampling case). For example, when converting from 48 kHz down to 32 kHz, frequencies higher than 16 kHz must not appear at the A/D input; therefore the brick-wall filter must remove components above 16 kHz. A major challenge of the AD1890 design was to mimic this effect digitally, with a smooth analog-like adjustment of the filter cutoff frequency during dynamic sample-rate changes.

We can consider the brick-wall analog filter of the Figure 3 to be an infinite interpolator: it produces an output voltage continuously at every instant of time. This leads to an interesting question; in the digital world, what interpolation ratio† do we need before the difference between the analog filter output of Figure 3 and the output of a digital interpolation filter become negligible?

This question may be answered by analyzing the "worst-case" signal—one with the highest slew rate. For audio, it is a full-scale 20-kHz sine-wave. A simple analysis shows that an interpolation ratio of 65,536 is required to reduce the difference between analog and digital interpolation to less than 1 LSB at the 16-bit level. This interpolation ratio, used in the AD1890, gives a worst-case distortion of about −96 dB. Signals at lower frequencies, with lesser slew rates, have less distortion.

Conceptually, all we need to do is to digitally interpolate by 65,536, and then resample this interpolated waveform by picking off the nearest computed point when an output sample clock occurs. Easy, right? All you need to do is look in your chip catalogues for an "interpolate-by-65,536" chip. Not so easy! A quick calculation of the input sample rate (say, 48 kHz) times the interpolation ratio gives an interpolated sampling rate >3 GHz!

Fortunately there are shortcuts. First, note that only 1 out of 65,536 interpolated samples are actually being used; the rest are simply discarded. If we know the exact arrival time of the output sample clock, this information can be used to compute only the requested output. Secondly, although the interpolation filter is extremely long (4 million taps), due to the high oversampling ratio, most of the data in the FIR filter are zeros, due to the zero-stuffing operation inherent in digital interpolation. These two simplifications permit interpolation and resampling to be done by a chip with realistic clock rates (16 MHz for the AD1890).

The final challenge is setting the cutoff frequency of the digital interpolation filter to be compatible with both up-converting and down-converting: as the output sample rate falls below the input sample rate, the interpolation filter's cutoff frequency must be reduced to prevent aliasing when the interpolated signal is re-sampled at a lower rate. This problem is solved in the AD1890 by dynamically stretching the interpolation filter's time-domain response as the output rate falls below the input rate; this reduces the frequency response of the filter in the frequency domain. It happens automatically; no user programming is required. For example, if the input and output rates are both 44.1 kHz, the frequency response of the chip is flat to 20 kHz. If the output rate drops to 32 kHz, the edge of the filter passband is scaled down by 32/44.1, resulting in a passband of 14.5 kHz.

Jitter rejection: In order to determine accurately the time at which to compute an output sample, based on user-supplied clock signals, the AD1890 employs a servo-control loop that is in many respects just like a phase-locked loop (PLL). This servo loop responds very slowly to changes in input or output sample rates; thus it averages the difference between the instantaneous arrival times of input and

*Use the reply card for technical data. Circle 4

†i.e., ratio of a theoretical internal sampler to the input clock

output clocks over many thousands of cycles, producing the equivalent of an "internal clock" that has sufficient accuracy to reliably pick the correct interpolated sample, even though each individual clock edge coming from outside the chip is measured with relatively low accuracy using the 16-MHz master clock.

This servo loop has several interesting implications. First, the jitter on the input or output clocks will be attenuated by the servo loop, which has a natural frequency of about 3 Hz. Jitter frequencies above 3 Hz are attenuated by 6 dB per octave. This is sufficient to remove even large amounts of clock jitter.

Another implication of this servo control loop is that step changes in the input or output sampling rate cause the internal clocks to slowly change to the new rate. While they are changing, the internal and external sample rates may differ. For this reason, the AD1890 uses buffer memory to temporarily absorb this rate difference without causing data error. The buffer is large enough to track real-time variations in sample rates (*vari-speed* operation, for example) with no audible errors.

The jitter-rejection capability of this chip is quite useful for manufacturers of stand-alone audio D/A converters that must recover a clock signal from the incoming serial data stream. The DAC's performance is often limited by jitter on the recovered clock signal. With the AD1890, the DAC can operate on a crystal-controlled clock feeding the output side of the AD1890, while the input side is driven by the PLL clock-recovery circuit.

Using the AD1890: for all its sophistication, the AD1890 is easy to hook up. Figure 4 shows the important signals. There are two serial ports, one each for the input and output. Each serial interface is quite simple and consists of an L/R clock, bit clock, word clock (optional), and data. Because this is an asynchronous SRC, the serial control signals are inputs to the chip (not outputs).

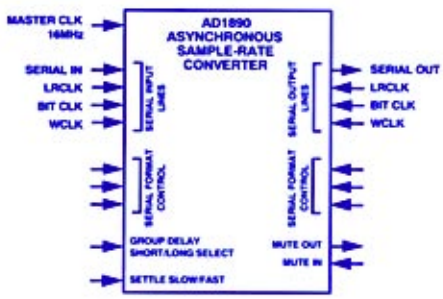


Figure 4. Control signals for the AD1890 VLSI SRC chip.

The input and output L/R clocks are generally square waves at the input and output sample frequencies; it is these clocks that are measured by the internal circuitry to determine the sample-rate ratio. The bit clock and word clock are only used as timing signals to get the data in and out of the serial ports.

Various serial circuit options are available to meet the most common interface standards, including the popular "I-squared S" standard. Common AES/EBU receivers and transmitters can typically be interfaced to these devices with no glue logic at all. In fact, a complete sample-rate converter with AES/EBU input and output can be made with only 3 chips: an AES/EBU receiver, the AD1890 ASRC, and an AES/EBU transmitter. A single master clock with a frequency between 16 MHz and 20 MHz is required for operation. This clock frequency need not have any relationship to the input or output clocks' rates.

Measurement results for the AD1890: An Audio Precision System One was used to make measurements of the AD1890's performance entirely in the digital domain, assuming an input sample rate of 48 kHz and an output sample rate of 44.1 kHz. Results at other frequencies are similar (with an asynchronous sample-rate converter, there are no anomalous sets of sample frequencies with markedly worse—or better—performance).

Conversion range: 2:1 up or down, with 60-kHz max output rate
Dynamic Range: 120 dB
THD+N, 1-kHz full-scale input: 107 dB
THD+N, 20-kHz full-scale input: 96 dB
Frequency response: 0-20 kHz ± 0.005 dB (output F_S = 44.1 kHz)
Settling time: 200 ms, fast mode[1]; 800 ms, slow mode
(to a 2:1 step change in input or output sample frequency)
Group delay: 700 µs (short group-delay mode), 3 ms (long group-delay mode)[1]

[1]**Note:** Long group delay mode and fast settling time mode are included for tracking very fast dynamic sample-rate changes without data errors.

Figure 5 shows the chip's distortion vs. level for both 1-kHz and 20-kHz input signals. As signal levels are reduced, the distortion relative to full-scale drops, limited by 20-bit quantization noise.

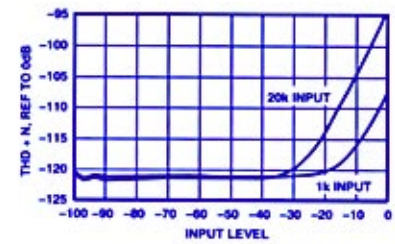


Figure 5. THD+N vs. level for 1-kHz and 20-kHz inputs.

Figure 6 shows an FFT of a full-scale 1-kHz input, with an input sample rate of 48 kHz and an output sample rate of 44.1 kHz. Note that all distortion components are less than −115 dB.

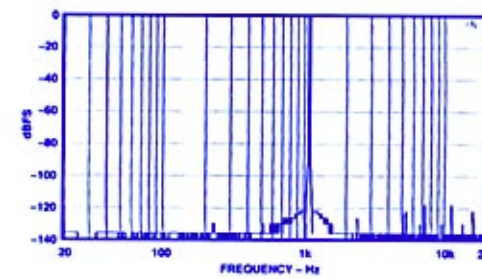


Figure 6. Output spectrum of 1-kHz input signal with sample-rate conversion from 48 kHz to 44.1 kHz.

To summarize, these chips solve what used to be a formidable problem: combining and processing digital signals whose sample rates are not synchronized. Equipment incorporating this IC at every input will look and feel more like an analog system than a digital one; any digital cable can be plugged in to any input, regardless of its sample-rate. In addition, the chips' jitter-rejection properties solve the problem of recovering a clean clock from a jittery serial interface; this may significantly improve the sound quality of many D/A converters.

The AD1890 and AD1891 are available in 28-pin plastic DIPs and PLCCs for the 0-to-70°C temperature range. Prices in 1000s start at $34 and $21, respectively.

Microprocessor Supervisory ICs Spec'd for −40/+85°C and MIL-Temp Ranges

ADM690-699 monitor the μP's supply, perform Reset and Backup tasks when it drops. And they do it *FAST*

Microprocessor supervisory circuits are the unsung heroes of digital equipment and systems. They detect when the power supply voltage is dropping during a power failure or brownout and take action to write-protect memory and switch to battery backup—or at least send a Reset signal to the processor. Some contain *watchdog timers*—circuits that monitor a vital microprocessor signal and provide Reset and warning signals if it fails to occur within an established time interval. Supervisory circuits are used widely in digital equipment, including computers, controllers, instrumentation, and automotive systems.

Designers have been designing kludges to perform these tasks as part of their systems for many years. More recently, chips have become available on the market to provide various combinations of functions. Now Analog Devices makes available an improved series of low-cost chips that are *pin-compatible with the earlier chips*, but consume up to 80% less power (5 mW), deliver up to twice the output current for battery backup (100 mA)—and have significantly shorter chip-enable propagation delay (5 ns) and faster V_{CC}-to-Reset response (120 ns). In addition, these chips are guaranteed to assert Reset with V_{CC} as low as 1 volt—*over the extended industrial and military temperature ranges**.

Members of the ADM69x family differ primarily in their level of functionality. Figure 1 shows the simplest chips. The **ADM698** monitors the 5-V V_{CC} and provides a $\overline{\text{RESET}}$ pulse during power up, power down, and low-voltage (<4.65-V) "brownout" conditions. The **ADM699** performs the same function and also includes a watchdog-timer input. The $\overline{\text{RESET}}$ output is forced low if the watchdog input is not toggled within the 1-second timeout period.

Both devices are available in 8-pin plastic DIP and 16-lead SO packages; the SO includes a non-inverted RESET output and a

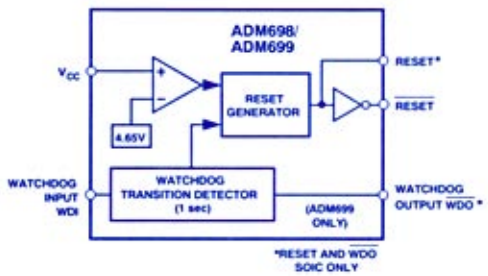
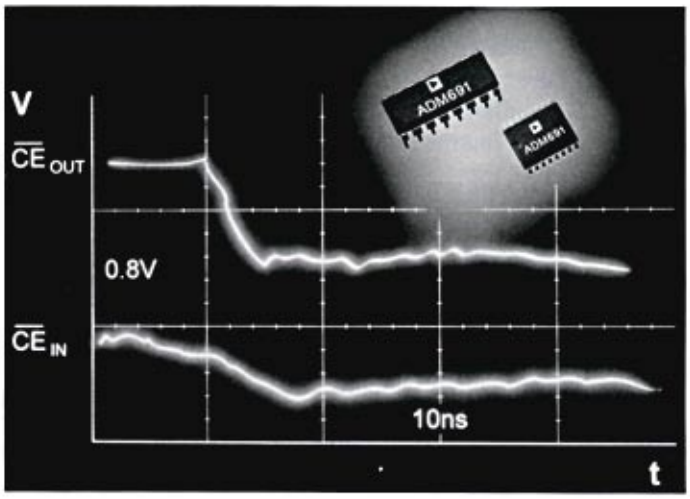


Figure 1. ADM698/699 block diagram.

*For technical data on these parts, use the reply card. Circle 5



(AD699) watchdog warning output, $\overline{\text{WDO}}$. Prices (1000s) start at $1.35/ $1.60 for the ADM698/699.

The **ADM690/692/694**, available in 8-pin DIP packages, provide RESET and watchdog functions, *plus* battery backup switching for CMOS RAM, CMOS microprocessor, and other low-power logic—and a 1.3-V threshold detector for power-fail warning, low-battery detection, or to monitor a power supply other than +5 V. They differ from one another in V_{CC} operating range, V_{BATT} operating range, Reset voltage threshold, and Reset timeout delay. Prices (1000s) start at $2.30/$2.30/$2.40.

The **ADM691/693/695** (Figure 2), housed in 16-pin DIPs and SO packages, offer similar functions to their even-numbered associates *plus* three additional functions: *write* protection of CMOS RAM or EEPROM (to prevent the microprocessor from writing erroneous data into RAM during power-up, power-down, brownouts, and momentary power interruptions); adjustable Reset and watchdog-timeout periods; and separate status outputs for watchdog timeout, backup-battery switchover, and low V_{CC}. Prices (1000s) start at $2.60 for all three types.

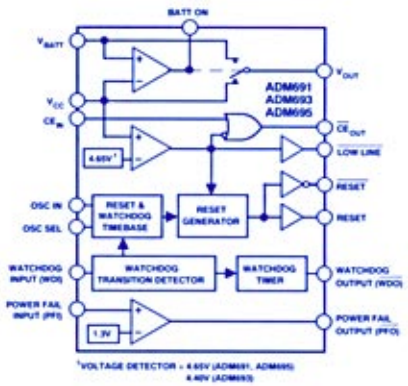


Figure 2. ADM691/693/695 block diagram.

The ADM696 and ADM697, housed in 16-pin DIPs and SO packages, offer most of the functions mentioned above; however, the **ADM696** provides battery backup switching for CMOS RAM, CMOS μP- and other low-power logic, while the ADM697 instead provides write protection for CMOS RAM or EEPROM. Prices for both (1000s) start at $2.60.

The ADM69x series was designed by Steve Harston at Analog Devices' Limerick, Ireland facility.

Getting the Most from IC Voltage References

A brief guide for users

by Walt Jung

As resolution and accuracy requirements of modern systems rise to 12 bits and beyond, the selection, specification, and application of voltage references becomes a key factor in system design. This article, devoted to designing with IC references, starts with the basic features of a good reference, discusses reference performance parameters, and concludes with examples of IC reference applications in high-performance circuits.

REFERENCE BASICS

Figure 1 depicts an ideal 1-volt reference source. This source is ideal in the sense that the 1.000000-V output is independent of time, temperature, and other environmental factors. Furthermore, neither connection polarity nor loading affects the voltage it delivers to the load. In this ideal world, connection of load, R_L, with either polarity, produces a constant voltage at the load, equal in magnitude to the original source, V_R.

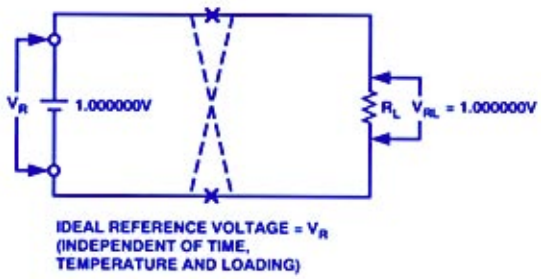


Figure 1. Ideal reference-voltage source.

In the real world, all the factors assumed ideal can and will vary. Major sources of error in reference voltage include initial calibration tolerance, output voltage drift with temperature and time, loading effects (characterized by output and wiring impedances), and noise components (both intrinsic and supply-related).

A variety of ways exist to produce a relatively stable voltage, including chemical, solar and low-temperature quantum devices. As a starting point, we will restrict our discussions to reference sources derived from system power, and in particular to reference circuits powered from positive or negative 3-30-volt dc supplies.

Most commonly, standard reference ICs are available in *three-terminal* form (V_{IN}, Common, V_{OUT}), with positive polarity. *Two-terminal* (diode-like) references, while more flexible regarding polarity, are restrictive as to loading. The constraints often complicate reference designs, making choices difficult (but inviting ingenuity).

Some basic two-terminal references are shown in Figure 2. In (a), a current-driven forward-biased diode (or diode-connected transistor) produces a voltage, V_F, approximately proportional to the logarithm of current and hence relatively insensitive to small changes in current. While its junction drop is somewhat independent of the raw voltage supply, it has numerous deficiencies as a reference. Among them are a significant temperature coefficient (TCV) of about −0.3%/°C, some sensitivity to loading, and a rather

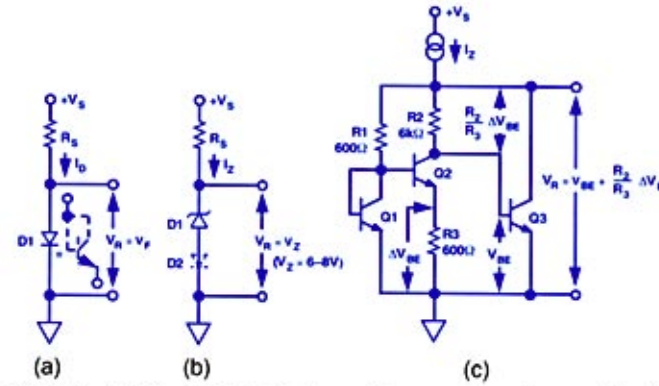


Figure 2. Basic semiconductor reference circuits. a. Simple forward-biased diode. b. Zener (avalanche) diode reference. c. Basic bandgap reference.

limited output voltage, about 600 mV; multiples of this voltage can be obtained by using series-connected junctions.

By contrast, this simple reference (as well as other shunt-type two-terminal regulators) has a basic advantage—that polarity can be readily inverted by reversing connections and drive current. However, a basic limitation of all shunt regulators is that driving current, I_D, does not decrease substantially when load current decreases.

In (b), by driving an appropriately selected reverse-breakdown diode at a current exceeding a threshold, an appreciably higher reference voltage can be realized. Although such reference diodes are almost universally referred to as "Zener" diodes, true Zener breakdown occurs below 5 V, while avalanche breakdown occurs at higher potentials.[1] With D1 chosen to have breakdown voltage in the 5-to-8-V range, its net positive TC adds to the negative TC of a series forward diode (D2), yielding a net TC of 100 ppm/°C or less with proper current bias.[2] In the past, carefully chosen diodes were combined to form single-package "zero-TC Zener references", such as the 1N821-1N829 series. Designs based on this concept were the basis for early hybrid IC references, which are in fact still sold today (more below).

While low TC can be realized in 2(b), the circuit has limitations on direct use of its output: First, the choice of voltage with high-accuracy diodes is limited, because the best TC combinations occur at specific voltages, such as the 1N829's 6.2 V. In addition, the range of load currents is limited, since the diode current must be carefully controlled for best TC. And, unlike a fundamentally low-voltage (<2-V) reference such as 2(a), Zener-diode-based references must of necessity be driven from voltage sources appreciably greater than 6 V, so this precludes their operation from 5-V system supplies. References based on old-style low-TC avalanche diodes tend to be noisy, an inherent property of the surface-breakdown mechanism. This noise is lower with monolithic buried-Zener types (more below).

The development of low-voltage (<5-V) reference circuits based on the bandgap* voltage of silicon led to the introduction of ICs that could provide good TC performance operating on low voltage supplies.[3] A bandgap reference develops an internal voltage proportional to absolute temperature (PTAT) to null out the temperature variation of a junction voltage, which has a negative TC (complementary to absolute temperature—CTAT). A basic

*The bandgap is the energy difference between the bottom of the conduction band and the top of the valence band. For references using silicon transistors the corresponding voltage, extrapolated to T = 0 K, is about 1.21 V—but is dependent on process and detailed curvature-compensation circuitry.

bandgap-based reference cell, driven by a constant current, is shown in Figure 2 (c). This circuit is also called a "ΔV_{BE}" reference, because of the correction voltage across R2. This voltage, based on the V_{BE} difference produced by differing current densities between matched transistors, Q1-Q2, is developed by a current resulting from ΔV_{BE} across R3 and transduced to voltage by R_2. It is summed with the V_{BE} of Q3 to produce V_R.

The bandgap technique is attractive in low-voltage IC designs because it is relatively simple and avoids noisy Zeners. It is used both for stand-alone IC references and as an internal reference within linear ICs. Buffered forms of 2-terminal 1.2-V reference ICs employing the bandgap concept provide additional current gain for stable, accurate operation over wide current ranges. Among them is the AD589, a synthesized 1.235-V "diode" with a 0.6-Ω dynamic impedance, a 50 μA to 5 mA operating current range, and TC grades ranging from 10 to 100 ppm/°C.

The basic designs shown in Figure 2 are sensitive to loading and require stable current drive. They generally need scaling of the output to more-useful levels, e.g., 2.5 V, 5 V, etc. For most applications, a buffer amplifier is used; besides driving loads, it provides voltage scaling to more useful levels.

An improved bandgap circuit (Figure 3), the "Brokaw cell", addresses these issues.[4, 5] This circuit is used in the AD580, the first precision bandgap-based IC reference. Still in production after 20 years, it is the first of a family of reference devices, such as the AD581 and AD584; the circuit also provides the internal reference in many Analog Devices ADCs and DACs.

At the heart of the AD580 are two transistors, Q2 and Q1, with equal collector currents and 8:1-scaled emitter areas (resulting in a 1:8 current-density ratio). The currents are maintained equal by matched load resistors and overall feedback voltage from the output amplifier (which also provides buffering), applied to the transistor bases. In this closed loop, the difference in the V_{BE}s (i.e., ΔV_{BE}) appears across R2, and a current equal to $2\Delta V_{BE}/R_2$ flows through R1, producing a PTAT voltage, V_1:

$$V_1 = 2\frac{R_1}{R_2}\Delta V_{BE}$$

V_1 appears in series with V_{BE}, thus a constant voltage, V_Z (about 1.205 V)—appropriately compensated for the variation of V_{BE} with temperature—appears between the bases and common.

The feedback attenuator, R4 and R5 (laser trimmed) permits the actual voltage appearing at V_{OUT} to be scaled higher, 2.5 V in the case of the AD580. In principle, this voltage can be raised to any practical level; for example, the selectable AD584 provides taps for 2.5, 5, 7.5, and 10-V operation.[6]

In practical applications, the amplifier is an invaluable feature. Besides its central role in optimizing the basic bandgap cell's performance, it also provides scaling and low output impedance. The AD580, operating from supplies of 4.5-30 V, outputs 2.5 V at up to 10 mA, a useful feature for a variety of circuits.[7] It is available in tolerances as low as 10 mV, with TCs as low as 10 ppm/°C (Table 1).

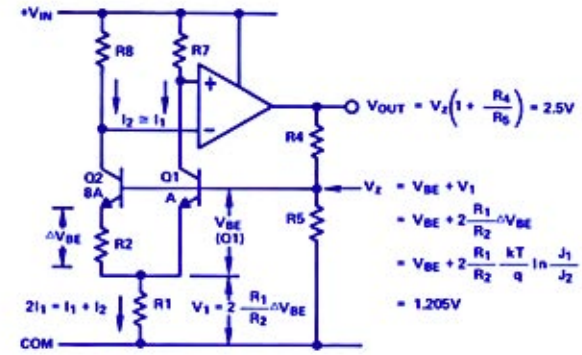


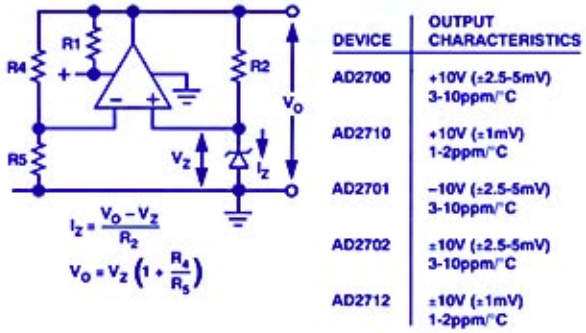
Figure 3. Functional diagram, AD580 precision bandgap reference

Table 1. Fixed Positive Output Three Terminal Monolithic IC References

Device	Type[1] (B, Z)	V_{OUT} (V)	Tolerance (+mV max)	Drift (ppm/°C, max)	$+V_S$ (V)	Load Sensitivity[2]	Line Sensitivity (μV/V, max)	Noise[12]	R_{TRIM} (Ω) ±Range (V)	I_Q (mA, typ)	PTAT Output (mV/°C)	Comment
AD780[8, 9, 11]	B	2.5	1–5	3–20	V_{OUT}+1.5 to 36	50	10	4 μV, 100	25k, 0.1	0.75	1.9	Precision 2.5 V
REF-43	B	2.5	15–50	10–25	4.5–40	50	5	220 (1 kHz)	10k, 0.095	0.45	1.9	Precision 2.5 V
AD680	B	2.5	5–10	20–30	4.5–36	100	40	250	NA	0.2	2.0	Low I_Q
REF-03	B	2.5	15	50	4.5–33	250	125	6 μV	10k, 0.15	1.0	2.1	Standard 2.5 V
AD580	B	2.5	10–75	10–85	4.5–30	1000	1–6 mV[7]	8 μV	NA	1.0	NA	3 Pin TO-52
AD1403	B	2.5	10–25	25–40	4.5–40	1000	3–4.5 mV[7]	8 μV	NA	1.2	NA	3 Pin Mini-DIP
AD586[11]	Z	5	2–20	2–25[4]	10.8–36	100–150	100	4 μV, 100	10k, +6%,–2%	2.0	NA	Precision 5 V
REF-195	B	5	2–10	5–10	5.1–15	20–40[13]	20–40[14]	50 μV	NA	30 μA[15]	NA	Note 10
REF-05	B	5	15–25	8.5–25[3]	8–33	500	500	10 μV	10k, 0.3	1.0	2.1	Note 5
REF-02	B	5	15–100	8.5–250	8–33	500–2500	500–2500	10 μV	10k, 0.3	1.0	2.1	Standard 5 V
AD587[11]	Z	10	5–10	5–20[4]	13.5–36	100	100	4 μV, 100	10k, +3%,–1%	2.0	NA	Precision 10 V
AD581[8]	B	10	5–30	5–30	13–30	500	200	40 μV	NA	0.75	NA	3 Pin TO-5
REF-10	B	10	30–50	8.5–25[3]	13–33	800–1000	1000	20 μV	10k, 0.3	1.0	NA	Note 6
REF-01	B	10	30–100	8.5–65	13–33	800–1000	1000–1500	20 μV	10k, 0.3	1.0	NA	Standard 10 V

NOTES
NA = not applicable for device in question.
[1]B = Bandgap, Z = Buried Zener.
[2]μV/mA, max, I_L = 0-10 mA, Sourcing.
[3]Long term stability 100 ppm (max.) per 1khours.
[4]Long term stability 15 ppm (typ.) per 1khours.
[5]Similar to REF-02 with long term drift specified.
[6]Similar to REF-01 with long term drift specified.
[7]Total over applicable supply range.
[8]Operates in two-terminal mode.
[9]2.5 V & 3 V output modes.
[10] Low I_Q, low dropout, shutdown pin.
[11]Optional noise reduction feature
[12]Typical, μV p-p, 0.1 to 10 Hz or nV/√Hz at 100 Hz.
[13]I_L = 0–30 mA, $+V_S$ = 6.3–15 V.
[14]$+V_S$ = 5.1–15 V.
[15]5 μA standby.

Zener-based references also benefit from careful buffering; and overall accuracy and stability are improved by including the Zener in the buffer circuit's feedback loop. Figure 4 depicts the basic circuit architecture of the hybrid IC AD27xx series. [8, 9] These devices have long provided stable +10-V, −10-V and ±10-V sources with very tight tolerances and TCs, as low as ±1 mV and 1-2 ppm/°C, performance only recently achieved by monolithic devices.



DEVICE	OUTPUT CHARACTERISTICS
AD2700	+10V (±2.5-5mV) 3-10ppm/°C
AD2710	+10V (±1mV) 1-2ppm/°C
AD2701	−10V (±2.5-5mV) 3-10ppm/°C
AD2702	±10V (±2.5-5mV) 3-10ppm/°C
AD2712	±10V (±1mV) 1-2ppm/°C

Figure 4. Precision Zener buffering architecture with gain provides regulated diode current for optimum TC.

Circuits of this type can feed back the optimum value of regulated current from the output $[(V_O - V_Z)/R_2]$ to operate a temperature-compensated diode at the op amp's + input. The Zener voltage is amplified using a pair of resistances whose ratio is laser-trimmed for accurate output voltage, $[(1 + R_4/R_5)V_Z]$. The op amp can drive load currents up to 10 mA with a typical output impedance of 50 μV/mA, and the inclusion of the diode in the feedback loop makes the device relatively insensitive to line-related errors, typically 125 μV/V for the AD2710. To further reduce the low calibration errors, a pair of fine-trim terminals is provided. The +10-V- output devices operate as shown, while the ±10-V AD2712 adds a precision inverter for the negative output.

IC REFERENCE SPECIFICATIONS

Monolithic IC references come in a variety of functional styles, dominated by three-terminal types with fixed positive output(s). The choice of bandgap or Zener technology determines the class of ultimate specifications and performance.

Figure 5 shows the standard basic pinout (input-2, output-6, ground-4) for + 2.5-, +5-, and +10-volt IC references in 8-pin cans and DIPs. Additional pins may be used for important housekeeping details, such as optional trimming (e.g., R_{TRIM} at pin 5) or providing a PTAT kelvin-scale thermometer output—an inherent bonus feature in bandgap devices ("V_{TEMP}" at pin 3). In general, all references should use an adjacent RF-quality input bypass capacitor, C_1, sometimes paralleled with larger C_2 for increased capacitance, to handle noisy sources and rapidly varying heavy loads. Some references may also allow (or require) an output bypass, C_{OUT} —or a noise-reduction capacitor connected to an internal point. Layouts should use a short, heavy (+) output conductor to minimize IR drops, while the (−) lead is less critical in this configuration, typically carrying ≤1 mA.

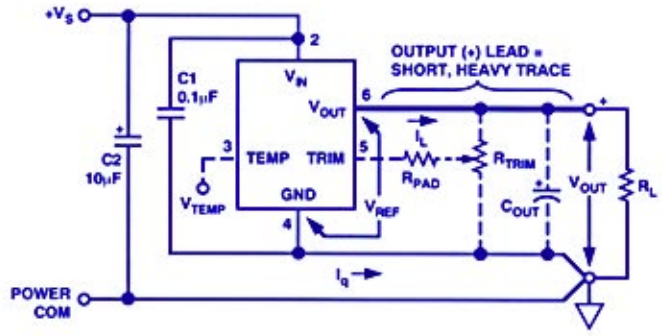


Figure 5. Standard positive-output three-terminal reference hookup (8 pin DIP pinout).

Table 1 is a summary of fixed-voltage three-terminal bandgap (B) and "buried"-Zener-based (Z) positive references. It compares the key device specs of output tolerance, drift, operating input supply range, sensitivity to load current (output impedance) and line voltage, noise, quiescent current, as well as trim range and PTAT thermometer availability. Comments and notes interpret and supplement the numerical specs. Table 2 compares references having selectable output voltage.

Table 2. Selectable Output Monolithic IC References

Device	Type[1] (B, Z)	V_{OUT} (V)	Tolerance (± mv max)	Drift (ppm/°C, max)	$+V_S$ (V)	Load Sensitivity (μV/mA, max, I_L=0–10 mA, Sourcing)	Sensitivity Line (μV/V, max)	Noise (typ, nV/√Hz or μV p-p 0.1-10 Hz)	Trim Range (±mV)	I_Q (mA, typ)	Tracking in Bipolar Mode (± mV, max)	Comment
AD584[8, 9]	B	2.5, 5, 7.5, 10	2.5–5, 7.5–30	5–30[5]	V_{OUT}+2.5 to 30 V	50[7]	Note 10	50 μV	Note 11	0.75	NA	Multiple positive output.
AD588[9]	Z	±5, +5/+10, −5/−10	1–5	1.5–6[3]	±13.5 to ±18	50	±200[6]	100	4	6	0.75	Precision programmable low noise + TC, Kelvin sensing buffer amplifiers.
AD688[9]	Z	±10	2–5	1.5–6[4]	±13.5 to ±18	40	±200[6]	140	5	9	1.5–3	Precision ±10 V, low noise + TC, Kelvin sensing buffer amplifiers.
REF08	Z	−10 −10.24	30–40, 40–60	50–100	−11.4 to −36	250	500	140	270	1.1	NA	Dual negative output.

NOTES
[1]B = Bandgap, Z = Buried Zener.
[2]NA = not applicable for device in question.
[3]Long term stability (ppm) 15 (typ), 25 (max) per 1khours.
[4]Long term stability (ppm) 15 (typ) per 1khours.
[5]Long term stability (pm) 25 (typ) per 1khours.
[6]T_{MIN} to t_{MAX}
[7]ppm/mA, 0-5 mA.
[8]Operates in two-terminal mode, 5 + 10 V.
[9]Optional noise reduction feature.
[10]0.002%/V, 15 to 30 V; 0.005%/V, V_{OUT} + 2.5 to 15 V
[11]Determined by user resistances.

All Analog Devices monolithic IC Zener references employ a subsurface breakdown technology, providing a salient improvement over the noise, drift, and reliability of surface-mode operated devices.[10] It was first applied in 1974, within the AD534 analog multiplier, [11] and later in DACs and other conversion products. The first stand-alone buried-Zener reference was the multiple-output AD588, a ±5-V, +10-V, −10-V precision unit, [12, 13] followed by the three-terminal +5-V AD586 and +10-V AD587, [14] and the negative-output REF08. Buried-Zener references offer the lowest drift, down to the 1-2-ppm/°C range (AD588 and AD586), and the lowest noise as a % of nominal output, 100 nV/√Hz or less at 5 or 10 V (AD586, -587, -588). The multiple-output AD588 and AD688 (±10 V) are listed in Table 2.

Tolerance: By choosing a unit specified for the required accuracy when possible, the user can avoid trimming (or gain scaling). This results in the best TC performance, since tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as 0.04% can be achieved with the AD586, AD780, and REF195, while the AD588 goes as low as 0.01%. If trimming must be used, be sure to use the specific circuit recommended on the device data sheet, with no more range than necessary. For scaling beyond the recommended range, use a precision op amp and accurate-ratio, low-TC tracking thin film resistors.

Drift: The lowest-drift (long-term and temperature-related) references are monolithic buried-Zener and hybrid types using temperature-compensated Zeners. Maximum TCs as low as 1 ppm/°C are available with the AD2710 hybrids, and 1.5 ppm/°C with the AD588 and AD688. Close behind is the AD586, at 2 ppm/°C; and the best bandgap is the AD780, at 3 ppm/°C. Lowest maximum long term drift is 25 ppm/1000 hr, in the AD588.

Temperature drift can affect full-scale accuracy in systems using A/D and D/A converters, as indicated by Table 3. This table shows system resolution in bits (column 1), required drift rate for 1/2-LSB drift over a 100°C change (column 2), and the voltages corresponding to 1/2 LSB for this 100°C example for three reference voltages. Drift of <1.2 ppm/°C is required to maintain 1/2 LSB error at 12 bits, but lesser temperature spans will require less-stringent drifts.

The temperature drift of references is seldom monotonic; there may be several reversals over the rated temperature span. Modern practice is to measure output at several temperatures, so as to guarantee a maximum error band applicable to the temperature range. The rated drift in ppm/°C is defined as the slope of a diagonal drawn between opposite corners of a box that bounds the applicable temperature range and the allowable maximum change. For example, the 5 ppm/°C, 5-volt AD586L (25 μV/°C) has an allowable change of 1.75 mV over a 70°C range (this technique is discussed in greater detail on the AD586 data sheet).

Table 3. Reference Temperature Drift Requirements for Various System Accuracies (1/2 LSB Criteria, 100°C Span)

Bits	Required Drift, (ppm/°C)	1/2 LSB Weight (mV), Various FS Ranges		
		10 V	5 V	2.5 V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Supply Range: Reference ICs generally require a supply range from about 3 V above rated output, to 30 V or more, except for devices designed for low dropout, such as the REF195 and the AD780. At low currents, the REF195 can maintain 5-V output with input voltage as low as 5.1 V (0.1-V *dropout*).

Load Sensitivity: Load sensitivity, or output impedance, is usually specified in μV/mA of load current (or mΩ), for output source currents of 0-10 mA. A reasonable value at low frequencies is 100 mΩ or less (AD780, REF43, REF195), but without due care, external wiring drops can add a comparable amount of series impedance, producing additional error (see Figure 5). Errors depending on load current are minimized with short, heavy conductors on the (+) output, and return wires to reference and power common from the low end of the load. For the highest precision, buffer amplifiers and separate force-sense (or Kelvin) connections—like those provided in the AD588 & AD688—can guarantee a precise voltage at the point-of-loading. Several of the applications illustrate Kelvin sensing.

Figure 6 is a plot of *dynamic* output impedance as a function of frequency for three 2.5-V references. These data were collected with a high resolution test setup using an Audio Precision System One, with software adapted from "IMPD"*, modified for 4-terminal high-resolution bandpass-mode operation. Input to the device under test is +15 V dc, and the test signal is 0.83-mA rms swept at 20-200-kHz, superimposed on a dc load of 2 mA.

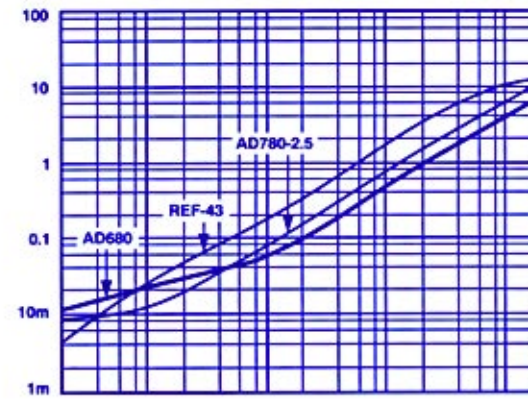


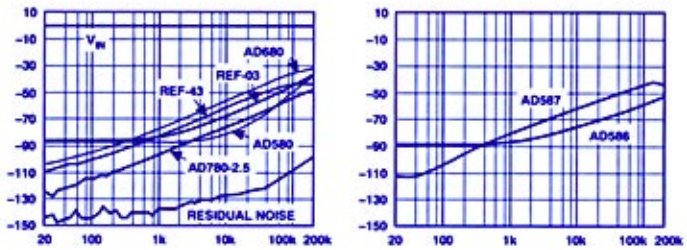
Figure 6. AD680, AD780, REF43; output impedance (ohms) vs. frequency (Hz); (V_{IN} (DC) = 15 V, I_L (DC) = 2 mA, I_L (AC) = 0.83 mA rms)

The plot compares their output impedance as a function of frequency. The characteristic 6-dB/octave rise above 100 Hz is essentially inductive (8-25 μH), while at low frequencies the impedance approaches or reaches a constant resistance in the vicinity of 10 mΩ for these devices. Some devices allow additional output load capacitance, which can be employed to further decrease output impedance at higher frequencies.

*Debi Brimacombe, "Generating Impedance vs. Frequency Plots With System One", AUDIO.TST, November 1992.

Line Sensitivity: Line sensitivity, the ratio of output change to a change of input, is less than 50 μV/V (−86 dB) in the REF43, REF195, AD680 and AD780. For dc and very low frequencies, such errors are easily masked by noise.

Plots of line rejection vs. frequency show susceptibility of a device to wideband noise on the input line (Figure 7). Data were collected with a high-resolution, screened and guarded test setup employing an Audio Precision System One analyzer operating in a bandpass-filtered crosstalk mode, for a dynamic range in excess of 130 dB. The device input is +15 V dc, and the output load is 1 mA. The test signal, superimposed on the input, is at 1 V rms, swept from 20 Hz to 200 kHz. For these plots, the V_{IN} 0-dB reference is 1 Vrms, and test-circuit residual noise below 1 kHz is ≅ −140 dB. Because of the bandpass nature of these measurements, in some instances they may not directly compare to results using wideband methods (which tend to become noise-limited at −90 to −100-dB levels).



(a) (b)

Figure 7. Various references, line rejection (dB) vs. frequency (Hz): (V_{IN} (DC) = 15 V, I_L (DC) = 2 mA, V_{IN} (AC) = 1 V rms). a. 2.5-V bandgap types. b. Buried Zener types.

Figure 7a shows line-rejection vs. frequency for a group of 2.5-V bandgaps. The recent AD680, AD780 and REF43 show rejection of 100 to 130 dB at low frequencies, decreasing to 40-55 dB at 100 kHz. The AD580 and REF03 have more-limited rejection (≅90 dB) below 1 kHz, but their behavior is comparable at the higher frequencies.

Line rejection for two 5- and 10-V buried-Zener devices (b) was measured in standard operation (no "noise reduction" used). The AD586 has greater rejection at high frequency; the AD587 at low frequency.

For references requiring greater line rejection, simple input filtering can be effective. A 100-Ω decoupling resistance with a 1-μF bypass filters frequencies above 1.6 kHz; the input DC headroom suffers only 0.2 V increase for 2-mA loading. This step is a wise precaution when references must derive their power from switch-mode power supplies. Additional output capacitance (where allowable) can also be helpful. Alternatively, line rejection can be increased with a preregulator, either a 78Lxx type regulator or stacked reference. [7]

Noise: Not all manufacturers specify the noise generated within a reference; when it is specified, there is little uniformity on how to measure it and present the data. For example, some devices are characterized for peak-to-peak noise in a 0.1-10-Hz bandwidth, others are specified in terms of rms for a specified bandwidth, and yet others in noise spectral density (nV/√Hz rms) at a given frequency. The most useful characterization would be a plot of noise spectral density over a range of frequencies, since it can be used for calculating any of the other specifications. Any noise fed through from the supply due to line sensitivity must be added (root-sum-of-squares) to the noise generated by the device.

Noise is an important characteristic in references because it limits accuracy and introduces uncertainty in high-resolution, wide-bandwidth systems. A noisy reference source used in a conversion system can result in reduced resolution. For low-frequency measurement systems, peak-to-peak specifications in the time domain are useful, because noise adds to the uncertainty of each unique data point. In higher-frequency systems, rms values for noise are more useful, because information usually has more redundancy, and signal-to-noise ratio, which compares their rms values, becomes a relevant criterion.

Gaussian noise is theoretically unbounded; for a given rms level, very large peak-to-peak values are possible, but their probability decreases very rapidly (for example, the probability of 14×rms peak-to-peak is only 2.6×10^{-12}). Conventionally, noise specs use a 6× ratio of p-p p/rms (0.27% probability of higher peaks).

For white noise (constant noise spectral density, e_n nV/√Hz), the rms value in a given bandwidth is the product of e_n and the square root of bandwidth, i.e., $e_n\sqrt{B}$, where B is a "brick-wall" noise bandwidth, $f_2 - f_1$. For converters, of resolution N bits, the target value of errors, 1/2 LSB, is $V_{REF}/2^{N+1}$. So, for 1/2-LSB rms white noise, the noise spectral density has to be

$$e_n \leq \frac{V_{REF}}{2^{N+1}\sqrt{B}}$$

and for 1/2-LSB peak-to-peak rms white noise, divide by 6:

$$e_n \leq \frac{V_{REF}}{6 \times 2^{N+1}\sqrt{B}}$$

For a 10-V, 12 bit, 100-kHz system with an unfiltered reference, the p-p noise requirement is modest, 640 nV/√Hz. Table 4 provides the set of required values for resolutions from 12 to 16 bits using 10-, 5-, and 2.5-V references. Note that the required e_n decreases with increased resolution, decreased V_{REF}, and increased bandwidth. However, the user can control the bandwidth with filtering, to make a noisy reference more useful.

Table 4. Reference Noise Requirements for Various System Accuracies (1/2 LSB/100 kHz Criteria)

Bits	Noise Density (n/V/√Hz), Various FS Ranges		
	10 V	5 V	2.5 V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

From Tables 1 and 2, bandgap and Zener references are available with noise densities from 100 nV/√Hz (usually specified at 100 Hz) and low-frequency noise from 4 μV p-p. Figure 8 illustrates the noise as a function of bandwidth and frequency for the AD780 (a) and the AD587 (b). These plots are taken with a swept bandpass filter with a gain of 100 and noise bandwidth, $B = f_2 - f_1 = 0.2316F$, in the vicinity of each frequency, F. Since the bandwidth is proportional to F and noise is proportional to $\sqrt{B}$,

the plotted noise will rise at about 3 dB per octave for white noise (constant e_n). At a given frequency, "F", e_n can be calculated by dividing the reading by $100\times\sqrt{(0.2316F)}$ (approximately $48\sqrt{F}$, about 1522 $\sqrt{\text{Hz}}$ at 1 kHz).

For example, the AD780 at 2.5 V (averaged plot through lower curve) reads about 160 μV at 1 kHz, whence the noise density is $160\times10^{-6}/1522 \cong 105$ nV/$\sqrt{\text{Hz}}$, as expected. The noise at 10 kHz is about $460\times10^{-6}/(48\sqrt{10000}) \cong 96$ nV/$\sqrt{\text{Hz}}$). Noise in the 3-V mode is proportionally higher. These curves reflect standard

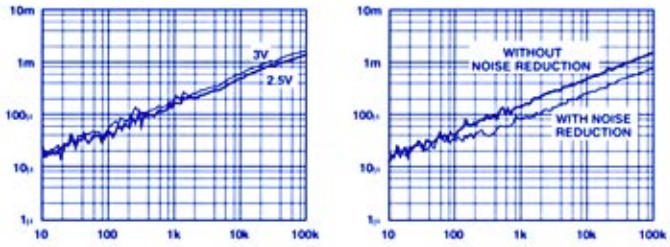


Figure 8. Various references, bandpass noise (V × 100) vs. bandpass frequency (Hz); (I_I (DC) = 2 mA). a. AD780, 2.5- and 3-V modes. b. AD587, with & without noise-reduction capacitor.

operation for the AD780; when the suggested noise-reduction capacitors are used, the noise at 1 kHz and 10 kHz is reduced to 53 and 32 nV/$\sqrt{\text{Hz}}$, respectively (not shown).

Data is plotted in Figure 8b for the AD587 in standard operation (upper), and with the recommended noise bypassing (lower). The noise is reduced by about 5 dB, from 200 Hz to 100 kHz; for example, at 1 kHz the reduction is from about 106 nV/$\sqrt{\text{Hz}}$ to 59 nV/$\sqrt{\text{Hz}}$. Noise bypassing works similarly for AD586, AD588 and AD688. The capacitor used should be a low leakage type (e.g., compact stacked film) placed close to the pin.

A useful alternative with any reference is a dc-accurate post-filter stage. This involves a low-impedance single- or multiple-pole low-pass filter, buffered by a precision low-noise op amp; it passes the reference voltage while removing high frequency noise (an example is shown in detail below).

Reference pulse response: Often of concern in reference applications is the transient change of output voltage in the presence of stepped loads. Fast load changes of up to full-scale current perturb the output voltage, often beyond the rated error band. Key questions: how quickly does the output transient recover to within the rated accuracy band after a load change? Can anything be done to reduce the effect?

For example, Figure 9 shows the response of a REF43 IC to a 10-mA load step, for conditions of no output decoupling (a) and with the recommended decoupling network (b) [10 μF tantalum in parallel with 0.01 to 0.1 μF ceramic from V_{IN} and V_{OUT} to ground]. Without decoupling, the output has a large spike, settling to within ±2.5 mV in 3-4 μs and producing a further disturbance in circuits served by the reference. When decoupled, the output remains within the error band, changing only slightly.

For references with similar dynamics to the REF43, output decoupling is useful in maintaining control. However, additional output capacitance may or may not be allowable towards buffering a given reference type against transient loads, so specific data-sheet recommendations should be followed.

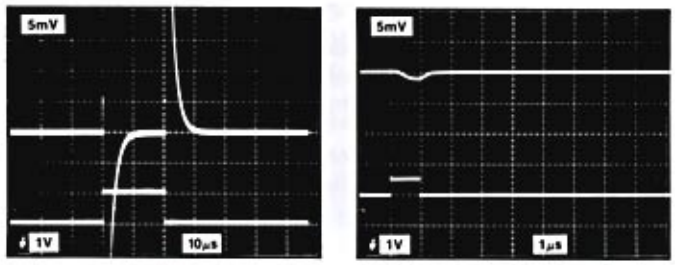


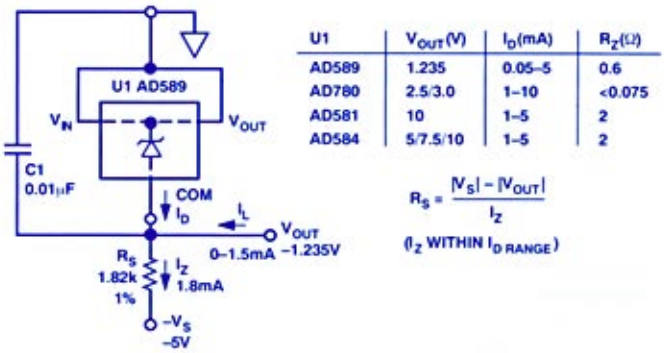
Figure 9. REF43 pulse response for 0-10-mA load change, with and without decoupling. a. Response with no decoupling. b. Response with output decoupling of 1 μF & 0.01 μF.

REFERENCE CIRCUIT APPLICATIONS

Shunt references: As noted earlier, shunt mode references can be used in either polarity, but they have the disadvantages of limited drive and relatively high output impedance; these tend to restrict them to applications with limited ranges of load variation.

Figure 10 illustrates a shunt-mode application, using two-terminal devices and three-terminal devices with V_{IN} and V_{OUT} jumpered for two-terminal operation. Here, an AD589 is used with a negative supply to provide a regulated negative reference. All shunt-operated references should be designed with careful attention to dc currents. R_S must be selected appropriately to maintain shunt current, I_D, in a limited range for any specified combination of load current, I_L, and supply voltage, V_S. With the AD589, R_S is chosen to allow 1.8 mA to flow with the magnitude of V_S 10% low. This will allow a 0 to 1.5-mA load current range, and the device will remain in a safe range with the load removed and $|V_S|$ 10% high. The AD589's typical R_Z of 0.6 Ω holds output changes <1 mV for a 1.5-mA I_L change.

A bypass capacitor is recommended to reduce high-frequency noise and ac impedance; the value shown in the figure can be increased for further impedance reduction. As the table shows, a wide range of voltages are available—with the same device in some cases (AD584, AD780); the AD780 provides the lowest output impedance.



U1	V_{OUT}(V)	I_D(mA)	R_Z(Ω)
AD589	1.235	0.05–5	0.6
AD780	2.5/3.0	1–10	<0.075
AD581	10	1–5	2
AD584	5/7.5/10	1–5	2

Figure 10. Shunt reference IC operation.

Negative references: Positive voltage references are the most widely produced and used, but negative references are often required. While this can be accomplished with a simple shunt reference, it is usually more desirable to operate negative references

as current-buffered voltage sources, to avoid the shunt circuit's loading restrictions.

A simple technique is to cascade a stable positive voltage reference with a precision inverting scaling amplifier, using a high quality op amp, such as an AD707 or OP177, and a high-accuracy resistor pair. This approach is workable and straightforward but its cost/performance is limited by the tradeoff between resistor accuracy and the cost of precision resistors—which can greatly exceed the cost of the op amp.

A more direct approach for a negative reference is to use an IC specifically designed for such use, namely the REF08 (Table 2). The buried-Zener REF08 is designed as a 10-V three-terminal negative reference; it functions as a mirror image of 10-V positive references, such as the AD587. It is applied in simple fashion, furnishing a −10-V output with tolerances of ±30 mV or ±40 mV; a ±270-mV trim range is available. With pin 4 strapped to ground, it furnishes an alternative −10.24 V ±40 or ±60 mV, suitable for easy scaling in 10-mV/LSB 10-bit applications. The REF08 is available with TCs of 50 or 100 ppm/°C.

Another alternative is to "invert" positive IC references, a design approach valuable because of the wider array of high-performance references from which to choose (Table 1); and the elimination of resistors and their scaling/drift errors. Resistorless inverters basically enclose the IC reference within a precision op amp feedback loop, driving the common (or negative) terminal so as to maintain the normally positive output at ground; thus the reference IC's common terminal is driven at $-V_{REF}$.[15]

An example of this scheme is illustrated in Figure 11, using an AD780 (or other positive three-terminal IC) for U1 as the reference IC. Overall, this circuit supplies a stable $V_{OUT} = -V_{REF}$, where V_{REF} is the 2.5-V (or other) voltage at U1's output (with no load). Thus the circuit inverts a positive reference's output, without the expense or errors of a precision resistor pair. The full dc precision of the basic reference IC is easily maintained, due to the buffering by the op amp, U2, while ac performance can be optionally improved even further.

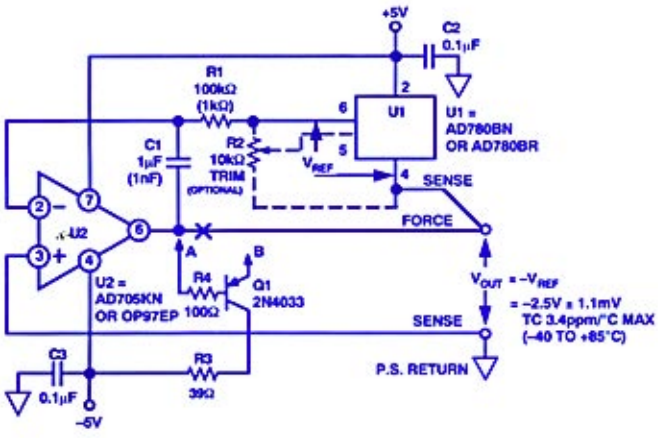


Figure 11. Buffered "inverted" negative reference.

DC accuracy is optimized largely by careful selection of the U1 device from Table 1, for initial tolerance, drift, etc. The drift characteristics of the op amp are usually less important, but may not be negligible. For example, a 1 µV/°C drift in U2 is equivalent to a negligible 0.4 ppm/°C drift in U1's 2.5 V. U2 should also have V_{OS} <100 µV, for negligible contribution to tolerance error. Given this drift/accuracy criterion, U2 should be a high DC precision type such an AD705KN or OP97EP when used with a low-drift IC such as the AD780 (or other). Current drain for the unloaded circuit is typically 1.2 mA.

U2 determines the output drive capability of the circuit. For lowest self-heating errors, dissipation in U2 should be minimized, with current outputs restricted to 10 mA or less (including the quiescent current of U1). Substantially higher currents of say 50 mA can be accommodated without side effects using a PNP booster transistor such as a 2N4033, inserted between points "A" and "B". Lower output impedance in wideband applications is available with the AD820 for U2, with some tradeoffs in dc accuracy and drift. Connecting the FORCE and SENSE leads as noted minimizes wiring-drop errors.

Filter R1-C1 sets the integrating time constant in U2 to promote stability and noise reduction. With the choice of larger values, the broadband noise of U1 is reduced to a minimum, and overall noise is close to the noise of U2; a typical measurement is <20 nV/√Hz at 1 kHz. If attenuation of reference noise is not necessary, the smaller values (in parentheses) should be used. Using the devices in the figure, the (untrimmed) output is −2.5 V ±1.1 mV, with a TC of 3.4 ppm/°C. U1 and U2 are available in both SOIC and DIP packages.

Shunt mode references, as essentially floating ICs, are used for positive or negative outputs. When used with a buffer op amp, in an inverted configuration, their load-current restrictions are removed. Figure 12 is an example of a buffered inverted shunt-mode negative reference. This circuit is similar to Figure 11, but includes input resistor, R1, to supply bias current for the reference diode. Because the op amp's (+) input is grounded, the feedback loop holds the positive terminal of D1 at virtual ground. As a result, the amplifier output is driven at the reference voltage, which, in the case of the AD589, is −1.235 V. The diode requires only a small bias current; the available load current is then limited only by the output specification of U1 (15 mA minimum).

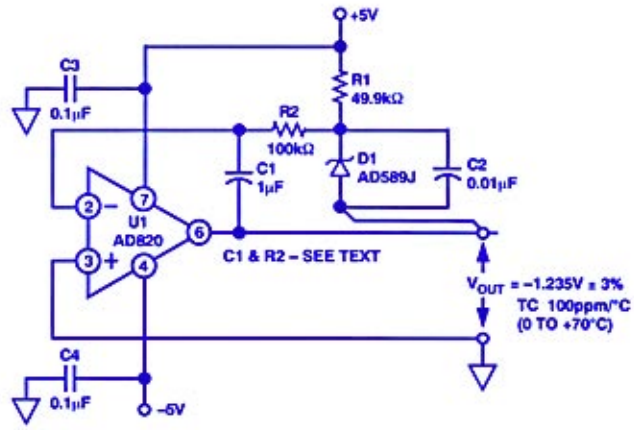


Figure 12. Buffered "inverted" low noise shunt reference.

This scheme can also be applied for the opposite output polarity (positive output), with D1 reversed and R1 returned to a negative voltage. For other supply voltages, R1 can be chosen for a standard value of D1 bias current, say 100 µA. Note that this principle applies for other voltages, using devices designed to operate in the shunt mode (see table of Figure 10). Kelvin sensing, used as shown, maintains high dc accuracy at the load.

As in the circuit of Figure 11, integrator time constant, R_2C_1, can be optionally chosen for noise filtering as shown; the noise is reduced to that of the op amp used. Using the AD820, the filtered noise measures ≅15 nV/√Hz at 1 kHz, and the circuit's output impedance is ≅0.05 Ω at 1 kHz. Without this filtering (much smaller time constant), noise output of the circuit is that of the AD589, or ≅200 nV/√Hz. In this simple circuit, the output accuracy is ±3%, that of D1. Trim is possible, using a resistive divider across D1, feeding R2, to adjust the output voltage.

Low-noise references for wide-dynamic-range converters: High-resolution converters, including Σ-Δ and (especially) high-speed types, benefit from the improved noise and load-capacitance tolerance of recently available references.

Figure 13 shows the AD780 used as a 3-V reference for the AD711x series of >20-bit Σ-Δ converters. The 3-V scaling (rather than 2.5) enhances the dynamic range of this and many other 5-V single-supply converters, while the ≅4-μV p-p noise (0.1-10 Hz) minimizes overall system noise.[16] In addition, the large decoupling capacitance at the converter's REF IN pin minimizes voltage errors due to transients. These same factors also enhance performance of wider bandwidth converters such as the 16 bit AD7884.[17]

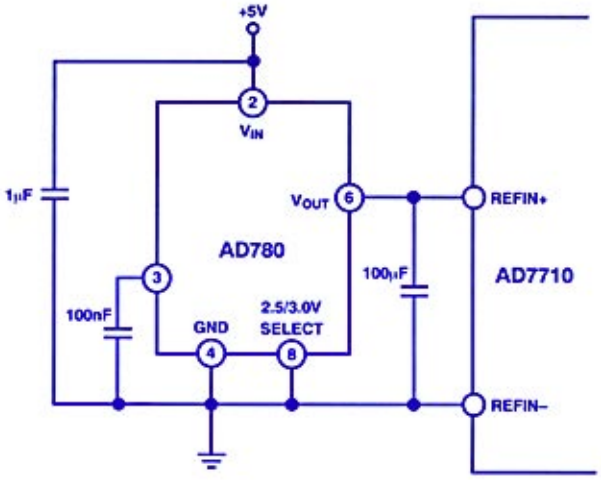


Figure 13. Precision 2.5/3-V reference for the AD7710-series high-resolution Σ-Δ ADCs.

Current-boosted 50-mA three-terminal reference: For highest dc accuracy, output current of reference ICs should be kept well within the 10-mA rating. Thus for loads of substantially more than about 5 mA, some form of booster should be considered. This can be accomplished with the addition of a PNP pass transistor, as shown in Figure 14.

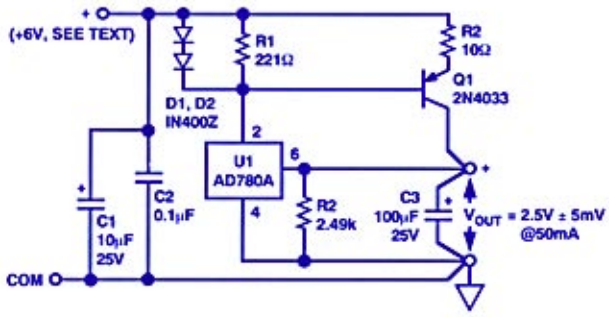


Figure 14. 50-mA current-boosted three-terminal reference with current limiting.

In this circuit the input current of U1 through R1 develops a base drive for Q1, whose collector provides the bulk of the load current. U1 never is called upon to furnish more than a few mA, so this minimizes internal temperature differential and drift. Short-circuit protection is provided by the diode clamps which limit drive to Q1, at about 80 mA of load current.

Other references and output voltages can be used for U1, but may require some R1 adjustment, dependent upon their I_q. The booster current-limiting configuration causes the dropout voltage of the circuit to increase, and operation from a +5-V supply may be marginal, especially when references having greater dropout voltage are used for U1.

Besides increasing output current, Q1 decreases output impedance; the loaded output impedance at 1 kHz is <10 mΩ, about 10-20 times better than for the AD780 alone. C_3 is high to minimize high-frequency output impedance (400 mΩ at 100 kHz), but smaller values can also be used. If an input voltage appreciably more than +6 V is used, heat sinking may be needed for Q1.

Bipolar-reference bridge driver: For optimum operation of a dc bridge, bipolar drive is useful; it virtually eliminates the output common mode component. Figure 15 shows an implementation using either an AD588 or AD688 buried-Zener reference with Kelvin sensing of the drive voltages at the bridge.

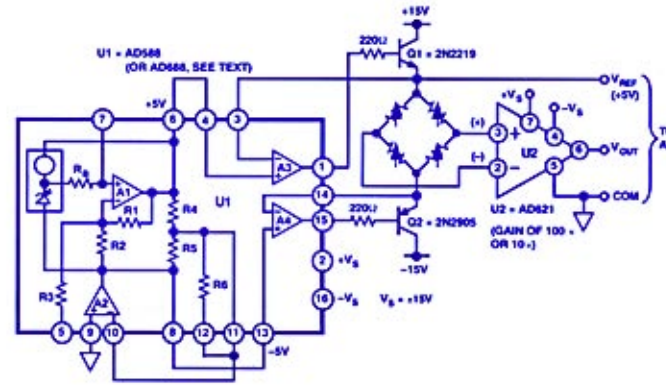


Figure 15. Bipolar (±5-V) bridge with precision in-amp.

The AD588 Zener cell and A1 produce a 10-V total potential, which can be shifted either above or below common, or split into ±5 V by R4 and R5, with ground enforced by A2, as shown here. The basic ±5-V signals then appear at pins 6 and 8; they drive Kelvin sensing follower-amplifiers A3 and A4. The amplifiers sense the voltage at each end of the bridge and drive those points through external current boost transistors Q1 and Q2, respectively, forcing the bridge end points to equal the ±5 V output of the reference, within the symmetry specifications of the AD588 (±1.5 mV). Metal-can transistors are used for Q1 & Q2, for best dissipation at the 30-mA drive level. For ±10-volt drive, the AD688 can also be used in a similar fashion.

The output sensing in-amp is the AD621, which provides tap-selectable gains of 10 and 100, with a gain tempco of 5 ppm/°C or less, lower in fact than can easily be done with readily available gain set resistors and a single ended amplifier. The scaled bridge output signal can drive an ADC; which can also use the +5-V bridge reference voltage as the conversion reference.

30-mA reference with shutdown: The REF195 bandgap reference is like the other references of Table 1; but it has a unique shutdown capability, which allows a precision 5-V output to be turned ON and OFF by a TTL/CMOS compatible digital input, as shown in Figure 16. It has a low dropout of 0.5 V at 10 mA and low current

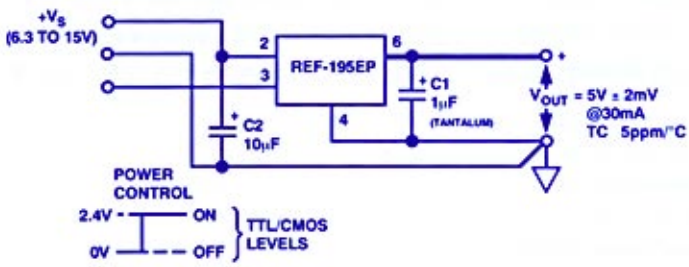


Figure 16. 30-mA reference with shutdown.

drain for both quiescent and shutdown states, 45 and 15 µA (max), respectively. For inputs in the range of 6.3 to 15 V, the REF195EP shown can furnish 5 V (±2 mV) for loads of up to 30 mA, with a 5-ppm/°C max TC.

The shutdown pin (3) is controlled by TTL or CMOS logic levels, with a "1" (or $+V_S$) commanding the output ON, while a low input shuts it OFF. With a 1-µF load bypass capacitor (the minimum recommended), transition OFF-ON time is several hundred µs. This OFF-ON transition time will be load dependent, increasing for higher C_L values. ON-OFF transition timing is determined by the load current and C_L.

To maximize DC accuracy in this circuit, the output of U1 should be connected directly to the load with short heavy traces, to minimize IR drops. The common pin is less critical, due to the much smaller current returning to the device.

Low noise 2.5/5/10-V reference: As noted earlier, voltage reference noise can contribute to system error. But the output of a reference can be buffered and filtered to effectively lower wideband noise by an order of magnitude or more.[18] For example, the low-noise reference circuit of Figure 17, using simple filtering, combines good ac and dc performance. It comprises a reference, U1, and a low-noise, buffered output circuit. Final output noise is largely determined by U2, and can range from under 2 nV/√Hz, to 20 nV/√Hz or more at 1 kHz, depending on the device.

The basic reference voltage is set by U1, a 2.5, 5 or 10-V IC chosen from Table 1 for required accuracy and drift. This circuit uses an AD586MN, a 5-V (±2 mV) buried-Zener reference with a 2 ppm/°C drift and low 1/f noise. U1's stable 5-V output is applied to a R1-C1/C2 noise filter, using electrolytic capacitors for a low corner frequency. DC leakage errors are minimized by bootstrapping C1 so as to see only the small R2 dc drop as bias, effectively lowering leakage to negligible levels. The filter corner frequency is about 1.7 Hz, providing about 35 dB of attenuation at 100 Hz. Attenuation is modest below 10 Hz, so reference choice is still important to noise performance at low frequencies.

The filter's low-noise, dc-accurate output is buffered by a unity-gain buffer using an OP113EP low-dc-error, low-noise op amp. With less than ±150 µV of V_{OS} error and less than 1 µV/°C drift, the buffer's dc performance will not compromise accuracy/drift of Table 1 references. The OP113 has a typical current limit of 40 mA, more current than IC references usually provide.

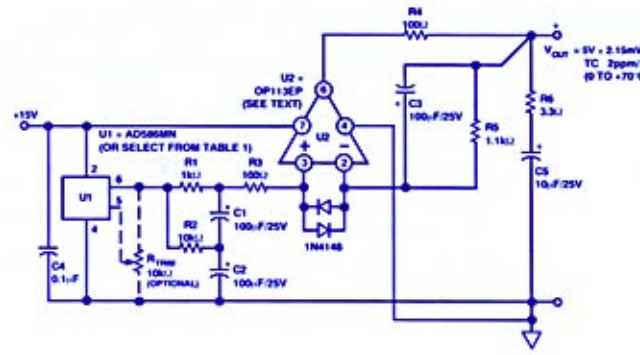


Figure 17: Low-noise 2.5/5/10-V reference.

While the single-supply OP113 is useful over the entire 2.5-10-V range, even lower-noise op amps are available for 5-10-V use. The AD797 has measured 1-kHz noise less than 2 nV/√Hz, compared to about 6 nV/√Hz for the OP113. Other 5-10-V range possibilities include the OP27 and OP176.

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Hardware & software data; GNU C compiler @ low cost

Analog Devices fixed- and floating-point processors, including the ADSP-216x and ADSP-217x, are supported by a complete suite of software and hardware tools, including the GNU-based Optimizing C compiler, for programming in an ANSI C environment (G21 for the ADSP-2100 family, G21K for the ADSP-21000 family). The C programming packages are available at new low prices.

The available software and hardware development tools for the fixed-point ADSP-21xx and floating-point ADSP-210xx families are described in a pair of new data sheets. Included are System Builder; Assemblers; Linkers; Library/Librarian; Simulators; PROM and HIP Splitters; C Compiler, CBUG source-level debugger, and C runtime library; EZ-ICE® Emulators; EZ-KIT starter packages; and much more. **Circle 16**

Quad Multiplier IC

MLT04: four 8-MHz analog multipliers on a chip

The MLT04, industry's first complete quad IC multiplier, provides 4 analog multipliers, plus 1.23-V reference, for voltage-control of gain, frequency, and filter parameters, power calculation, modulation, frequency doubling—and for specialized applications such as generating waveforms at low-cost for correcting distortion in hi-resolution CRT displays.

It operates on ±5-V supplies, with inputs and output normalized to ±2.5 V. Specs include 0.2% nonlinearity, 0.005% drift of total error over temperature, 8-MHz small-signal BW, 53-V/μs slew rate and 1-μs settling time, 0.02% THD+N on the Y channel (0.1% on the X channel). A SPICE model is included in the new 31/2" ADSpice disk. The MLT04, spec'd for −40 to +85°C, is available in 18-pin DIPs and SOICs. Prices start at $11.95 in 100s ($3/channel). **Circle 11**

Receive Port

AD7013: Baseband I & Q for TIA IS-54 digital cellular

The AD7013, operating on a +5-V supply, is a complete low-power CMOS TIA IS-54 baseband receive port. At its heart is a pair of Σ-Δ A/D converters, providing two channels of conversion for differential or single-ended in-phase (I) and quadrature (Q) signals, with choice of brick-wall (analog mode) or root-raised-cosine (digital mode) FIR filtering. An input multiplexer allows a choice between main and auxiliary signal sources.

In addition to the ADCs, it includes 3 D/A converters (2 @ 8-bit and 1 @ 10-bit) for performing such auxiliary functions as AGC and AFC, on-chip voltage reference and calibration logic, and 16-bit serial interfacing, plus power-down options (<30 μW in sleep mode). It is housed in a 28-pin SSOP and specified for −40 to +85°C. It is priced at $9.37 in 1000s. **Circle 12**

Clock-Recovery PLL

AD803 recovers clock, retimes 20-Mbps NRZ data

The AD803 is a clock-recovery and data-retiming phase-locked loop for 20.48-Mbps non-return-to-zero (NRZ) data, the newest member of a family recently described in these pages (vol. 27-1, pp. 3-6). Its principal employment is in fiber in the loop or passive optical network applications. Unlike other PLL-based clock recovery circuits, the AD803 does not require a preamble, an external VCXO, or an external crystal to lock onto input data. It acquires frequency and phase lock using two control loops.

Random jitter is 3° rms and pattern jitter is virtually eliminated. It operates on a single +5-volt supply, consuming only 185 mW typical, 275 max. With TTL-compatible inputs and outputs, it operates at temperatures from −40 to +85°C, and is available in a 20-pin SOIC. Its price is $25 in 1000s. **Circle 13**

What's New in A/D and D/A Conversion

Two Fast SADCs

AD775: 8 bits, 20 MSPS
AD871: 12 bits, 5 MSPS

The **AD775** is a high-performance, low-power 8-bit, 20-MHz sampling A/D converter, designed for digitizing video signals, high-speed stepped dc (CCD, IR and multiplexed data acquisition), and baseband signals. 1175-compatible, it requires but a single +5-V supply and dissipates only 60 mW. It is available in 24-lead SOIC and plastic DIP, for the 0 to +70°C range. Price is $6.95 in 1000s.

The **AD871** is a complete, low-noise, 12-bit, 5-MSPS monolithic sampling A/D converter with an internal 2.5-V reference, designed for high-resolution image digitizing and high-speed data acquisition at low cost. Guaranteeing no missing codes, it has low noise, <0.17 LSB rms, 68-dB S/N+D, and 73-dB spurious-free dynamic range (SFDR). Available for commercial and MIL-temp ranges, it is housed in a 28-pin ceramic DIP and 44-pin LCC. Price is $95 in 1000s. **Circle 17**

165-MHz Video DAC

ADV458: 3 channels, 8 bits
Includes 256 × 24 RAM

The ADV458 is a 165-MHz triple 8-bit single-supply (+5-V) CMOS RAM-DAC for high-resolution color graphics. It is pin- and functionally compatible with existing second-source products.

The ADV458 directly drives RGB monitors (RS-343A/RS-170) with 8-bit pseudocolor at screen resolutions up to 1,600 × 1,280 pixels. Its 256 × 24 lookup-table RAM allows for the display of up to 256 colors out of a total palette of 16.7 million addressable colors. It also includes triple 4 × 8 (i.e., 4 × 24) overlay registers.

Digital inputs are TTL-compatible, and pixel input ports are multiplexed 4:1 or 5:1. Available clock rates include 165, 135, 110, and 80 MHz. It is housed in an 84-pin PLCC and specified for 0 to 70°C operation. Typical Prices $18 (1000s), $14 (10,000s). **Circle 19**

18/16-bit Stereo A/Ds

2-channel audio AD1879/78:
SNR: 103 dB, THD+N: −98 dB

The AD1878 and AD1879 are complete 16- and 18-bit audio-band sigma-delta dual A/D converters with serial output. The **AD1879** is capable of a state-of-the-art signal-to-noise ratio of 103 dB, with total harmonic distortion + noise −98 dB, while the **AD1878**'s performance is limited only by its 16-bit output data format. The Σ Δ architecture simplifies antialiasing and offers excellent differential nonlinearity, with no missing codes.

Applications are primarily in professional digital audio—recording, effects machines, workstations, network switches/routers, compact disc (CD) recorders—but these converters are attractive for many other applications in the audio band. They are rated for operation from −25 to +70°C and packaged in a 28-pin DIP. Prices (100s) start at $42. **Circle 21**

Data-Acquisition ICs

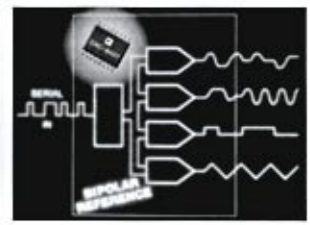
8-b AD8401: DAC+4-ch. A/D
12-b AD7890: 8-ch, 100 ksps

The **AD8401** is a complete single-supply (+5-V), 4-channel, 8-bit data-acquisition & control system. It contains an analog MUX, a sampling ADC with 2-μs conversion time, a DAC, and an internal voltage reference. An analog I/O port, it directly interfaces with high-speed 8-bit data buses. Its 28-lead SOIC package saves board space. Operation is from −40 to +85°C. Prices start at $7.11 (1000s).

The **AD7890** is a low-power single-supply (+5-V) 12-bit 8-channel data-acquisition system with 100-kHz throughput rate and processor-compatible serial output. Flexible features include Low-power and Power-down modes and accessible MUX output. It is available in a choice of input range options: 2.5, 4.0, and ±10-V full scale. It is packaged in 24-pin skinny DIP and SOIC. Prices start at $10.20 (1000s). **Circle 18**

Quad 12-bit DAC

DAC8420: 3-wire serial, flexible reference, SOIC-16



The DAC8420 is a 4-channel 12-bit D/A converter with a 3-wire serial interface and buffered voltage outputs; it is packaged in 16-lead DIPs and space-saving tiny SOICs. It operates with supplies from +5 to ±15 V, and accepts bipolar reference voltages anywhere within 2.5 V of either supply rail. Power consumption is only 35 mW max with +5-V supply. The serial interface can be clocked at up to 10 MHz. Operation is from −40 to +85°C. Prices start at $26 (1,000s). **Circle 20**

16-bit DACPORT®

Serial AD660: tiny, low-cost, Has asynchronous Clear

The AD660 is a complete 16-bit D/A converter with bit- and byte-serial input, via double-buffered latches, housed in a space-saving 24-pin DIP or SOIC package. It includes a precision buried-Zener reference and output buffer amplifier. Its versatile control logic includes an asynchronous CLEAR function to permit the output to be set to zero at any time—a useful feature in industrial applications.

The AD660 has ±1-LSB integral linearity and 15-bit monotonicity, with 83-dB signal-to-noise. Output settling is 10 μs to 1/2-LSB for a full-scale step. The serial input and output pins permit devices to be "daisy chained" with a single serial port. Various temperature and performance grades, including MIL-STD-883, are available. Prices start at $16 (100s). **Circle 22**

What's New in Amplifiers

Dual FET, 3 to ±18 V

AD822 swings rail-to-rail, Drives 15 mA and 350 pF

The AD822 is a dual precision low-power FET-input op amp that can operate from a single supply of +3 V to +36 V, or dual supplies of ±1.5 V to ±18 V. Output swing extends to within 10 mV of each rail, and the input can actually swing 0.2 V below ground with single supply.

Characteristics include offset and drift of 800 μV max and 2 μV/°C, bias current <25 pA with (10^{13}-Ω) input impedance; 1.8-MHz unity-gain bandwidth, −93 dB THD at 10 kHz, and 3 V/μs slew rate. The AD822 provides minimum full-scale output current of 15 mA and can drive 350 pF of capacitive load as a follower.

Three performance grades are available for −40 to +85°C, including a 3-volt grade; a MIL-temp grade is also available. Packaging is in 8-pin plastic DIP, hermetic cerdip, and SOIC. Prices (1000s) start at $2.04. **Circle 23**

Three Fast Multi-Channel Op Amps

Dual AD828: 130 MHz BW, Diff. gain, phase: .01%, .05° Low-power (+3 V to ±15 V) dual AD812, triple AD813

The **AD828** is a high-performance low-cost voltage-feedback dual video op amp designed for applications with closed-loop gain magnitudes ≥+2/−1. With its 130-MHz bandwidth (G=+2), high output drive (50 mA), excellent differential gain and phase (0.01% & 0.05°), and fast settling (80 ns to 0.01%), it is an ideal choice for driving back-terminated video cables. It has wide supply and temperature ranges (±2.5 V to ±18 V, −40 to +85°C), and is available in 8-pin plastic DIP and SO-8 packages. Price (1000s) is $2.10.

The single-supply **AD812**, a dual current-feedback amplifier, can operate on supply voltages from +3 V to ±15 V, drawing 5.5 mA max per channel. It features typical bandwidths up to 145 MHz, slew rates as high as 1600 V/μs, 50-mA output drive, and differential gain and phase of 0.02% and 0.02°. It is a good choice wherever many video-speed amplifiers are needed with low cost, low power, and small size. Available in 8-pin plastic mini-DIP and SO packages, it is specified for operation at temperatures from −40 to +85°C. Price (1000s) is $2.48).

The **AD813** is a low-cost *triple* current-feedback amplifier for video applications (e.g., RGB). It can operate on supply voltages from +3 V to ±15 V, drawing 5.5 mA max per channel. It features typical bandwidths up to 125 MHz, with flat response (within 0.1 dB) to 50 MHz. It has an unusual Disable feature for powering down individual amplifiers or for high impedance in multiplexing. It is housed in 14-pin DIPs and narrow SOICs and operates from −40 to +85°C. Price starts at $3.74 (1000s). **Circle 25**

Two 3-36V Families

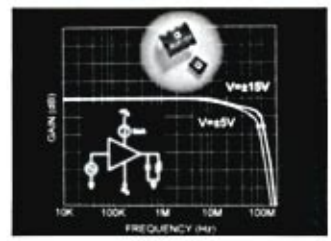
OP495 is a precision quad OP183/283 fast single/dual

Both of these families will operate with single (+3 to +36-V) or dual supplies. The **OP495** has 4 op amps with similar performance to the dual OP295. It has a low 300-μV offset voltage and accepts a wide input voltage range; output swing is rail-to-rail and it can drive capacitive loads. Quiescent current is only 150 μA per channel. It is available for industrial and military temperature ranges; packaging is 14-lead DIPs and SOL-16 surface-mount. Prices start at $3.56 (1000s).

OP183/OP283 are single and dual high-speed op amps for circuits where high gains and moderate bandwidths (5 MHz) & slew rates (10 V/μs) are required, such as filters, PLLs, and A/D buffers. They can supply 25 mA to a short-circuit load and are available in plastic DIP and SO-8 for −40 to +85°C. Prices (1000s) start at $1.42/$2.15. **Circle 24**

3,000 V/μs Buffer

±50-mA BUF04: 100-MHz; Available in SO-8 package



The BUF04, a unity-gain precision buffer amplifier with ±50-mA output current at ±10 V, 110-MHz bandwidth, and 2000-V/μs minimum slew rate (typically 3000), is available in 8-lead DIPs and narrow-body SO-8. With <1 mV offset, 30 μV/°C drift, and 4 nV/$\sqrt{\text{Hz}}$ noise, it can stand alone—or in compound with precision op amps for even higher performance. It is available for −40 to +85°C and −55 to +125°C temperature ranges. Prices start at $3.71 in 1000s. **Circle 26**

Low-Cost Dual, Quad

Single (+5 V) or dual supply General-purpose OP292/492

The OP292 and OP492 are low-cost general-purpose dual and quad operational amplifiers designed for single- or dual-supply operation. They are low-power devices (1.2 mA max, 0.8 typical, per channel at +5 V) with good performance: 4-MHz gain-bandwidth, 3 V/μs slew rate, V_{OS} <1 mV—considerably better overall performance than for comparably priced CMOS devices. Performance specs are available for +5-V and ±15-V operation for − 40 to +85°C (industrial) and −40 to +125°C (automotive) temperature ranges.

In single-supply operation, the input common-mode range includes ground; and the output swings to ground. The dual OP292 is available in 8-lead SO and epoxy DIP; the quad OP492 is packaged in 14-lead narrow-body SO and epoxy DIP. Prices in 1000s start at $1.32/$2.16 (66¢/54¢ per channel. **Circle 27**

New Interfaces, Analog Switches, Signal Conditioner

Quad SPST Switches

High-performance, Latchup-free ADG431/2/3

The ADG431, ADG432, and ADG433, housed in 16-pin DIP and SO packages, provide four independently selectable single-pole, single-throw switches. They offer similar functions to the earlier ADG21x and AD41x families, but with greatly improved performance, and trench isolation, which provides freedom from latchup.

Typical specs include fast switching time (t_{on}<165 ns, t_{off}≤130 ns), low leakage (0.25 nA), low (and flat) ON resistance (<24 Ω), and low power dissipation (3.9 μW). Switching action is break-before-make, and the switches will operate on single- or dual supplies. The switches differ in their turn-on logic polarity, **ADG431**: *low*, **ADG432**: *high*, and **ADG433**: two switches *low*, two *high*. B and T grades are available, for −40 to +85°C and − 55 to +125°C. Prices start at $2.29 (100s). **Circle 28**

RS-485 Transceivers

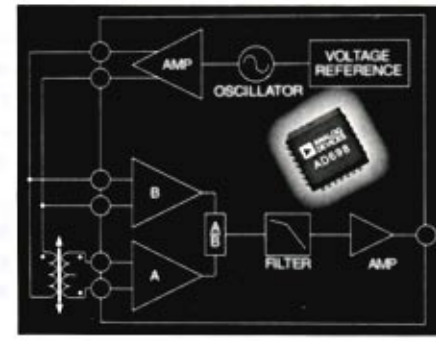
ADM485 & 1485 support fast data rates: 5 and 30 MB/s

The ADM485/1485 are differential line transceivers for communicating high-speed data bidirectionally on multipoint buses. Designed for balanced data transmission, they comply with EIA standards RS-422 and RS-485. The faster **ADM1485** supports a 30-Mb/s data rate; the **ADM485** operates at up to 5 Mb/s.

The 3-state driver and receiver may be independently enabled. Fabricated in high-speed, low-power BiCMOS, and packaged in 8-pin DIP or SO, the ADM485/1485 operate from a single +5-V supply and can handle a bus common-mode range of −7 to +12 V. Thermal shutdown protects the output against shorts and bus contention. Temperature ranges are 0 to 70°C or −40 to +85°C. Prices (1000s) start at $1.24/$1.55. **Circle 30**

LVDT Interface IC

AD698 is complete, includes sine-wave excitation



The AD698 is a *complete* monolithic conditioning system for LVDTs: providing both excitation and synchronous demodulation to decode the output of *any* LVDT or ac-bridge type of transducer. No other active circuits are needed. It is packaged in PLCC and cerdip, for operation at −40 to +85°C and −55 to +125°C, respectively. Prices (1000s) start at $8.19. **Circle 32**

CMOS Multiplexers

8- and differential-4-channel Rail-rail ADG408/09/428/29

This new rail-to-rail multiplexer family comprises the 8-channel ADG408 and ADG428 —and the differential-4-channel ADG409 and ADG429. The '428 and '429 have on-chip control latches (Write and Reset) to facilitate μP interfacing. The 8-channel muxes are controlled by 3 address lines and an Enable input; the differential 4-channel devices use 2 address lines and Enable.

These devices use an industry-standard pinout; they will operate from single- or dual supplies and will switch signals that extend to the supply rails. The switches are break-before make, and they operate at high speed (150 ns t_{on} and t_{off}), with 100-Ω ON resistance and 1.6-mW power consumption. Packaging is in 16-pin SO and DIPs. B and T grades are available for −40 to +85°C and −55 to +125°C. Prices start at $3.50 (100s). **Circle 29**

Octal Drive/Receive

ADM5170 RS-232 drivers ADM5180 RS-232 receivers

The **ADM5170** is an 8-channel line driver for RS-232/RS-423. Each channel transforms a TTL signal (up to 116 kb/s) into a single-ended ±5-V waveform that conforms to RS-232 and RS-423 protocols and to CCITT V.10/X.26. The complementary **ADM5180** is an octal receiver that transforms an RS-232, RS-422, RS-423 signal (up to 200 kb/s) to TTL, interfacing between communication lines and a CPU bus. Both functions are popular in workstations.

The drivers' 3-state outputs are protected against short circuits; the receivers operate on a 5-V supply and have differential inputs protected for up to ±25 V. Both device types, fabricated in low-power BiCMOS, are available in 28-pin plastic DIPs and PLCCs for both 0 to +70°C and −40 to +85°C operation. Prices (1000s) start at $2.72 for both. **Circle 31**

RS-232 Interfaces

ADM230L-241L +5-V-power Line drivers & receivers

The ADM230L through ADM241L are a family of eleven monolithic chips with various numbers of drivers and receivers for EIA-232-E and V.28 communications interfaces, with data rates up 100 kb/s—plus other individual features—to meet the needs of computers, peripherals, modems, printers, and instruments.

Operating on a single +5-V supply, they include a pair of internal charge-pump dc-dc converters to generate voltages such as ±10 V. Some devices have a low-power shutdown mode for reduced dissipation (to reduce battery drain). This "L" family is an enhanced low-power, faster slew-rate, smaller-capacitor (1 μF) upgrade for the older ADM2xx family and competitive devices. They are housed in 14-to-28-pin DIPs, SOICs, and SSIPs. Prices start at $1.20 in 1000s. **Circle 33**

Ask The Applications Engineer—15

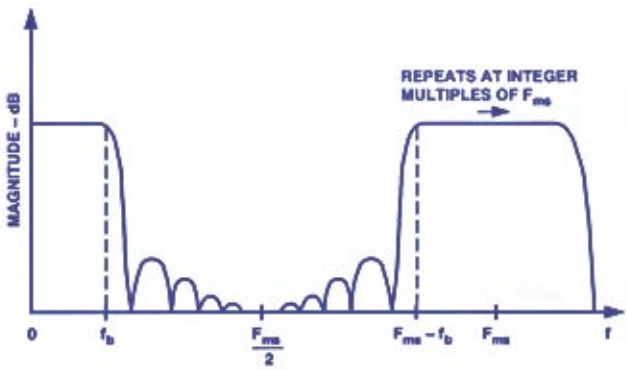
by Oli Josefsson

USING SIGMA-DELTA CONVERTERS—PART 1

Q: I'd like to use sigma-delta A/Ds but have some questions because they seem markedly different from what I've been using. To start with, what issues do I need to consider when designing my antialiasing filter?

A: A major benefit of oversampling converters is that the filtering required to prevent aliases can be quite simple. To understand why this is the case and what the filter constraints are, let's look at the basic digital signal processing that takes place in such a converter. For the purpose of anti-alias filter design we can think of a sigma-delta converter as a conventional high-resolution converter, sampling at a rate much faster than the Nyquist sampling rate, followed by a digital decimator/filter. That the input into the digital decimator is 1-bit serial with a noise-shaping transfer function doesn't matter.

The input signal is sampled at F_{ms}, the modulator input sampling rate, which is much faster than twice the maximum input signal frequency (the Nyquist rate). The figure shows what the frequency response of a decimation filter may look like; frequency components between f_b and $F_{ms}-f_b$ are greatly attenuated. Thus, the digital filter can be used to filter out all energy from the converter within $[0, F_{ms}-f_b]$ that does not fall within the bandwidth of interest $[0, f_b]$. However, the converter can not distinguish between signals appearing at the input that are in the range $[0, \pm f_b]$ and those in the ranges, $[kF_{ms} \pm f_b]$, where k is an integer. Any signals (or noise) in those ranges get aliased down to the bandwidth of interest $[0, f_b]$ via the sampling process; the decimation filter, which works only on the digitized samples, cannot be of any help attenuating these signals.



Thus it is the input noise energy in these bands $[kF_{ms} \pm f_b]$ that must be removed by the antialiasing filter before the input signal is sampled by the converter.

Q: So if I were to use the AD1877 (available in Spring, 1994), which has a dynamic range of 90 dB, the anti aliasing filter will need attenuation well above 90 dB at $F_{ms}-f_b$ (≈ 3 MHz)?

A: Not quite. You are assuming that the A/D has full-scale input at frequencies close to the modulator sampling rate; this is simply not the case in most systems. The only signal input of concern for aliasing is normally just noise from sensors and circuitry preceding the converter. The noise is usually low enough for a simple RC filter to suffice as an anti-alias filter.

Q: How do I make sure that a one-pole RC filter will suffice for my application—and establish the time constant of the filter?

A: Your application will typically specify a maximum allowable attenuation of an input signal that falls within the bandwidth of interest. This in turn puts a minimum on the 3-dB point of the RC filter. Let's take a look at an example using the AD1877 to illustrate this point further and to show how one might verify that a single-pole filter will provide enough filtering.

Let's assume that we have an application where the bandwidth of interest is 0 to 20 kHz, and signals in this range must not be attenuated more than 0.1 dB, or a ratio of 0.9886 [dB = $20 \log_{10}$ (*ratio*) for voltage and $10 \log_{10}$ (*ratio*) for power]. From the formula for attenuation of a single-pole filter,

$$ratio = \frac{1}{\sqrt{1 + (2\pi fRC)^2}} > 0.99 \text{ at } f = 20 \text{ kHz}$$

$$RC \leq \sqrt{\frac{1 - (ratio)^2}{(2\pi f)^2 (ratio)^2}} \approx 1.21 \times 10^{-6} \text{ s}$$

Choosing RC = 1.0 μs, to allow for component tolerances, the −3-dB frequency will be 159 kHz. We can now calculate the attenuation the filter will provide in the frequency bands, $kF_{ms} \pm f_b$, that alias down to the baseband. Assuming that the AD1877 has a modulator sampling rate of 3.072 MHz (and output sampling rate of 48 kHz), the first frequency band occurs at 3.052 MHz to 3.092 MHz. The attenuation of the RC filter at these frequencies is approximately 25.7 dB (about 0.052) over the whole band. Over the second band (6.124 MHz to 6.164 MHz), the attenuation is 31.8 dB (0.026). We know that the noise in these two bands (and all higher bands up the scale) that escapes through the filter to the A/D input will be aliased down to the baseband and get added as root sum-of-the-squares (rss) of their rms values, i.e., $\sqrt{n_1^2 + n_2^2 + \ldots + n_1^2}$. For values given in dB, the formulas shown the Appendix can provide results directly in dB, avoiding the intermediate step of computing the ratios.

For white noise, the noise spectral density is constant as a function of frequency, and each frequency range has the same bandwidth, so each band contributes an equal amount of noise to the input of the filter. We can therefore find the effective attenuation of the RC filter by adding the attenuation of the different frequency bands in rss fashion. The noise contribution from the first two bands, for example, is the same as the contribution from a single frequency band with attenuation of $\sqrt{0.052^2 + 0.026^2} = 0.058$, or 24.7 dB, compared with 25.7 dB for the first band. How many bands do we need to consider when calculating the total aliased noise? For this case, the rss sums of the first 3, 4, 5, and 6 bands are, respectively, −24.2, −24.0, −23.9, −23.8 dB. The first band is therefore quite dominant; its attenuation is within 2 dB of the attenuation for all bands. It is usually sufficient to take only the first band into account unless the noise is exceptionally large or has a non-white spectrum; in addition, the A/D itself, though fast, has limited bandwidth; it tends to reject high-order bands.

Now that the attenuation is in hand, we can consider the noise magnitude itself: Let's be conservative (by about 50%) and take the effective filter attenuation to be 20 dB (i.e., 0.1 V/V). To be able to calculate the maximum allowed noise spectral density when using a single pole filter, an estimate should be made of

the maximum performance degradation that aliased noise can contribute. From the dynamic specs of the AD1877 we find that the total noise power internal to the converter is 90 dB below (32 ppm of) full-scale input. If the whole system is to be within, say, 0.5 dB of this spec, the total aliased noise power can't exceed the rss difference between −90 dB and −89.5 dB or −99.1 dB (11.1×10^{-6}). Using this information, and the fact that the input scale of the AD1877 is 3 V p-p, we find that aliased noise must not exceed $3/(2\sqrt{2})$ V × 11.1 × 10^{-6} = 11.8 μV. If all this noise were assumed lumped in a single aliased band, and noting that rms noise = noise spectral density × $\sqrt{\text{BW}}$,

$$N.S.D. < \frac{11.8\ \mu\text{V}}{\sqrt{3.092\ \text{MHz} \times 3.052\ \text{MHz}}} = 59\ \text{nV}/\sqrt{\text{Hz}}$$

This is the maximum post-filter spectral density allowed. To find the maximum prefilter spectral density (MPSD), with the effective filter attenuation of 20 dB (i.e., × =10) established previously, M.P.S.D. = 10 × 59 nV/$\sqrt{\text{Hz}}$ = 0.59 μV/$\sqrt{\text{Hz}}$.

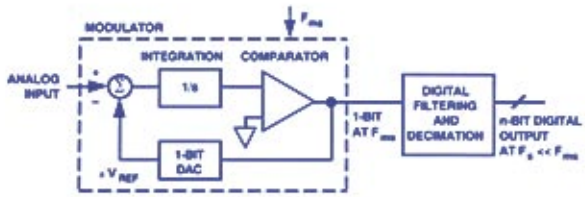
Clearly your system has to be pretty noisy in the 3-6-9-12-MHz regions in order for a simple RC filter not to suffice; however, as always, one must be careful of ambient rf pickup.

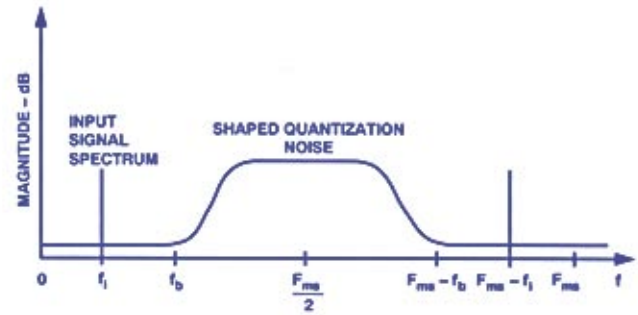
Q: *As I understand it, the noise floor of sigma-delta converters may exhibit some irregularities. Any thoughts on that?*

A: Most sigma-delta converters exhibit some spikes in the noise floor, called *idle tones*. In general, these spikes have low energy, not enough to substantially affect the S/N of the converter. Despite that, however, many applications cannot tolerate spikes in the frequency spectrum that extend much beyond the white noise floor. In audio applications, the human ear, for example, does an excellent job of detecting tones in the absence of large input signals even though the tones are well below the integrated (0-20-kHz) noise of the system.

There are two sources of idle tones. Their most common cause is voltage-reference modulation. To understand this mechanism a basic understanding of sigma-delta converters is needed. Here is a one minute crash course on sigma-delta converters (to probe further please consult).[1]

As the block diagram shows, a basic sigma-delta A/D converter consists of an oversampling modulator, followed by a digital filter and a decimator. The modulator output swings between two states (high and low, or 0 and 1, or +1 and −1), and the average output is proportional to the magnitude of the input signal. Since the modulator output always swings full-scale (1 bit), it will have large quantization errors. The modulator, however, is constructed so as to confine most of the quantization noise to the portion of the spectrum beyond f_b, the bandwidth of interest.



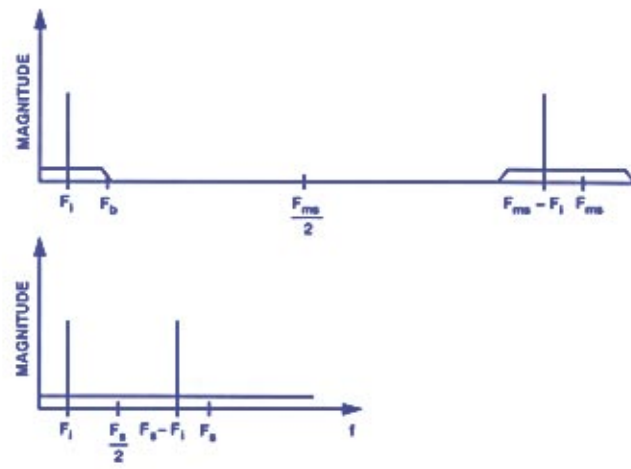


As shown, the spectral "sticks" (single frequencies) at f_i *and* $F_{ms}-f_i$ correspond to an input signal, while the shaded area shows how the quantization noise has been pushed (shaped) beyond the bandwidth of interest, f_b.

The digital filter, which is often an n-tap FIR filter, takes the high-speed low-resolution (1-bit) modulator output and performs a weighted average of n modulator outputs in a manner dictated by the desired filter characteristics. The output of the filter is a high-resolution word, which becomes the A/D output. The digital filter is designed to filter out "everything" between f_b and $F_{ms}-f_b$, *where* F_{ms} is the sampling rate of the modulator. Cleaning out all the noise in between f_b and $F_{ms}-f_b$ makes it possible to reduce the sampling rate to values between F_{ms} and $2f_b$ without causing any spectra to overlap (i.e., aliasing).

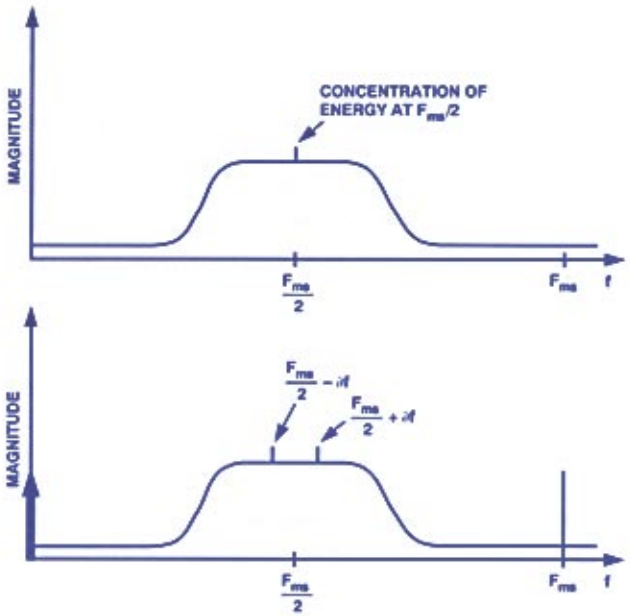
Conceptually, reducing the sample rate, i.e., *decimation*, can be thought of as only sending every dth digital filter output to the A/D output, where d is the decimation factor. This will bring the spectral images close together, as shown in the figure, which makes the output look like an output from a non oversampled converter. The upper figure shows the output of the modulator after digital filtering but prior to decimation. The lower figure shows the spectral output after decimation—the final A/D output.

In real converters, digital filtering and decimation are intimately combined for economy in design and manufacture. Thus, the terms "digital filter" and "decimator" are used interchangeably to describe the digital circuitry processing the modulator output to produce the output of the converter.



O.K., now back to "idle tones". Let's start by looking at the output of the modulator when a dc signal is applied to the input. For an exact mid-scale dc input level, the output of the modulator is equally likely to be high (1) or low (0), in other words,

the pulse density is 0.5, very likely to result in bitstream patterns like 010101. These regular patterns mean that the output spectrum will have a spike at $F_{ms}/2$ (upper figure). If the dc input now moves somewhat off midscale, the modulator output bit pattern will change accordingly. The spectrum of the modulator output will now show spikes at $F_{ms}/2-\partial F$ and $F_{ms}/2+\partial F$, with ∂F proportional to the dc change from midscale (lower figure).



With effective digital filtering, how can such tones possibly find their way down to baseband? The answer is via the *voltage reference*. The digital output is a measure of the ratio of the analog input to the voltage reference. An x% change in the magnitude of the voltage reference will result in a $-x$% change in the magnitude of the digital output word. Voltage-reference change will, in effect, amplitude modulate the A/D output. Now, we have clocks internal to the converter, and possibly also externally, running at $F_{ms}/2$. If small amounts of these clock pulses get coupled onto the voltage reference line, they will change it slightly and, in effect, modulate the tones at $F_{ms}/2-\partial F$ and $F_{ms}/2+\partial F$. One of the difference frequencies created by this modulation is at ∂F, and it is clearly in the bandwidth of interest. Nonlinearities may also create tones at multiples of ∂F.

Q: *From your explanation it seems that if I apply an ac signal to the converter I do not have to worry about idle tones?*

A: Well, any ac signal generally has a dc component associated with it, which will have to be represented by the modulator output, so the explanation above still applies. But if the total dc input offset (i.e., internal converter offset plus external offsets) in your system is exactly 0, the tones will be at dc (0 Hz).

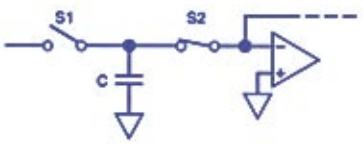
There is another source of idle tones in lower-order (<3rd-order) modulators. The order of the modulator (number of integrations) is a measure of how much quantization-noise shaping takes place. Second-order modulators can actually exhibit bit patterns that show up directly in the baseband, even if voltage-reference modulation is not occurring. This is one of the reasons why sigma-delta converters from Analog Devices that are designed for ac applications use higher-order (≥3) sigma-delta modulators.

Q: *So what can I do to minimize the chances of idle tones interfering with my A/D conversion?*

A: Follow the layout recommendations and bypassing schemes recommended by the manufacturer of the converter. This applies not only to the voltage reference, but to power supplies and grounding as well. It is the manufacturer's responsibility to minimize the voltage-reference corruption that takes place *inside* the converter, but it is up to the system designer to minimize the *external* coupling. By following those guidelines, the user should be able to reduce the coupling to a negligible level. If, despite the proper design precautions, idle tones are still an issue, there is yet another option that can be pursued. As I explained previously, frequency of the idle tones is a function of the dc input. This opens up the possibility of introducing enough dc offset on the A/D input to move the idle tones out of the bandwidth of interest to where they will be filtered out by the decimation filter. If the user does not want the dc offset to propagate through the system it can be subtracted out by the processor that handles the data from the A/D.

Q: *What kind of a load does the input of sigma-delta converters present to my signal conditioning circuitry?*

A: It depends on the converter. Some sigma-delta converters have a buffer at the input, in which case the input impedance is very high and loading is negligible. But in many cases the input is connected directly to the modulator of the converter. A switched-capacitor sigma-delta modulator will have a simplified equivalent circuit like that shown in the figure.



Switches S1 and S2 are controlled by the two phases of a clock to produce alternating closures. While S1 is closed, the input capacitor samples the input voltage. When S1 is opened, S2 is closed and the charge on C is dumped into the integrator, thus discharging the capacitor. The input impedance can be computed by calculating the average charge that gets drawn by C from the external circuitry. It can be shown that if C is allowed to fully charge up to the input voltage before S1 is opened that the average current into the input is the same as if there were a resistor of $1/(F_{sw}C)$ ohms connected between the input and ground, where F_{sw} is the rate at which the input capacitor is sampling the input voltage. F_{sw} is directly proportional to the frequency of the clock applied to the converter. This means that the input impedance is inversely proportional to the converter output sample rate.

Sometimes other factors, such as gain, can influence the input impedance. This is the case for the 16/24-bit AD771x family of signal conditioning A/Ds. The inputs of these converters can be programmed for gains of 1 to 128 V/V. The gain is adjusted using a patented technique that effectively increases F_{sw} (but keeps the converter output sample rate constant) and combines the charges from multiple samples. The input impedance of these converters is, for example, 2.3 MΩ when the device's external clock is 10 MHz and the input gain is 1. With input gain of 8, the input impedance is reduced to 288 kΩ.

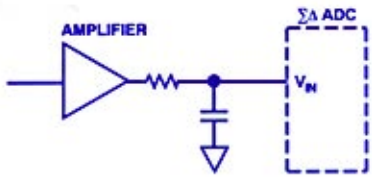
These impedances, as noted earlier, represent the average current flow into or out of the converters. However, they are not the impedances to consider when determining the maximum allowable output impedance of the A/D driver circuitry. Instead, one needs to consider the charging time of the capacitor, C, when S1 is closed. For dc applications the driver circuit impedance has only to be low enough so that the capacitor, C, will be charged to a value within the required accuracy before S1 is opened. The impedance will be a function of how long S1 is closed (proportional to the sampling rate), the capacitance, C and C_{EXT} in parallel with the input (unless $C_{EXT} >> C$). The table shows allowable values of external series resistance with f_{CLKIN} = 10 MHz which will avoid gain error of 1 LSB of 20 bits—for various values of gain and external capacitance on the AD7710.

Typical External Series Resistance Which Will Not Introduce 20-Bit Gain Error

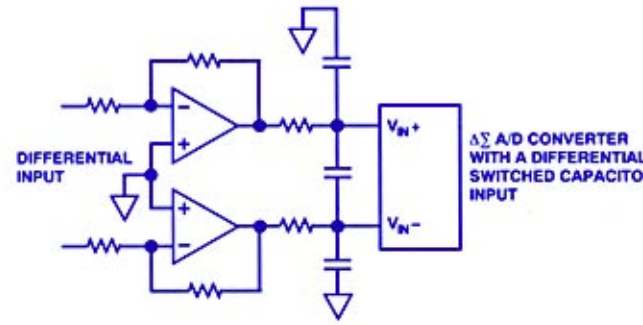
	External Capacitance (pF)					
Gain	0	50	100	100	500	5000
1	145 kΩ	34.5 kΩ	20.4 kΩ	5.2 kΩ	2.8 kΩ	700 Ω
2	70.5 kΩ	16.9 kΩ	10 kΩ	2.5 kΩ	1.4 kΩ	350 Ω
4	31.8 kΩ	8.0 kΩ	4.8 kΩ	1.2 kΩ	670 Ω	170 Ω
8–128	13.4 kΩ	3.6 kΩ	2.2 kΩ	550 Ω	300 Ω	80 Ω

For ac applications, such as audio, where the modulator sample rate is around 3 MHz for 64× oversampling, the input capacitor voltage may not have enough time to settle within the accuracy indicated by the resolution of the converter before the capacitor is switched to discharging. It actually turns out that as long as the input capacitor charging follows the exponential curve of RC circuits, only the gain accuracy suffers if the input capacitor is switched away too early.

The requirement of exponential charging means that an op amp can not drive the switched capacitor input directly. When a capacitive load is switched onto the output of an op amp, the amplitude will momentarily drop. The op amp will try to correct the situation and in the process hits its slew rate limit (non linear response), which can cause the output to ring excessively. To remedy the situation, an RC filter with a short time constant can be interposed between the amplifier and the A/D input as shown in the figure. The (low) resistance isolates the amplifier from the switched capacitor, and the capacitance between the input and ground supplies or sinks most of the charge needed to charge up the switched capacitor. This ensures that the op amp will never see the transient nature of the load. This additional filter can also provide antialiasing.



For converters that have a differential input, a differential version of this circuit may be used, as shown in the figure below. Since one input is positive with respect to ground while the other is negative, one input (the negative one) needs to be supplied negative charge while the other needs to get rid of negative charge when the input capacitors are switched on line. Connecting a capacitor between the two inputs enables most of the charge that is needed by one input to be effectively supplied by the other input. This minimizes undesirable charge transfers to and from the analog ground.



To be continued. Topics to be covered in the next installment include multiplexing, clock signals, noise, dither, averaging, spec clarifications

APPENDIX

RSS addition of logarithmic quantities: The root-square sum of two rms signals, S_1 and S_2, has an rms value of $\sqrt{S_1^2 + S_2^2}$. One often needs to calculate the rss sum of two numbers that are expressed in dB relative a given reference. To do this one has to take the antilogs, perform the rss addition, then convert the result back to dB. These three operations can be combined into one convenient formula: If D_1 and D_2 are ratios expressed in dB [negative or positive] their sum, expressed in dB, is

$$10 \log_{10} (10^{D_1/10} + 10^{D_2/10})$$

Similarly, to find the difference between two rms quantities,

$$x = \sqrt{S_2^2 - S_1^2}$$

the result, x, expressed in dB, is

$$10 \log_{10} (10^{D_2/10} - 10^{D_1/10})$$

References (not available from Analog Devices):

[1]*Oversampling Delta-Sigma Data Converters—Theory, Design, and Simulation*, edited by J.C. Candy and G.C. Temes, IEEE Press, Piscataway, NJ, 1991.

[2]J. Vanderkooy and S.P. Lipshitz, "Resolution Below the Least Significant Bit in Digital Systems with Dither," *J. Audio Eng. Soc.*, vol. 32, pp. 106-113 (1984 Mar.); correction ibid., p.889 (1984 Nov.).

[3]A.H. Bowker and G.J. Lieberman, *Engineering Statistics*, Prentice Hall, Englewood Cliffs, NJ, 1972.

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System Applications Guide, 826 pages, softcover, 1993, published by Analog Devices, $30. Topics include: Precision sensor signal conditioning and transmission; Multiplexing; Programmable gain amplifiers; High-accuracy sample-and-hold circuitry; Voltage references; High-accuracy A/D conversion; Intelligent digitizing signal conditioner; Audio applications; High-speed signals and systems; High-speed amplification; Video signal transmission & processing; Selecting the right high-speed ADC; Interfacing to high-speed ADCs; Sigma-delta ADCs and DACs; Wide dynamic range A/D conversion; Verifying high-speed ADC performance; Direct digital synthesis and high-speed DACs; Signal computing applications in communications; Motor-control circuits; Index. *Use the book order card, fax or phone the Literature Center.*

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THE AUTHORS *(continued from page 2)*

Oli Josefsson (page 26) is a Senior Applications Engineer for Analog Devices' Sound-Processing Team. His responsibilities have involved designing customer evaluation boards and providing applications support for consumer, computer, and professional-audio products. A member of the IEEE, he holds BSEE and MENG degrees from Cornell University. In his leisure time he enjoys the outdoors and strumming his guitar.

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PATENTS • • • 5,243,319 to A. Paul Brokaw for **Trimmable resistor network providing wide-range trims** • • • 5,252,908 to A. Paul Brokaw for **Apparatus and method for temperature-compensating Zener diodes having either positive or negative temperature coefficients** • • • 5,258,757 to David C. Reynolds for **Apparatus and method for increasing the output impedance of a current-type digital-to-analog converter** • • • 5,262,345 to Mohammad S. Nasser, Saurabb M. Desai, and Derek F. Bowers for **Complementary bipolar/CMOS fabrication method** • • • 5,262,934 to Colin C. Price for **Bipolar voltage doubler circuit** • • • 5,285,173 to David C. Reynolds for **Signal-controlled ring oscillator with delay cells having constant gain with change in frequency.**

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