Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

VGA

ANALOG
DEVICES
ADV7146

Volume 24, Number 3, 1990

**ANALOG
DEVICES**

Editor's Notes
PRECISION MONOLITHICS

Analog Devices recently announced the purchase of Precision Monolithics, Inc. from Bourns, Inc. PMI has now become the Precision Monolithics Division of Analog Devices, Inc. This development, a momentous occasion for both companies—as well as an important industry occasion—has had an immediate impact on this publication: an increased number of pages, including an article on the PMI TrimDAC™ (page 16).

PMI was founded in 1969—at about the same time as Nova Devices, which became the Analog Devices Semiconductor division. Introducing the world's first IC digital-to-analog converter (DAC-01) in 1970, PMI became a technology- and product leader. The DAC-01 was followed by DAC-100 and a string of precision op amps (OP-01 to OP-77) that became industry standards and led to sustained profitable growth. PMI continues its leadership, using bipolar, CMOS, and BiCMOS technologies.

Aficionados of precision monolithic analog devices are well aware of the similarities in our product lines; for example, ADI has long second-sourced such devices as the OP-07 (*Analog Dialogue* 14-3, 1980); and PMI's 1981 catalog shows the DAC-12 as a pin-for-pin equivalent of the AD562. And the list of overlaps has grown.

What our readers may be less aware of is that PMI brings to the joint effort large areas of complementary unique competencies. Here are a few examples:

- Item: PMI has developed numerous low-power and single-supply products; these are now available from Analog Devices.
- Item: PMI has taken the lead within the industry in providing SPICE models and noise analysis for analog products. Designers can look forward to the compatible extension of this to major portions of the ADI product line.
- Item: PMI is well-established in the professional audio field, through its SSM Audio Products Group. Their technology and experience should complement Analog Devices' ability to serve all ranges of the audio-equipment market, including professional, consumer, automotive, medical, military, and industrial.
- Item: Precision Monolithics has a unique track record in the ultra-reliability "Class S" field. The people, facilities, and procedures that have made this possible are now potentially available to users of a wide range of other ADI parts.
- Item: PMI products are sold through distributors. The ease of purchasing in any quantity, and the benefits of local delivery that this brings to both small- and large-quantity users will be potentially available in the future for many Analog Devices parts.

These are just a few of the ways the PMI relationship will benefit Analog Devices and its customers. Beyond this—more than ever—the combined company brings to our customers the reassurance of dealing with a leader. With our greater geographical diversity and our combined worldwide strength in people, material resources, and design and process knowhow, our markets can look for ever more advanced products. Though not yet the largest in the field, we are together on a clear track towards becoming the world leader in non-consumer analog ICs.

Dan Sheingold ▶

THE AUTHORS

Walt Heinzer, (page 16) New-Product Marketing Manager, Data Conversion, for the Precision Monolithics Division of ADI in Santa Clara, CA, defines new products and introduces new data-conversion ICs. He received BSEE and MSEE degrees from the University of California, Berkeley. Before joining PMI in 1982, he had worked at Siliconix, applying power FETs, analog switches and converters. Walt has published technical papers and contributed to the McGraw-Hill book, *Designing With Field-Effect Transistors.* In his free time, he enjoys hiking and photography.

Joe Buxton, (page 16), an Applications Engineer for the Precision Monolithics Division, has worked extensively on the development of SPICE op amp models; he writes application notes and articles for publication and also helps customers resolve their circuit and design problems. In 1988, Joe received a BSEE from the University of California, Berkeley. He enjoys bicycling, hiking, skiing, and listening to music in his leisure time.

Ian Bruce (page 8) is a Senior Technical Marketing Engineer in ADI's Marketing Communications group at Norwood MA. His photo and a biographical sketch appeared in the last issue.

Bill Schweber (page 3) is a Senior Technical Marketing Engineer and Contributing Editor to *Analog Dialogue.* Besides having his BSEE and MSEE degrees, he has designed µP-based machine controls, been a product marketing engineer, and written three textbooks. He contributes numerous articles to *Analog Dialogue* and the electronics press—many of which introduce new products to the market.

COVER DESIGN

The cover illustration symbolizes the role of the CEG/DAC™ in improving VGA graphics. Designed and executed by Shelley Cohane, of Design Encounters, Hingham MA, it includes an adaptation of a photo from Digital Art/Westlight.

RAM-DAC Upgrade Dramatically Enhances VGA Graphics

AD7148 provides 1280 × 1024 apparent resolution, 792,000 colors, transparently solves longstanding "jaggies" aliasing problem

by Bill Schweber

The ADV7141, ADV7146 and ADV7148 RAM-DACs* for video graphics use a unique algorithm to dramatically enhance the resolution, color rendition, and line quality of industry-standard VGA display systems. Using the patented Edsun Continuous Edge® Graphics scheme, these CEG/DAC™ monolithic ICs—pin- and register-compatible with standard RAM-DACs (such as the Analog Devices ADV471, ADV476, and ADV478)—contain embedded, dedicated DSP circuitry to implement the user-transparent Continuous Edge algorithm automatically.

The resolution of a standard VGA system is sufficient for some applications (e.g., bar charts), with 320 × 200 pixels and 256 colors or 640 × 480 pixels and 16 colors, yet falls short for many others, such as computer aided design (CAD), photorealistic visualization, and what-you-see-is-what-you-get (WYSIWYG) text and layout. For enough hues of a given color to create the fine shading that the eye expects to see (Figures 1, 2, and 3), these applications need a large universe of available colors, together with high resolution's fine detail and definition.

Limited resolution results in visual aliasing: lines have jagged edges ("jaggies") when they ideally should be straight or smoothly curved (Figure 1); and a limited number of displayable colors means that the smooth color shading and slight differences in hue of a photorealistic image cannot be achieved, because quantization produces observable steps in color rather than an apparently seamless transition between colors.
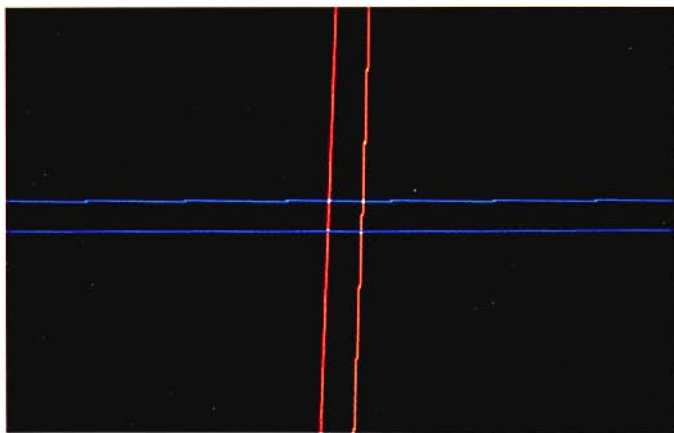

Figure 1. Nearly horizontal and vertical lines, showing visual aliasing (right-hand and upper lines), are compared with CEG-processed lines at the same slope.

*Use the reply card for technical data.

Most solutions to the age-old aliasing problem require costly higher-resolution (hence higher-speed) displays and support circuitry (workstations with typically 1,000 × 1,000-pixel or better resolution), as well as special computation-time-intensive software algorithms that are often image-dependent. CEG/DACs produce comparable images *using a standard PC platform*.

A CEG/DAC (Figure 4) combines embedded, dedicated DSP circuitry—to execute algorithms—with the traditional RAM, which embodies the video color palette (or color lookup table, *CLUT*), and the associated triple DACs (for red, green, and blue outputs). Until initialized to CEG mode, it behaves like a standard RAM-DAC. But, when the video driver software initializes it to CEG mode, the algorithm hardware—interposed between the RAM and the DACs—is activated. Pixel data fed to the DACs from memory is intercepted and processed to provide antialiasing and a wider apparent color selection.

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CEG/DACs come with a 256-word-deep lookup table in two resolutions: 18-bits for "6-bit color" (3 × 6 bits per displayed pixel), and a 24-bit-wide memory with 8 bits per primary color. Each CEG/DAC, following industry convention, has an 8-bit µP port for access to the color-palette address register, color-palette RAM, and pixel-mask register; these registers are *100% compatible with non-CEG RAM-DACs*. Information latched into the pixel port determines the DAC output states for each pixel.

THE CEG/DAC ALGORITHM

With the CEG/DAC algorithm, the color of a displayed pixel depends on the colors of the adjacent pixels. If a line of pixels forms a visual boundary (a distinct line or a color change) and the display substitutes the correctly weighted averages of the two adjacent color values for the original pixel colors, the edge will appear smooth and un-aliased. [The basics of video graphics and implications of CEG are discussed in the tutorial on page 5.]

In the CEG/DAC, only 223 of the 256 palette pixel values represent pointers to distinct colors; and in CEG mode the other 32 (one of the 256 locations is reserved for internal use) represent an opcode for computation of relative proportions of two colors. The CEG/DAC allows a set of colors to be mixed according to the desired proportions. In concept, the CEG/DAC computes a real-time weighted average—an interpolated value—for each of the primary colors of each pixel as they are read out of the palette RAM. This mixed-color (P_{MC}) calculation can be expressed by:

$$P_{MC} = P_N \,(Mix) + P_{N-1}\,(1-Mix),$$

P_N = new-pixel color, P_{N-1} = previous-pixel color, and *Mix* = mix ratio stored in the RAM.

In words, the color to be displayed is the mix-ratio-weighted sum of the input colors for the new pixel and the adjacent previous pixel. This equation is executed by DSP circuitry embedded in the device in three parallel structures—for red, green, and blue. The CEG algorithm is in effect an *interpolation* process; it blends colors of adjacent pixels to smoothly feather the perceived color as the boundary is crossed from one color region to the next.

The interpolation process assumes linearity between the numeric color value representation and the apparent screen intensity. Since a CRT's phosphors do not linearly relate displayed intensity to color number (i.e., DAC output voltage), the three mixed colors first go through a *gamma correction* circuit—an internal ROM containing the inverse color value–screen intensity transfer functions in compressed, optimized form (to reduce necessary memory space)—before they go to the RGB DACs.

The ADV7141 (triple 6-bit) and ADV7148 (triple 8-bit) are compatible with industry standard '471 and '478 devices; housed in a 44-pin PLCC, they are optionally available for 35-, 50-, and 66-MHz clock rates. A similar device, the ADV7146, in a 28-pin plastic DIP, is compatible with '171 and '476-type triple-6-bit RAM-DACs. Prices (1,000 pieces) range from $30 to $50.

VIDEO GRAPHICS AND THE CEG PRINCIPLE, A TUTORIAL

The complete display of a video graphics monitor is composed of individual picture-element dots—*pixels*—which the viewer's eye integrates to form a complete image. In a monochrome black and white monitor, each pixel can have any intensity from full-off to full-on, seen by the eye as a shade of gray. In a cathode-ray-tube (CRT) color monitor, each pixel actually comprises adjacent
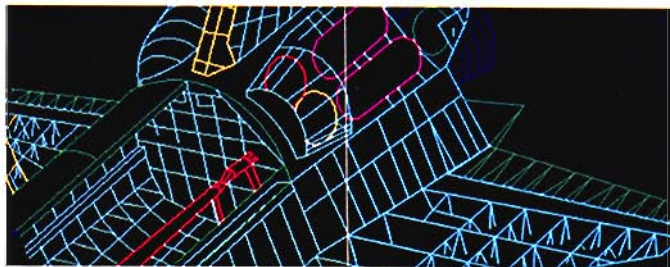

Figure 2. Split-screen CAD wireframe modeling shows both conventional image limitations (L) and CEG improvements (R).

Figure 3. Smooth color rendition and fine detail are shown in the CEG-enhanced image.

primary-color phosphors on the face of the tube (red, green, and blue, or RGB); they can be combined in varying intensities and proportions to produce the full range of visible colors and shadings. Three electron beams sweep across and down the CRT face in a repetitive pattern (*raster scan*); and pixel-determined signals control the intensity of each beam. The pixel information is synchronized with the position of the raster scan, so that pixels repeatedly appear on the screen in their correct locations.

Each pixel's intensity is established by the computer program. The hardware interface between the running program and the screen consists of a special video memory and digital-to-analog converters (DACs)—which transform the digital value associated with each pixel into an equivalent analog value ranging from pixel color *off* to full *on*. (One DAC serves a monochrome system; there are three—R,G,B—in a color system.) How many shades of gray—or primary color—each pixel can display depends on the number of memory bits per pixel and the DAC's resolution.

A monochrome system with 1 bit/pixel (and a 1-bit DAC—basically an on-off switch) will turn each bit either on or off, for black
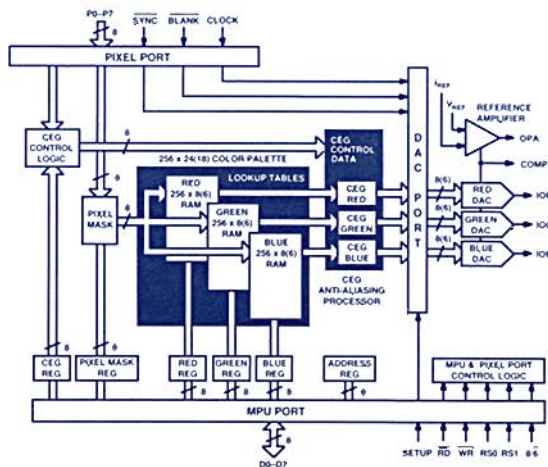

Figure 4. Block diagram of a CEG/DAC.

or white without intermediate shades of gray. A 4 bit/pixel memory, in contrast, will provide $2^4 = 16$ shades of gray, and 8 bits/pixel will make available $2^8 = 256$ shades of gray.

For color systems, the memory must be allocated among the three primary colors. The minimum memory of 1 bit per primary color (3 bits) provides a total of $2^1 \times 2^1 \times 2^1 = 8$ unique colors (TABLE). Two bits per primary color in each pixel give a total of 64 colors—6 memory bits/pixel. The display DAC must have enough resolution to use all of each color's bits of memory.

Red	Green	Blue	Perceived Color
Off	Off	Off	Black
On	Off	Off	Red
On	On	Off	Yellow
Off	On	Off	Green
Off	On	On	Cyan
Off	Off	On	Blue
On	Off	On	Magenta
On	On	On	White

A display with just 8 or 64 available colors is probably suitable for drawing simple charts and tables on screen but is insufficient for many graphics applications. As more bits are assigned to each primary color, the number of apparently available colors rises dramatically. For example, varying intensities of red and green produce a range of hues and intensities of yellow and orange.

The color potential of the memory in the graphics system is often described by the number of bits per pixel. When 6 bits are assigned per primary color, there are $6 + 6 + 6 = 18$ bits per pixel; this is known as "18-bit" color. The actual number of distinct colors that can be displayed is

$$2^6 \times 2^6 \times 2^6 = 64 \times 64 \times 64 = 262,144$$

but they may not be simultaneously displayable if the number of available display locations—pixels—on the screen is limited. Similarly, a system with 8 bits per primary color is a "24-bit" system $(8 + 8 + 8)$; it can select more than 16 million colors:

$$2^8 \times 2^8 \times 2^8 = 256 \times 256 \times 256 = 16,777,216$$

The availability of so many distinct colors may not appear to be necessary, since the screen doesn't have enough pixels to display them all simultaneously, and the eye cannot distinguish them when they are randomly placed. However, the eye can perceive small *differences* in adjacent colors, so a large available-color universe makes smooth transitions possible, permitting subtle shading and the display of photorealistic images, because the image color varies smoothly—steps between adjacent colors are small. (A picture of a red teapot illuminated by white light can show many shades of red, depending on how the light hits it.)

A perceived gap between displayed colors breaks up the image; while more colors, with smaller steps between shades of the same basic color, leads to a cleaner image. In a system with just 8 colors, the gaps are very evident; and a universe with 256, or even 262,144 colors, has noticeable gaps between colors, with a lack of smoothness in shaded areas with low- or high-contrast.

Lookup Tables: Memory can be used more flexibly, and with simplified requirements, by the addition of a programmable lookup table ("color lookup table," or CLUT, Figure 4)—a special memory area residing between the pixel information memory and the display DACs. A typical depth is 256 words.

In this "indexed" approach, instead of using pixel memory to directly create 256 display colors, the bits of each pixel can address any one of the 256 lookup table locations, producing a palette of 256 different colors. The word currently stored at the specified location generates the actual display color bit pattern for all three DACs. The palette's colors can be changed "globally" at any time by loading a different set of patterns into the CLUT.

The number of *bits* within each of the 256 words in the CLUT determines how finely the color spectrum can be divided; the number of *words* that the CLUT contains determines how many colors from that universe are displayable on a single screen.

Lookup tables permit displayed images to be altered interactively without any rewriting of the pixel values. For example, a selected band of contrast levels in a map can be expanded to show subtle variations in vegetation density. Colors can be changed during the course of a fabric design, without any recalculation within the main part of the software; only the new set of colors need be loaded into the CLUT. Lookup tables can also be used to apply unique corrections to the image, e.g., gamma correction, to compensate for nonlinear intensity functions (mentioned earlier).

The lookup tables make it easier to work with the actual color

DESIGN METHODOLOGY AND IMPLEMENTATION
A CEG/DAC is a sophisticated high-speed mixed-signal chip that adds digital signal-processing (DSP) to the already eclectic combination of analog (three DACs), memory, and miscellaneous logic found on graphics chips. To obtain the needed performance on a chip of manageable size, advanced computer-aided-design (CAD) technologies are essential. The following brief discussion may appeal to those interested in mixed-signal chip design:

The CEG/DAC device uses synchronous CMOS logic and (primarily) static memory cells. The RAM and DAC components were designed using detailed device-level circuit simulation, with a SPICE-like tool and manually-generated layout. The remainder of the circuit was captured and simulated with the Symbolics NS VLSI design tool suite. The interpolator datapath and ROM were laid out using a library of symbolic virtual grid cells created especially for this chip; the ROM was software-generated in a virtual grid from a table description of the desired contents.

The remaining modules were designed using the Timberwolf placement package, the virtual grid symbolic cells, and symbolic routing. As a result, all layouts (except the DAC and RAM) could be automatically targeted to a wide range of CMOS processes.

The top-level chip routing was performed using JANUS, an Analog Devices proprietary tool that provides automatic channel routing and compaction after manual block placement. The tool allows operator interaction, a necessity since the layout involves four internal power supplies (developed from a single +5-V external supply) and pre-defined pinout and packaging (because the CEG/DACs must be interchangeable with graphics chips). Chips were fabricated in a 1.2-μm double-level CMOS process.

Testing: Because CEGDACs must be interchangeable with devices having a limited number of observable digital outputs, testing can be hampered. To handle this, the part contains four serial scan chains: three are in the mixing logic to allow external loading and sampling of the interpolator inputs and outputs and ROM outputs; the fourth chain passes through the control logic.

range in use, but by themselves they don't change the number of potentially available colors in the overall color universe. RAM-DACs are ICs that incorporate both the CLUT memory and the three DACs, along with essential support and interface circuits—including the microprocessor bus port and pixel port (Figure 5).
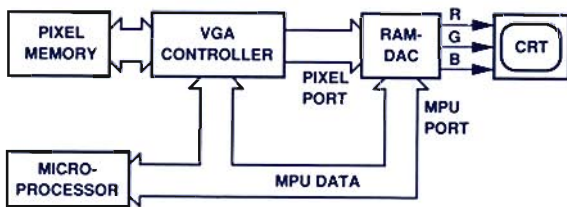

Figure 5. The RAM-DAC accepts both processor bus data and pixel data.

Pixels, Resolution, and Aliasing: Any image boundary—an abrupt change of either intensity (light blue to deeper blue) or color (red to blue), or a pair of successive changes that form a line element—as the screen is traversed, will involve one or more pixels in each row of the raster. Since the pixels are not infinitely small, some pixels in the vicinity of the boundary lie entirely within one or the other color [used synonymously with *intensity*], others straddle the boundary (Figure 6).
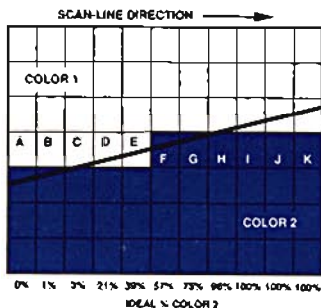

Figure 6. Straight line crossing through screen pixels. Aliasing results when choice is 100% color-1 or color-2.

Ideally, each pixel at the display boundary would display color-1 and color-2 in proportion to the area of each color within the pixel intersected by the boundary. But this is not possible, because the pixel must be set to *either* color-1 or color-2. A conventional video display circuit (and RAM-DAC) can only judge the predominant color in the pixel area and implement the choice.

The visual impact of this *aliasing* is that lines (both straight and curved) acquire discontinuities as they cross rows or columns of pixels. Even simple 1-bit monochrome line drawings and text on the screen will represent oblique lines by multiple steps, notably if the slope is just off the horizontal or vertical. In some cases, because of misalignment due to these "jaggies," two lines that should meet at a corner won't, raising problems in CAD systems.

Typically, to produce images in which aliasing and image corruption are reduced to insignificant levels, workstations are needed, with resolutions of at least 1,000 × 1,000 pixels and a universe of 262,000—or even 16 million—colors. But one might pay $10,000 to $20,000 and more for this level of performance, compared to $2,000 to $5,000 for a representative VGA system that includes PC, VGA driver circuitry, and monitor.

Continuous Edge Graphics (CEG)

CEG, a patented technique, brings workstation-like resolution

and color to VGA systems. The CEG algorithm, applied to the DAC inputs, adjusts the color of pixels along the boundary between two colors by blending them. The precise amount of blending at each pixel—the relative proportions of colors 1 and 2—is calculated by the algorithm, using the values of nearby pixels and a set of rules that specify mixing based on adjacent pixel color differences (Figure 7). The resulting "feathering" of one color into the other, *using the existing VGA display monitor and PC*, produces an apparent resolution of 1,600 × 1,280 pixels and 792,000 colors; visual resolution is 1/32 of a pixel.
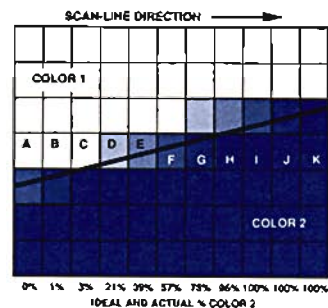

Figure 7. The CEG algorithm produces a blend of colors along the color-1/color-2 boundary.

To implement CEG, two changes to the system are needed. First, the RAM-DAC on the VGA display driver board must be replaced by the pin-compatible CEG RAM-DAC, which contains dedicated digital-signal-processing (DSP) circuitry to perform the calculations needed to adjust the color of the blended pixels. The algorithm is implemented in hardware, so the image is displayed without a time penalty—and the calculations, performed concurrently with the presentation of pixel information to the RAM-DAC, are transparent to the user.

Second, the software within the user application that presents display data to the VGA display card in the PC must be modified to prepare the display data in a slightly different format, so it can be accepted by the CEG algorithm. Modified display drivers for LOTUS 1-2-3 and Autodesk AutoCAD are available now—with more coming. The modified drivers increase execution time by a barely perceptible 10% compared to the non-CEG drivers. With the modified driver loaded into the system to replace the conventional driver, the CEG algorithm is transparent to the user: CEG images automatically replace conventional VGA images.

No changes are necessary for developed programs or software. Even after being initialized to CEG mode, the CEG RAM-DAC can be software-set to revert to conventional VGA mode and bypass the CEG DSP circuitry. This can even be done "on the fly" during the screen raster scans, making possible a split-screen display, with conventional and CEG VGA images side by side.

The ADV714X series was designed by a team including Tim Cummins, Steve Harston and Richard Meaney of Analog Devices, Inc., N. Weste and J. Leonard of TLW, Inc., and Larry Bodony of Edsun Laboratories, Inc. ◢

References:

"A 66-MHz DSP-augmented RAMDAC for smooth shaded graphics applications," by S. Harston, R. Meaney, N. Weste, J. Leonard, and L. Bodony, *Proceedings of the 1990 IEEE Custom Integrated Circuits Conference.*

Digital Signal Processing in VLSI, by Richard J. Higgins. Englewood Cliffs, NJ: Prentice Hall), 1990.

First Monolithic Triple 10-Bit Video DACs Provide True Color

ADV7121/7122 are optimized for video graphics, color correction. The 8-bit ADV7120 has similar functions for flexible performance choice

The ADV7121 and ADV7122* are the first monolithic triple-10-bit video-speed DACs. They are functionally identical; the only difference is that the ADV7122, housed in a 44-pin plastic leaded chip-carrier (PLCC), includes Blank and Sync inputs; the ADV7121, in a 40-pin plastic DIP, doesn't.

The video DACs directly drive the red, green, and blue (RGB) input circuitry of the color monitor. Their 10-bit resolution (more than 10^9 colors) makes them suitable for highest-resolution color graphics, such as medical imaging, high-definition TV (HDTV), image processing, CAD modeling, photorealistic imaging, and workstation displays.

Each CMOS IC comprises three high-speed 10-bit DACs, a TTL input interface, analog outputs, reference amplifier, and internal control register. A single +5-V supply, 1.23-V reference, and pixel clock are all that are required, in addition to the three color signals. The outputs (17.62 mA nominal for Reference White level, decreasing at 17.28 µA/LSB down to Reference Black) are compatible with RS-343A, RS-170, and most proposed studio production HDTV standards, including SMPTE 240M.

Smooth color shading requires a large number of display colors. With triple 10-bit DACs, $2^{10} \times 2^{10} \times 2^{10}$ distinct colors (just over 1 billion!) are available (though not all can be displayed in a single frame). Although there are more colors than the human eye can differentiate, such resolutions are needed in sophisticated graphics applications when performing *gamma correction*, used to linearize the drive-current/perceived-color-intensity transfer function, which results in a viewer's perceiving truer color.

The required color-shift corrections could be calculated, but they are generally provided by a separate color-correction lookup table

Figure 1. ADV7122 functional block diagram.
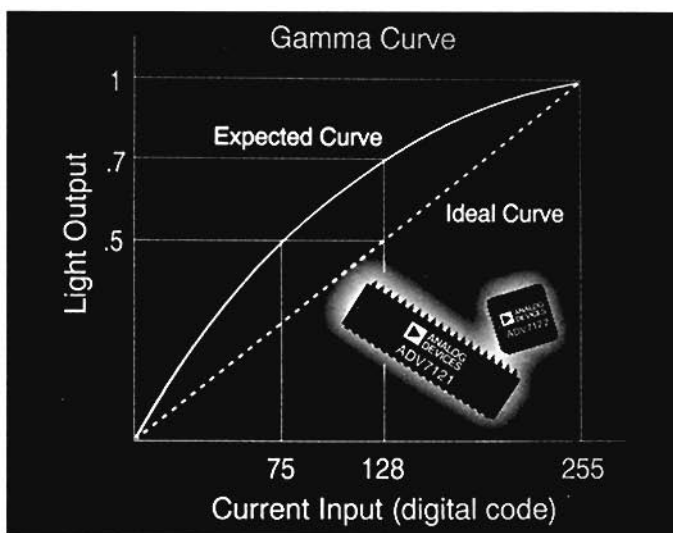
(LUT) between the system processor and the video DAC. This greatly simplifies calculations of color shadings. For example, it is much easier for the software to call directly for 463/1,024 of a given primary color by using the corresponding digital code, which is then gamma-corrected via the hardware LUT and fed to the DAC, than to *calculate* the ideal color and its gamma correction in software.

The clock speed (or dot rate) needed in a video DAC is estimated from the desired horizontal and vertical resolution, and the screen refresh rate:

clock rate = $1.3 \times$ H resolution $\times$ V resolution $\times$ refresh rate.

The 1.3 factor approximately accounts for the time required for the electron beam to retrace *horizontally* to the beginning of each new line plus the time required to retrace *vertically* to the beginning of the next frame. These 10-bit DACs are available in 30-, 50-, and 80-MHz versions; in the fastest grade, they can support a 60-per-second refresh rate for a more than $1,000 \times 1,000$-pixel raster.

Integral nonlinearity (INL) of these 10-bit DACs is ±3 or ±2 LSB, for the J and K grades, respectively, while differential nonlinearity (DNL) is ±1 LSB for the K grade and slightly greater for the J grade. Gray scale error is ±5%, maximum.

The ADV7120* is an eight-bit version of the ADV7121/7122. Housed in the same package options as the 10-bit devices, it has extra pins available for a Reference White control input, in addition to Blank and Sync; device grades are available for the same three speeds as for the 10-bit DACs.

Although it can't divide the color universe into as many colors as the 10-bit DACs, it still provides photo-realistic images via more than 16 million colors ($2^8 \times 2^8 \times 2^8$, so-called "24-bit" color), which approaches the limits of what the eye can distinguish. INL is ±1 LSB and DNL is ±0.5 LSB.

Power consumption of these devices is less than 500 mW, and price depends on clock speed. In 1,000-piece quantity, the ADV7120 ranges from $13.60 to $23.75, and the ADV7122 is priced from $19.00 to $35.30 in a 44-pin PLCC.

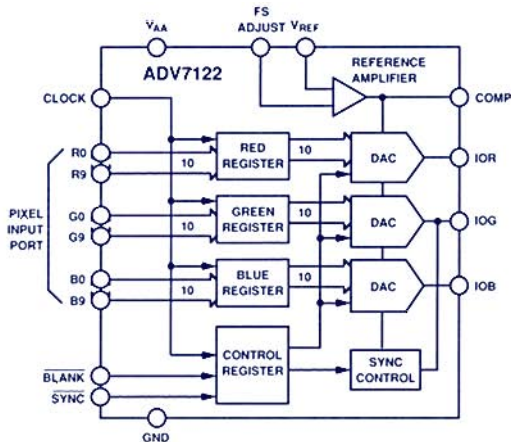*The ADV7120, ADV7121, and ADV7122 were designed by Declan Dalton at Analog Devices BV, in Limerick, Ireland.* ◗

Complete Monolithic Current Transmitter

AD694 converts a high-level voltage to a 0- or 4-20-mA current. Use it in process control loops and as a sensor transmitter

by Ian Bruce

The AD694,* a complete monolithic current transmitter, accepts high-level inputs and directly drives a single-ended 0- or 4-to-20-mA current loop. Included on-chip is an uncommitted buffer amplifier, a precision 2- or 10-volt programmable reference, a current-output driver with 4-mA offset, and an alarm circuit that detects an open 4-to-20-mA loop (Figure 1). Conversion error is only 0.15% of span with nonlinearity of ±0.005% and ±10-μA offset error.

WHY CURRENT TRANSMISSION?

Current loops are common in process-control systems because current signals—less susceptible to electrical noise than voltage signals—can be transmitted over several thousand feet using twisted pair; and they are simpler to isolate than voltage signals.

In process-control systems, current loops perform two distinct functions: they transmit control signals from a control computer to operate remote valves and actuators; and they transmit sensor information back to the control computer. These applications impose different requirements on the current transmitter because of differences in the input signals and loop-power availability.

When the current transmitter controls a remote actuator, the input is usually a high-level voltage- or current signal from the control computer via a digital-to-analog converter (DAC). The computer power supply operates the transmitter and provides power to the current loop. In the latter case, the output signals from a sensor are usually at very low-levels, and the sensor may be remote. When transmitter power supplies are unavailable, power must be derived from the current loop.

Until recently, designers of process-control systems have had to design discrete circuits or use bulky modules to generate the current signal. *Modular* solutions, precise and (often) programmable, are not inexpensive; *discrete* circuit designs are often less
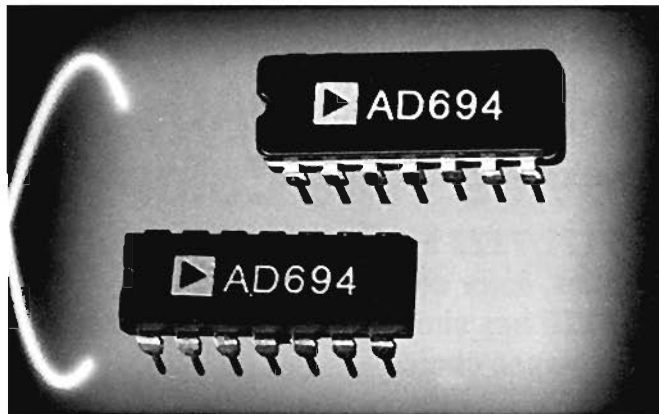
costly (but less accurate). Now cost-effective monolithic integrated circuits can replace less-accurate board-level designs to generate precise current signals.

CURRENT-TRANSMITTER ARCHITECTURE

The AD694 is optimized to provide precision current signals to control remote process-control loads.† Although specified for a 24-volt supply, the transmitter will operate from power-supply voltages between 4.5 and 36 V—a common span for battery-powered equipment. Pin-programmable input ranges are pre-calibrated to match DAC spans of 0 to 2 V or 0 to 10 V. The AD694's selectable 2- or 10-volt reference, accurate to ±0.2% over temperature, can also serve a process-control computer's DAC for accurate tracking.

The AD694's uncommitted input op amp, A1, has an initial input offset of only ±500 μV and is compliant to within 2 V of the supply voltage; it can be configured to buffer and scale an input voltage or, when a low-cost current-output DAC is used to drive the transmitter, A1 can serve as the DAC's output I/V amplifier. The buffer amplifier drives a voltage-to-current (V/I) converter over a 0-to-20-mA or a 0-to-16-mA output range (the latter adds a bias from a 4-mA offset generator to provide 4-to-20-mA operation).

The V/I converter consists of the two operational amplifiers, A2 and A3, and their associated circuitry. The first amplifier, A2, drives a Darlington transistor whose emitter is fed directly back to the inverting input of A2. This unity gain configuration forces the emitter voltage to equal the voltage value at A2's noninverting input, which is the output of the buffer amplifier, A1.

The jumper-selectable combination of R1 and R2, the two ground resistors for the transistor emitter, establish Q2's emitter ($\approx$ collector) current, 0.8 mA for 10-V input—or for 2.0-V input with pin 4 grounded. This current develops about 0.72 V across R3, and amplifier A3 forces the same voltage to appear across R4, thus forcing Q3's emitter current, I_{OUT}, to be 16 mA. (If Q2 and Q3 have equal βs, the emitter currents are in the exact ratio of R_3 to R_4). For 4-to-20-mA applications, a fixed, selectable offset current of 200 μA, added to the input-generated current, creates a fixed 4-mA output offset at the transmitter output. For 0-to-20 mA, the input voltage range is simply extended to 2.5 V (or 12.5 V)
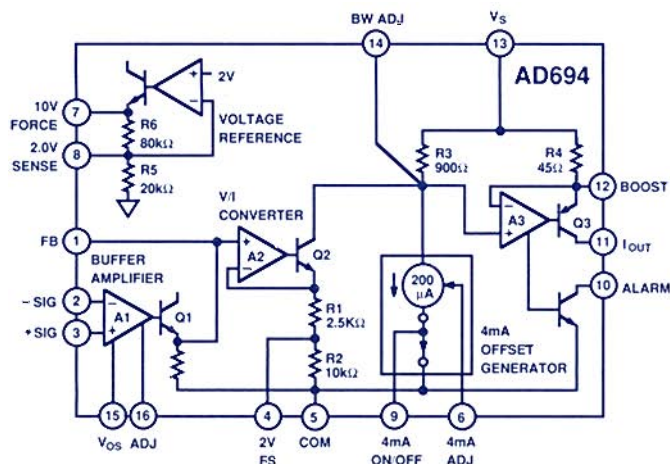

Figure 1. Functional Block Diagram of the AD694.

*For technical data use the reply card.

†Earlier, the AD693 was introduced in these pages (*Analog Dialogue* 21-1, 1987, pp. 3–6) this companion device accepts low-level signal inputs from pressure, temperature, and other process-control sensors and converts to a precise 4-to-20-mA output, deriving its power from the current loop itself.

The output voltage of the AD694 is compliant to within 2 V of the positive power supply. Three grades are available; the AD694BQ (−40 to +85°C, 16-pin cerdip package) has maximum current offset error of ±20 μA, maximum transfer-function error (span and offset) of only ±0.25% of span for full-scale inputs of 2 or 10 V, and ±0.005% maximum nonlinearity over temperature. Comparable specs for the cerdip AD694AQ and the 16-pin plastic-DIP (0 to +70°C) AD694JN are ±40 μA, ±0.5%, and ±0.015%. Pricing (100s) ranges from $3.50 for the AD694JN to $7.85 for the AD694BQ.

The AD694 is a stand-alone, complete current transmitter; it requires no external components. However, for best performance in high-dissipation applications, provisions have been made for the use of an external NPN pass transistor; this permits the majority of the power dissipation to be moved off-chip, potentially enhancing performance and extending the operating temperature range of the device (Figure 2). In such applications, the positive output voltage compliance is naturally reduced by V_{be}, the base-emitter voltage of the transistor, typically 0.7 V.
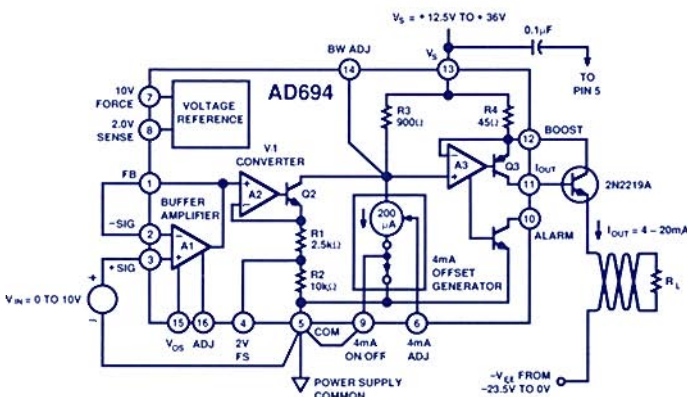

Figure 2. Using an optional pass transistor to minimize self-heating.

DIGITAL TO CURRENT—SINGLE-SUPPLY

The AD694 and a low-cost multiplying DAC are the only ingredients necessary to construct a complete digital-input-to 4-to-20-mA output interface operating from a single +15 V supply. In Figure 3, the AD694 is connected with an AD7541A 12-bit, four-quadrant multiplying DAC. Both operate from a single +15-volt supply.

The DAC is operated in a voltage mode (see *Analog Dialogue* 14-1, pp. 16-17); the +2 V reference from the transmitter is connected to the DAC output OUT1 terminal, and the reference input, V_{ref}, which serves as a voltage output in this connection, goes directly to the AD694's buffer amplifier input. In this mode of operation the DAC acts as a unipolar, noninverting voltage switch with
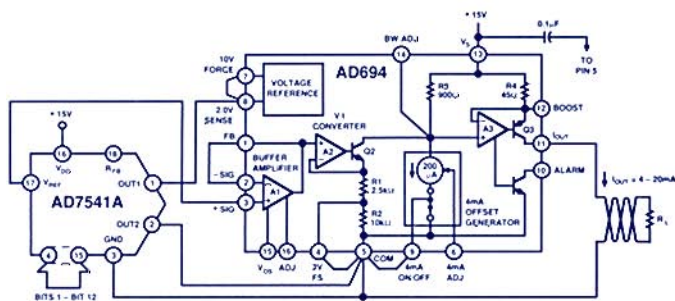
voltage output, $V_{out} = DV_{ref}(4095/4096)$, where D is the fractional gain proportional to the digital word. The AD694's input amplifier buffers the DAC with unity gain.

The V/I converter has been set for 2-V operation (pin 4 is connected to ground; this shorts R2 and increases the current gain at amplifier A2, maintaining a full-scale output of 0.8 mA for a 2 V input). Connected in this manner, a full-scale digital input code to the DAC will result in a 20-mA output (less 1 LSB), and an all-zero digital input code will result in a 4-mA output. The loading on the AD694's voltage reference is code-dependent, based on the switch state of the DAC's R-2R resistor ladder; the response time of the circuit will be determined by the reaction time of the voltage reference. The reference can source a total current load of up to 5 mA, and the force-sense terminals make it possible to add a boost transistor to increase the current drive capability.

In some applications it may be desirable to permit some over-range and under-range in the 4-to-20-mA output. For example, if an under- and over-range capability of ±5% (i.e., an output span increase of 10%) must be handled, the output current range corresponding to the full-scale digital input to the DAC is 3.2 mA to 20.8 mA. This is simply accomplished by feeding back the input buffer amplifier for a gain of 1.1, then reducing the 4-mA offset by 0.8 mA. Adjustments to the offset can be made by connecting a potentiometer between the 4 mA ADJ pin and Common, with the potentiometer wiper connected to the force pin. Adjustments can also be made to the current output's span or to the reference output in both 2-V and 10-V operation.

ALARM CIRCUIT

The integrity of the 4-to-20-mA current loop is critical in many process control systems. Detecting an open or grounded loop is easy with the AD694 alarm circuit, which warns of open circuit conditions at I_{out} (Pin 11), or of a demand to drive the voltage at I_{out} higher than (V_s− 2 V). The alarm transistor will go low if an out-of-control condition is sensed, providing a current of up to 20 mA. In a typical digital/analog system application, the alarm is connected to provide a TTL signal to the controller (Figure 4). The collector of the alarm transistor is tied to the system's logic supply through a 20-kΩ pull-up resistor. The alarm is off in normal operation, and the voltage at the alarm pin is *high*. In the event that the wire from I_{out} is opened, or if a short-circuit forces the I_{out} terminal to the vicinity of V_s, the alarm pin is driven *low*. This simple arrangement is TTL- or CMOS-compatible and can directly drive a LED or a computer alarm system.

The AD694 was designed for Analog Devices Semiconductor's Automotive and Sensor Products Group, Wilmington MA, by Analog Devices Fellow Paul Brokaw. ▶
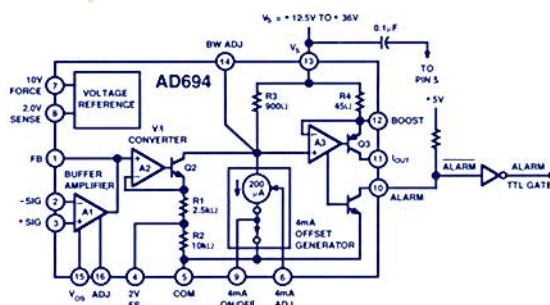

Figure 3. Single-supply digital-to-4-to-20-mA output.

Figure 4. Driving a TTL gate from the Alarm terminal.

DSP Enhancements Include IC Processors, Development Tools

ADSP-2101 Family offers selection of features, price, performance. EZ-ICE In-Circuit Emulator and EZ-LAB Demo Board ease development

System Performance

Analog Devices' family of digital signal processing microcomputers continues to grow as two new processors become available: the ADSP-2105* and ADSP-2111.* Based on the proven ADSP-2101* architecture, each has a different combination of built-in features to provide users with the optimal level of integration, performance, and price for an improved match to the universe of applications.

Along with these new devices, two new development tools for the ADSP-2101/2105 are now available. **EZ-ICE™***, a compact, stand-alone emulator, connects to a host (running a terminal emulation program) and allows users to run and debug code in their final target system. **EZ-LAB™*** is an applications demonstration board; it provides for code development, execution, and de-bugging—and incorporates analog/digital and digital/analog converters.

The ADSP-2105 and ADSP-2111

The ADSP-2101 [*Analog Dialogue* 23-2], the ADSP-2105 and ADSP-2111 are three variants of the same architecture (Figure 1) that offer a choices of performance and functionality for signal-processing applications: the popular ADSP-2101, an upgraded variation appropriate as system needs increase (ADSP-2111), and a simplified device for carefully defined, cost-sensitive applications (ADSP-2105). All three devices are software-compatible and have identical basic architectures, making the transition from one device to another relatively easy.
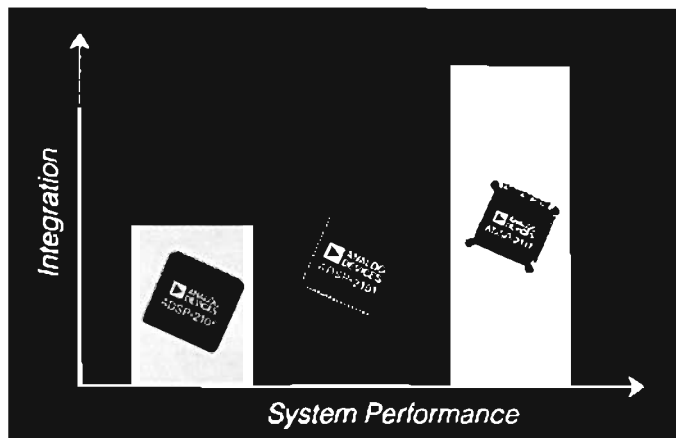
The **ADSP-2105** is a somewhat simplified form of the ADSP-2101 with one-half as much memory (1K words of program memory and 512 words of data memory—vs. 2K and 1K). In addition, the ADSP-2105 has a single serial port instead of the two ports of the ADSP-2101. Otherwise, they are pin- and code-compatible; this means that an application initiated on the ADSP-2105 can later be upgraded to the ADSP-2101 if higher performance and more on-chip capability become necessary.

On the other hand, the **ADSP-2111** is a code-compatible extension to the ADSP-2101 for increased system performance and integration. The ADSP-2111 gains flexibility by adding a Host Interface Port (HIP) for direct access to common microprocessors. The HIP (also available on the ADSP-21msp50, *Analog Dialogue* 24-2), allows the ADSP-2111 to interface to other DSPs or a non-DSP processor (typically acting as a host or supervisory processor).

The HIP is a completely asynchronous parallel I/O port with 16 data pins and 11 control pins; it can be software-configured for a variety of interface protocols including 8- and 16-bit data transfers, with multiplexed or nonmultiplexed address and data. The HIP allows the ADSP-2111 to look like a memory-mapped peripheral on the host computer bus. Status registers in the HIP provide information to both the ADSP-2111 and the host processor.
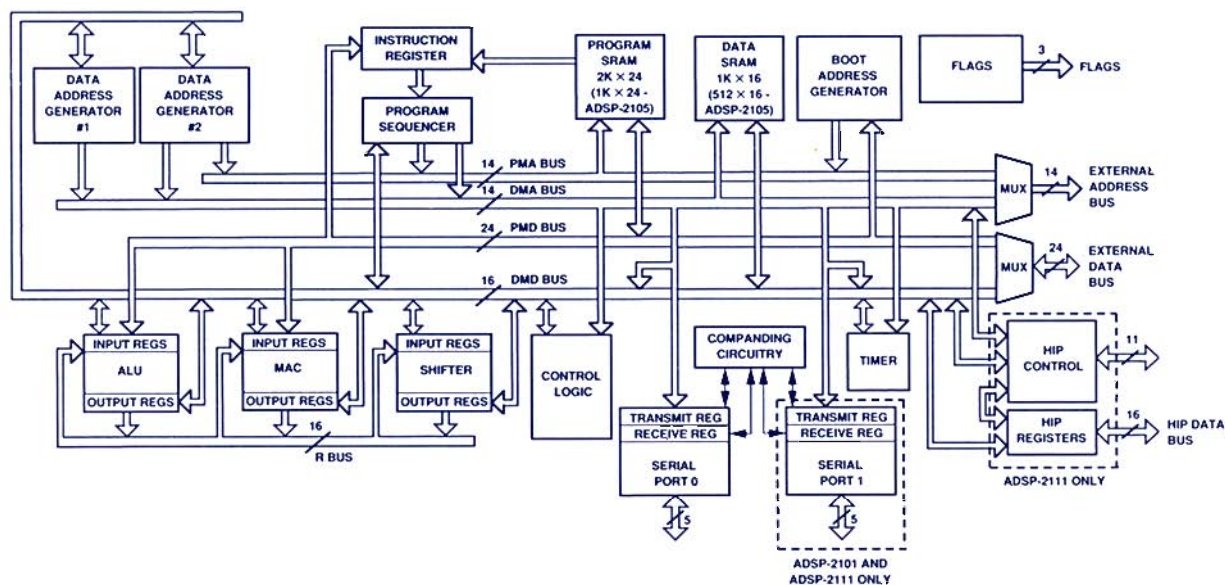

Figure 1. Block Diagram of ADSP-2111, with distinguishing −2101 and −2105 features identified.

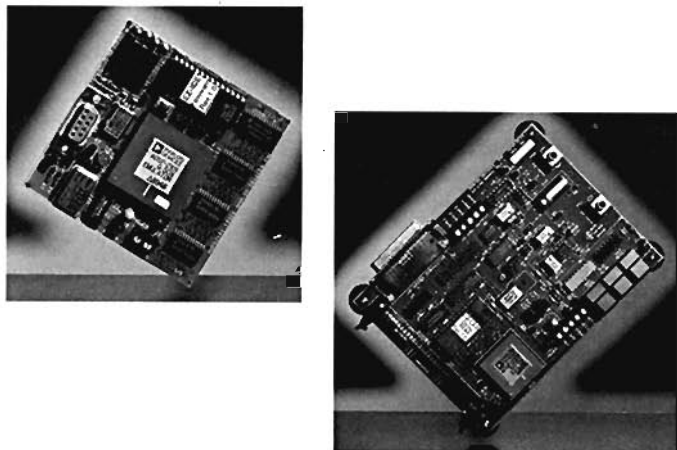*For technical data use the reply card.

Figure 2. EZ-ICE (left) and EZ-LAB.

The ADSP-2111 can be "booted" in two ways. In the first method, the contents of an external byte-wide memory IC (such as an EPROM) are loaded automatically on Reset. After boot loading, the entire program is located within the ADSP-2111 and thus executes entirely on-chip, without needing to go off-chip.

In the second method, the HIP is used. The host processor automatically transfers the program opcodes (as data) into the ADSP-2111 via the HIP. The advantage of this method is that the program can be changed by the host processor, a useful feature in adaptive applications which demand extra flexibility in establishing algorithm parameters—or the algorithms themselves.

Speed: Both devices execute as many as six operations in each clock cycle, due to their advanced signal-processing-optimized architecture. The ADSP-2105, with 100-ns cycle time, yields 10 MIPS sustained operation, while the 77-ns cycle time of the ADSP-2111 provides 13 MIPS sustained performance.

DEVELOPMENT TOOLS

The **EZ-ICE Emulator** (Figures. 2 and 3), housed on a 3.5" × 3.5" circuit board, requires just +5 V and a serial communications cable for operation. Plugged into the user's target-system board, the EZ-ICE Emulator runs and monitors ADSP-2101 programs from either target memory, emulator memory, or both. Emulated performance is at full speed—12.5 MHz—with no degradation of performance or signal timing (except that Bus Request, Bus Grant, and Reset may differ in a minor way from the data-sheet values); the clock can be supplied by the target system or the emulator itself.

All emulator operation is menu-driven from the host, using emulation firmware located in EPROM in the EZ-ICE module; the
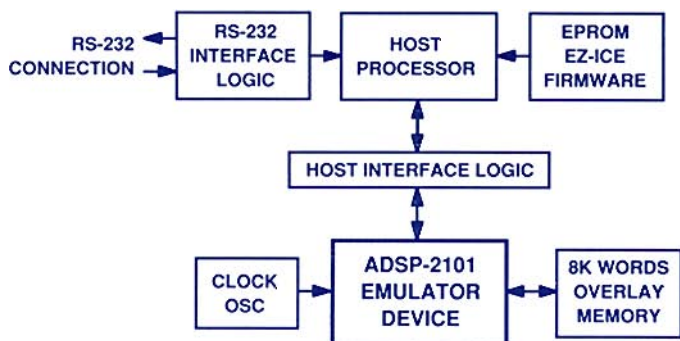

Figure 3. Block diagram of EZ-ICE.

entire emulation process is managed by an internal microcontroller. Standard emulation features include *single-step operation* (with or without register displays), *multiple breakpoint capability* (up to 16 individually set breakpoints), and *program and data memory image download/upload capability.*

The entire EZ-ICE package includes the in-circuit probe board, a cable and adapter for connection to the host computer, a user's manual, and a listing on diskette of the board's firmware.

The **EZ-LAB Demonstration Board** (Figs. 2 and 4), is a convenient and compact (4.5" × 6") vehicle for developing and debugging code for the ADSP-2101, as well as for loading and testing the effectiveness of algorithms. It accepts an EPROM containing program code (developed with one of the available development systems); the code is automatically loaded into the processor's RAM on powerup or Reset; no external memory board is needed.
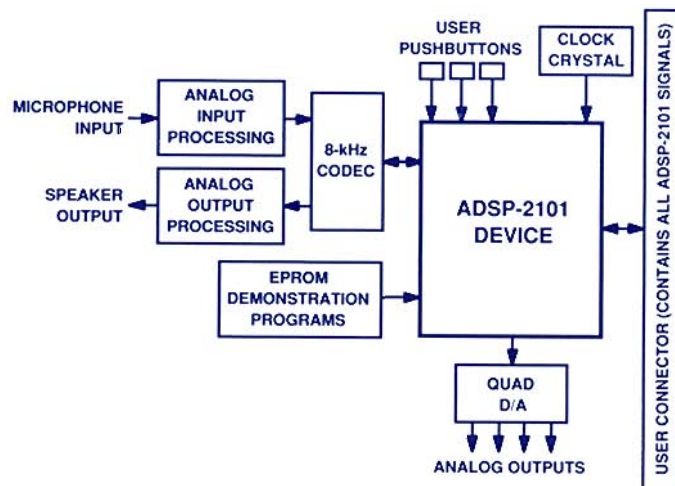

Figure 4. Block diagram of EZ-LAB.

Also included on the board are a/d and d/a converters (codec), plus a four-channel d/a converter. The converters are connected to the ADSP-2101 serial ports and can be used for digitizing sources such as a microphones or a high-impedance signal generator; the analog output (driven by the DSP) can provide an audio output via a small speaker to generate synthesized voice or tones (for example). The system includes a pre-formatted EPROM; its application programs help the user become familiar with and evaluate the ADSP-2101.

The EZ-LAB system requires +5 V and includes a user's manual and board schematic. The user can set the ADSP-2101's Interrupt and Flag In signals, or generate a Reset signal, using pushbuttons. All ADSP-2101 signals are available at a user connector on the demonstration board.

The ADSP-2105 is available in a 68-lead PLCC; the ADSP-2111 is packaged in a 100-pin PGA and 100-lead plastic quad flat pack). The ADSP-2105 is priced at $9.90 each (*any quantity from 1 to 100,000 pieces*—$0.99/MIPS); prices of the ADSP-2111 start at $87 in 100s. The EZ-ICE in-circuit emulator is $2,101 (1s), and the EZ-LAB demonstration board is $225.

These products were all designed at Analog Devices' Digital Signal Processing Division, Norwood, Massachusetts. The ADSP-2105 and ADSP-2111 were designed by the Fixed-Point Design Group; and the EZ-ICE emulator and EZ-LAB demonstration board were designed by the Applications Group. ▶

Mixed-Signal ASICs Offer Designers an Alternative Solution

Advanced software tools are essential for effective simulation. Analog Devices' JANUS system provides an integrated toolset

Mixed-signal ASICs offer design engineers the potential to reduce complex, multiple-IC designs to a single IC. Such a highly integrated, monolithic solution has the potential of being less costly, consuming less power, and being far smaller than equivalent implementations based on hybrid ICs or printed circuit boards containing discrete IC functions. While all-digital ASICs—and the requisite design support tools—have been commercially available from a wide variety of sources for many years, *mixed-signal* ASICs, which combine both analog and digital circuitry on the same silicon, are much more complex to design, simulate, and fabricate.

As a result, it is only recently that mixed-signal ASICs have become widely available and commercially viable. Analog Devices concentrates its efforts on *high-performance* mixed-signal ASICs with significant analog content and 12-bit (or better) performance.*

What is an "ASIC"? The industry has used many definitions. However, the following definition applies to the devices discussed in this article: *an integrated circuit designed for a specific customer, application, or market using cell-based techniques, where the necessary functional blocks are taken from a cell library, interconnected, and simulated to provide the desired system functions and level of performance. This definition excludes ICs designed with conventional "custom" design techniques.*

CHALLENGE AND STRATEGY

Although the goal of realizing a cell-based monolithic design for a mixed-signal device can be stated simply, significant obstacles exist. The process often used for high-performance linear circuitry is bipolar, while efficient, compact, low-power digital circuitry is achieved in CMOS. Therefore, the ASIC cell library must have both types of cells; this calls for a BiMOS process—which complicates effective modeling, simulation, and device predictability.

Of greater importance, effective simulation of the circuit's final performance is needed to cope successfully with the high costs (time and money) of developing an integrated circuit. This, in turn, requires good models and effective simulation algorithms. However, it is always difficult to simulate the subtleties of linear design—and even more challenging when compounded with phenomena often found in digital circuitry (such as noise, power-rail glitches, thermal issues, and crosstalk effects) when analog and digital circuits share a common substrate. Yet, a viable cell-based ASIC strategy demands heavy reliance on accurate simulation to get circuits that can meet the design spec in timely first silicon.

Nevertheless, typically available hardware (such as a 10-MIPS workstation) and software (a device-level SPICE simulator) cannot realistically provide system-level simulation. Either the accuracy of the simulation is poor—because unavoidable interactions between cells aren't adequately accounted for—or simulation time is too long (hours or days), or both. Any simplifications used to accelerate the simulation or reduce its complexity may excessively degrade its detail or accuracy—the inevitable speed-versus-accuracy tradeoff.

The strategies to achieve economical simulation include:

- *reduced number of nodes:* use higher-level *behavioral* models (i.e., models representing sections of circuitry having predictable behavior). This approach is supported by a general-purpose mixed-signal modeling language, and by models which represent classes of circuitry in common use, with embedded math to compute the time-domain transfer function. An example is a linear model that accepts *s*- or *z*-domain pole-zero locations to define the transfer function.

- *event driven:* only simulate when there is activity.

- *exploit latency:* restrict the number of nodes being evaluated at any event to those affected by the event (i.e., ignore *latent* nodes).

- *exploit loose couplings:* dividing the circuitry into loosely coupled and relatively independent clusters of tightly-coupled nodes (where possible) may significantly shrink the matrices to be solved.

- *simplified device-level models.*

- *coarse voltage stepping:* this implies reduced accuracy, especially with high-transconductance bipolar elements.

The benefit from each strategy varies from circuit to circuit, and the benefits of latency and loose coupling also depend on circuit dynamics. Analog Devices' strategy recognizes that a steady-state linear simulation is not enough; an effective mixed-signal simulator must be event-driven so that it can encompass devices such as d/a converters and digital logic.

The simulator should permit behavioral and device-level models to be mixed. Substantial latency requires an event-driven simulator framework; this allows the voltage resolution defining an event to be set as needed on a *per-node* basis, rather than with a single global setting. Loose coupling of nodes is desirable for speedy simulation; but the accuracy and efficient convergence of tightly coupled nodes are usually essential for effective analog simulation. One solution is to dynamically partition the active nodes into tightly and loosely coupled groups. By combining these features, computation time can be reduced without suffering a commensurate reduction in accuracy.

JANUS AND THE SPECTRUM SIMULATOR

The JANUS tool set was developed by Analog Devices to meet the needs of mixed-signal ASIC design. JANUS, a "suite" of proprietary computer-aided design tools, provides *simulation*, *autolayout*, and *unification* of the design and layout information into a single database to implement complete *design-spec-to-final-silicon* designs. Its *schematic editor* speeds design entry via an efficient user interface, which generates devices under menu-control. The editor, employing numerous time-saving techniques, provides for specification of parameters such as wire widths, routing layers, and routing priorities. It also generates the netlist used by subsequent tools automatically.

*Write for the brochure, "Mixed-Signal ASIC Designer's Guide."

Many commercially available mixed-signal simulators consist of two (or more) distinct simulators. When netlists are generated, the overall circuit is partitioned into the separate netlists of each simulator. Some newer mixed-mode simulators are driven from a single netlist and use a consistent node state-variable to minimize the signal mapping problem so that multiple algorithms can operate concurrently, but they still rely on static, predetermined partitioning of the circuit.

SPECTRUM, an event-driven mixed-signal simulator based on a *dynamic partitioning algorithm*, is more advanced. It significantly reduces simulation time by providing a flexible environment for integrating various simulation algorithms. First it statically partitions the simulation into unidirectional (causal) transfer-function coupling and bidirectional conductive coupling. It then dynamically partitions the bidirectional coupling (based on the coefficients) into loose and strong coupling during the simulation. Simulated sources stimulate the network, and the simulator produces response equations that must be solved. SPECTRUM solves each of the three kinds of response equations (tightly coupled, closely coupled, and unidirectional transfer) using the appropriate algorithm. Dynamic partitioning allows SPECTRUM to exploit circuit latency so as to reduce computational complexity where and when appropriate.

To speed simulation, the simulator adjusts the matrix size and time steps. It can operate at the transistor level, use behavioral models, or do both simultaneously; this choice permits tradeoffs between speed and accuracy. For accurate analog simulations, SPECTRUM uses ADICE, Analog Devices' enhanced version of SPICE. With its improved convergence properties, ADICE is tuned to match Analog Devices' high-performance-device fabrication processes; in the JANUS environment, it interfaces efficiently with users.

SPECTRUM has four major components: a design system interface, a modeling environment, automatic model generation, and the simulation algorithms (Figure 1).
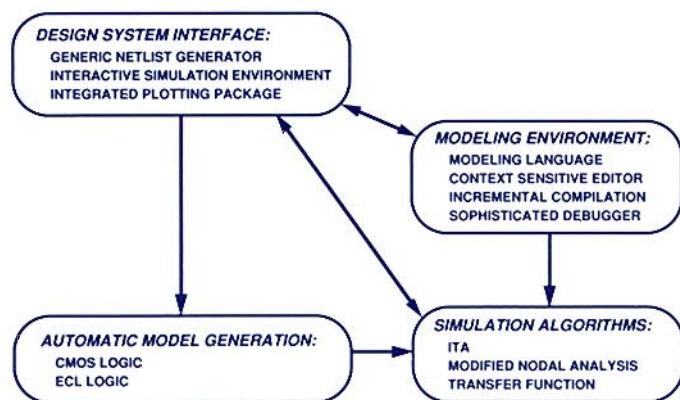

Fig. 1. SPECTRUM Architecture.

The design system (user) interface is designed to support both behavioral and diagrammatic design. In support of behavioral design, it automatically generates schematics from the model specifications. It supports diagrammatic design with: netlist generation from information provided by the schematic- and layout databases, an interactive simulation environment, and an interactive plotting environment for analyzing results (this last can show causes and effects of events on wires—enhancing debugging of large and complex circuits).

The modeling environment, an extension of common LISP, brings with it a powerful editor, incremental model compilation, and sophisticated debugging tools. The language is hierarchical—models can refer to other models—and it supports parameter passing.

For example, Figure 2 shows the SPECTRUM model for each of the binary-weighted, switched current sources of a current output digital-to-analog converter. This model defines a model named *simple-ndac-switch* with port wires, *vp*, *vn*, *io*, and *ref*, specified. Parameters of *ion*, *ioff*, and *current* may be passed to the model; if the parameter is not specified, the default value is used. To define which port wires are inputs and which are outputs, relationships between wires (transfer functions and conductive coupling) are defined within the model.

```
(define-model simple-ndac-switch (vp vn io ref)
      ((ion 0)
        (ioff 0)
        (current 0))
  (def-relation (io) (vp vn)
    (setq current (if (> (get-analog-value vp)
                        (get-analog-value vn))
                    ion
                    ioff)))
  (usepart isource "isource" (io ref) :value (get-the current)))
```

Fig. 2. SPECTRUM model for a switched-current source.

The effect of evaluation in this case is that a variable current has its value set to *ion* or *ioff*, based on whether the analog value of *vp* is greater than that of *vn*. Another model, *isource*, is used to describe the coupling between the output, *io*, and the reference port, *ref*.

The automatic model generator analyzes circuit topology and creates switch-level behavioral models. At present, the algorithm—based on pattern recognition and signal flow—generates CMOS and ECL logic models and a wide range of analog models, such as differential pairs, current mirrors, and integrators.

The algorithm begins by scanning the user-entered schematic or layout connectivity pattern for *interesting nodes* (inputs, outputs, and patterns of connected load devices, in the case of digital logic). It follows the signal path and generates appropriate logic expressions and equations, simplifying Boolean logic to reduce future computation time. The overall process of node recognition, pattern matching, and signal tracing produces a piece of LISP code that represents a behavioral model at the switch level. The incremental compiler then compiles this model code, making it available for use by the simulator.

Simulation algorithms fall into three categories—iterated timing analysis, modified nodal analysis, and behavioral (unidirectional transfer function). The appropriate one is chosen during the first phase of a SPECTRUM simulation-run (there are three phases—model evaluation, initialization, and propagation of stimulus). During the first phase, simulation wires are created and the relationships between them are defined (unidirectional transfer or conductive coupling). During the second phase, initial values are specified for the simulation wires and model parameters. In the final phase, the network created by the first two phases is evaluated. Events are placed on an event "wheel" and then evaluated in order.

When an event causes a state change on a wire, relationships associated with that wire are evaluated; this involves many paths. Unidirectional transfer functions are evaluated and results are stored in a queue. Next, statically-coupled nodes are enumerated, and the conductive coupling between them is evaluated and classified as loose or tight; different mathematical solution techniques can be used to solve each. The process iterates until convergence is reached, and charge-storage-element contents are updated. Temporarily stored results are moved to the active queue, and the next set of events is evaluated. The process continues until no further events remain on the queue, or a user-specified simulation time limit is reached.

A DESIGN EXAMPLE

In automatic test equipment (ATE), each pin of the device under test is connected to various drivers, comparators, loads, time-delay elements, leakage-current detectors, and other functions (*Analog Dialogue* 23-4). Many of these test functions are controlled or set via a dc signal level, directed by the ATE's central processor. A high-pin-count tester requires hundreds or thousands of controllable dc sources, which consume considerable power, space, and money. The number of sources can be reduced by combining them.

The AD75028 (Figure 3) is a mixed-signal seven-channel level-generator ASIC; it generates all the control voltages for a single pin of the tester. It also holds the local calibration factors associated with the pin. Instead of using seven d/a converter functions linked to a single processor interface, this device uses seven sample-and-hold circuits (SHAs) to maintain the desired dc output levels. Each SHA is sequentially refreshed (updated) automatically by the single 12-bit main DAC. The IC also contains two 8-bit DACs for gain and offset error correction, plus a clock, sequencer, multiplexer, and memory. The sequencer, functioning as an internal microcontroller, controls the memory, multiplexer, and overall operation.
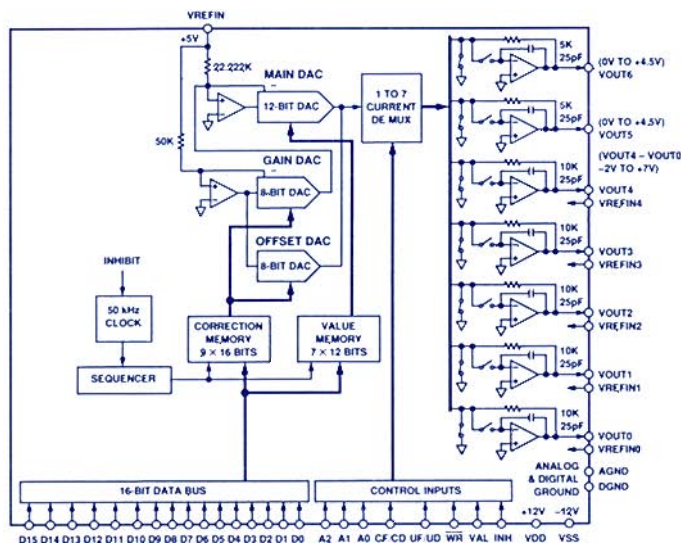

Fig. 3. Block diagram of 7-channel level-generator IC.

Each of the SHA outputs has a –2.5-V to +7.5-V overall range; the ranges of adjustment for the offset and gain DACs are ±200 mV and ±400 mV, respectively. Using the internal 200-kHz clock, the seven SHAs are updated every 140 µs. To refresh each SHA, the DAC currents are steered to the appropriate SHA, which is in sample mode; while one SHA is being addressed the other six SHAs are in *hold* mode and retain the last voltage they received from the DAC, subject to *droop*.

The design specification—which includes a functional block diagram, functional description, list of key parametric specifications, a description of the system application, package requirements, and environmental, test, and screening requirements—is used by the JANUS schematic editor to develop a device schematic (Figure 4).
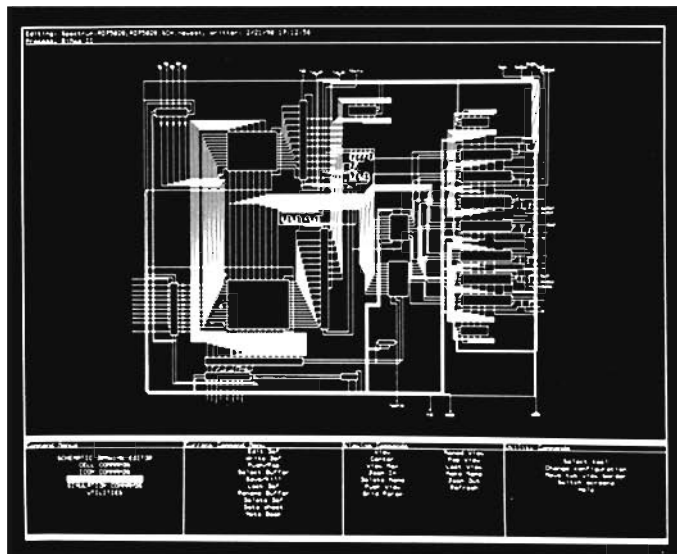

Fig. 4. Typical device schematic, showing all interconnections.

The data in the schematic ports directly to the SPECTRUM mixed-signal simulator. SPECTRUM chooses a set of voltages to represent the various digital signal levels, since the design requires internal level shifting. The user screen shows these levels—which all represent logic 0s or 1s, but with appropriately different voltages at different points—with unique colors.

The chip was simulated on two levels. SPICE simulations allowed detailed parameters, such as charge injection and pedestal error, to be evaluated. Behavioral simulations, run in the event-driven mixed-signal simulation mode, simulate the overall chip performance and ensure that the individual functions will "play together" as intended.

When the device is satisfactorily simulated, device generators create a physical representation of the circuit schematic. The placement editor optimizes the location of devices and cells—based on thermal and noise performance, die area, and net length. The layout is optimized by interactive manipulation of the polygons that represent devices.

The JANUS router (Figure 5), driven by the connection path of the schematic, permits the designer to manually control the routing of critical analog signal paths, power-, and ground lines; it uses autorouting for less-critical nets and to adjust component spacing so as to enforce the layout rules. The router can use up to three interconnect levels and will automatically expand and contract intercell spacing to achieve 100% routing. Finally, the layout is verified to assure conformance to both the schematic and design rules, using industry-standard layout-verification tools.
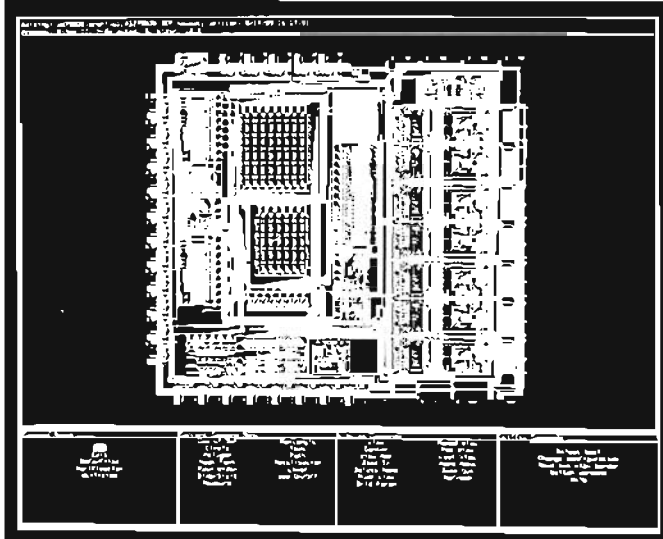
Fig. 5. Chip layout using cell routing.

The final IC design (Figure 6) was fabricated in a 24-V BiMOS process with laser-trimmed thin-film resistors and packaged in a 44-pin PLCC. The higher supply voltage allows wide dynamic range signals (other BiMOS processes in the library operate at supplies ranging from a single +5-source to dual ±15-V sources). Two levels of metal interconnect were used for expeditious autorouting.
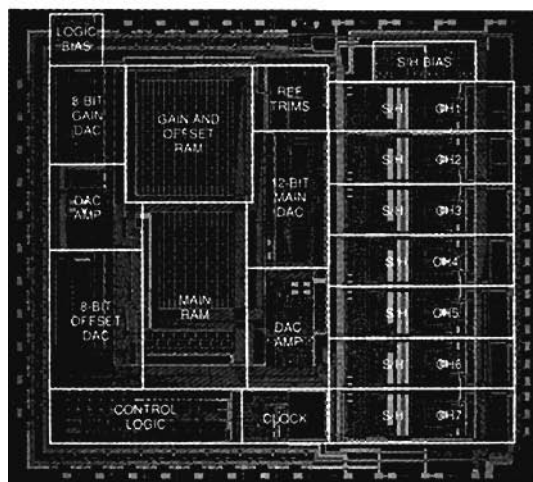

Fig. 6. AD75028 microphotograph.

First silicon was checked with the proprietary ASIC Evaluation System (AES), an integrated hardware- and software environment for circuit characterization; it is designed as part of the JANUS framework for characterizing and testing ASICs. AES is meant to provide a tool that bridges between CAD and high-volume tester environments. The AES test workstation has analog and digital test capabilities, minimum support circuitry, a flexible hardware interface, a flexible software environment, and debugging for hardware and simulation.

AES has three major sections: an IEEE-488 (GPIB) controller (a Macintosh IIx), IEEE-488 instrumentation, and a flexible interconnect system (Figure 7). Instrument I/O pins are connected to preassigned positions on a substrate board, while interchangeable application boards, configured for each chip, are mounted on this substrate board. The objective is to provide enough instrumentation to minimize the need for additional test hardware re-

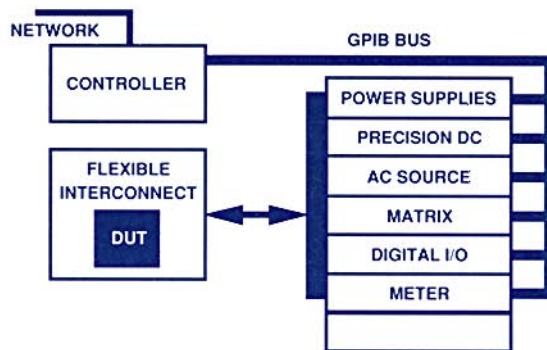sources, while standardizing the device-under-test (DUT) interface.

Fig. 7. The ASIC Evaluation System.

The *C* language is used for low-level control of the test instrumentation and for translating the desired function into the differing command sets of the individual IEEE-488 instruments. Common LISP was used to integrate and control the instruments and create an environment for design and test development.

Instruments are divided into generic families (oscilloscopes, meters, function generators, etc.); templates are created for each family and a generic command set is created for the instruments. This command set is mapped to low-level executable IEEE-488 instructions so that the user sees a friendly, consistent interface, even when similar instruments with different instruction sets are used.

To integrate the AES with the design process, the characteristics of the circuit and test resources are modeled, and "scripts" are written to manipulate the models; this links design and test, traditionally separate worlds, through the JANUS database. In Figure 8, the AES screen displays simulated and measured AD75028 linearity errors.
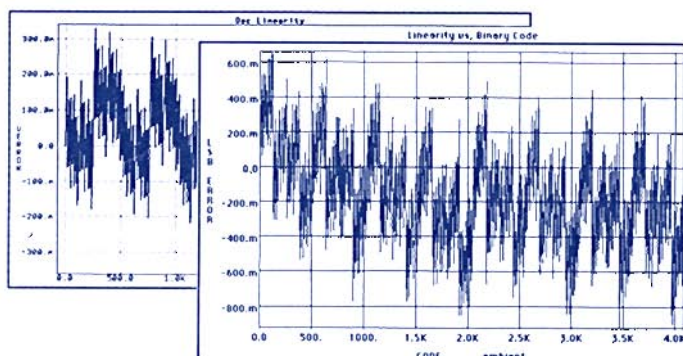

Fig. 8. AES test (right) compared with simulation of the AD75028.

This article is based, in part, on these papers* presented at the 1990 IEEE Custom Integrated Circuit Conference:

● R. Brewer, "A technical strategy for mixed analog/digital customs."
● T. Vucurevich, "SPECTRUM: A new approach to event-driven analog/digital simulation."
● G. Sheehan, G. McGlinchey, and K. Wilsher, "A 7-level generator chip for a VLSI digital tester."
● G. O'Donoghue, I. Tham, and D. Lucas, "An integrated framework for supported mixed-signal ASIC design and test."

All authors (except K. Wilsher) are with Analog Devices, Inc.'s Mixed-Signal ASIC Group (at various geographical locations). ▶

*Reprints of these papers are available free from Analog Devices.

Electronic Adjustment Made Easy With The TrimDAC™

Manipulate voltages and gains digitally, replacing pots. Serial drive keeps pin-count low. Are manual trims obsolete?

by Walter Heinzer and Joe Buxton

The TrimDAC™ is a multi-channel d/a converter designed specifically for adjusting gains and dc levels in electronic circuits digitally and without moving parts. It combines many of the properties of the adjusting pot(entiometer) with the prospect of hands-off automatic adjustment and high reliability. The highly desirable attributes of TrimDACs include small package size, many devices per package, serial interface (reduces pin count) and low power dissipation. TrimDACs in electronic adjustment reduce cost in two ways: the higher speed of adjustment under software control saves time and capital investment; and the device itself is quite cheap, less than $1 per channel.

Most designers of new circuit designs would like to avoid the once-ubiquitous variable resistor because of its mechanical sensitivity, relatively wide absolute tolerances, and high labor cost. But there is generally a need for factory adjustments and calibrations in electronic equipment. Even digital products need a power supply adjusted or calibrated to a specified tolerance. And many electronic systems are connected to real world sensors or output devices in *systems* that need calibration. A key issue facing engineers who design such systems is cost reduction of factory calibration and field maintenance.

Electronic factory-calibration of chips by semiconductor manufacturers is already widely used; calibration and adjustment problems are solved on (and with) integrated circuits by autozero, self-calibration, Zener-zap, fuse link, EPROM and laser trim. Something akin to this in larger-scale real-world systems is highly desirable.

Recognizing this problem, we sought to design products to fill the need for digitally adjustable electronic devices to automate, speed up, and eliminate manual and mechanical adjustments.

For example, consider the CRT display; curvature aberrations in the manufacturing of glass tubes require that the elements of focus (convergence & color purity) be individually adjusted, especially for high-resolution displays. Since the convergence adjustment of CRT display systems with resolutions of more than 1,000 lines requires that 6 to 8 variable-resistor adjustments be made in high-volume production—currently by robot-controlled screwdrivers—displays are ideal candidates for electronically controlled adjustment devices. The TrimDAC™ offers an attractive alternative to this mechanical adjustment approach. Previously a labor-(human or robot) intensive process taking minutes, the operation now can be done in seconds.

VOLTAGE ADJUSTMENT, THE FIRST GENERATION
The first TrimDAC, the DAC-8800,* is a monolithic CMOS IC

*Use the reply card for technical data.

with all the ingredients necessary for general-purpose dc voltage setting. It contains eight unbuffered voltage-output d/a converters in a 20-pin skinny DIP package (Figure 1). The output voltage range, unipolar or bipolar, can be independently set for each group of four DACs. Output voltage ranges are established by the choice of high- and low- external-reference inputs. The 8-bit DACs provide 256 voltage levels within each range.
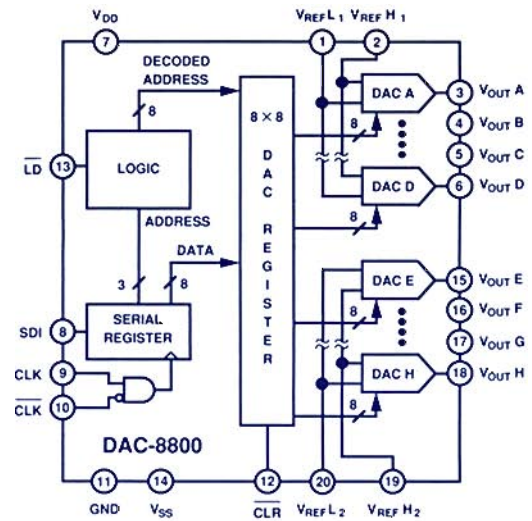

Figure 1. DAC-8800 Block diagram. Shared references determine output voltage range.

A TTL-compatible 3-wire serial interface loads the contents of the eight internal DAC registers. These can all be set to zero by an asynchronous Clear (CLR) input, very handy for system power-up. An internal regulator provides TTL compatibility over a wide range of V_{DD} supply voltages. Single-supply operation is available by connecting V_{SS} to GND. The device achieves its performance and flexibility with a low 24 mW of dissipation.

The output voltage of each DAC is changed by clocking an 11-bit word (3 address bits, 8 data bits) into the serial shift register. The internal logic decodes the three address bits to establish which internal DAC register will receive the 8 bits of data from the serial register during the Load (LD) strobe. One DAC is updated with each LD strobe. At the maximum clock rate of 6.6 MHz, all eight d/a converters can be loaded in as little as 14 microseconds.

The output voltage range is determined by the external input voltages applied to V_{REFH} and V_{REFL} (Figure 2). If V_{SS} is negative, V_{REFL} may be set to a negative value; this results in a programmable bipolar range of output voltages. The relationship between V_{OUT} and V_{REFH}, V_{REFL}, and the digital input, D (a base-10 integer between 0 and 255), is:

$$V_{OUT}(D) = (D/256)(V_{REFH} - V_{REFL}) + V_{REFL}$$

The DAC-8800 is tested for operation with V_{DD} = 12 V and V_{SS} = 0 V or –5 V. However, it was designed to operate from a wide variety of available supply-voltage combinations. Here are some typical pairings: V_{DD}, V_{SS} = +15 V, 0 V; +12 V, 0 V; +12 V, –5 V; +5 V,–5 V; +5 V, –12 V; +5 V, 0 V.

The primary application of the DAC-8800 is with fixed reference inputs for dc voltage setting. Outputs may be applied directly to high-impedance circuits—or to external op amps for buffering.

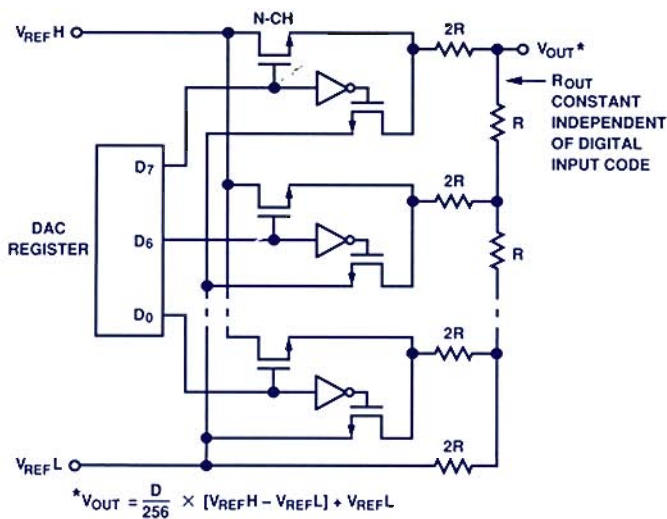$$^*V_{OUT} = \frac{D}{256} \times [V_{REF}H - V_{REF}L] + V_{REF}L$$

Figure 2. Simplified equivalent voltage-switching DAC circuit. The output resistance remains constant at a nominal 11 kΩ.

ADDING GAIN: THE SECOND GENERATION

Second-generation TrimDACs, such as the DAC-8840* and DAC-8841,* solve the problem of replacing variable resistors for adjusting ac or varying dc voltages—for example, in audio volume control. Other common applications where ac signals must be attenuated include some circuits found in video displays, projection-TV displays, instrumentation, oscilloscopes, medical gear, modulation circuits, modems, and so on.

The DAC-8840 contains a multiplying DAC structure with four-quadrant multiplying capability. Figure 3 shows the connection of one of the eight independent channels of the DAC-8840. This
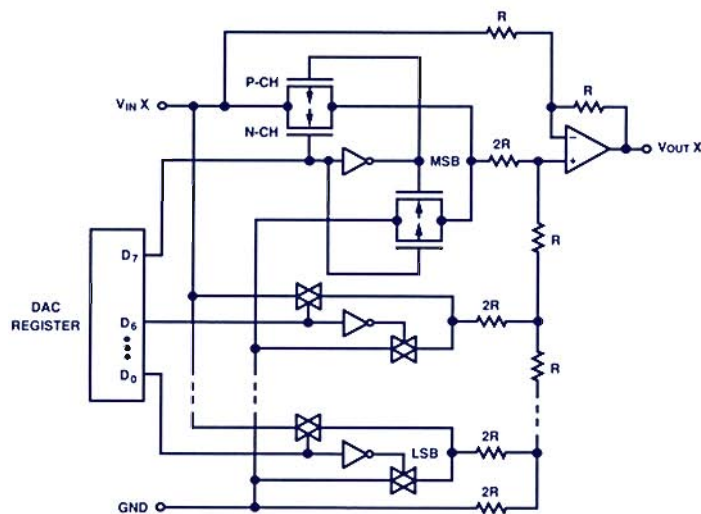

Figure 3. One channel of the Four-Quadrant Multiplying DAC-8840.

multiplying channel has a 1-MHz bandwidth for ±3-V input signal levels while operating from ±5-V supplies. A typical signal channel has 0.01% total harmonic distortion and can slew at 2.5 V/μs. Because the output amplifier is connected in a differencing (push-pull) configuration, the gain for signals applied to V_{IN} can range from full-scale positive to full-scale negative, depending on the applied digital (offset binary) word. The magnitude of the binary word corresponds to the wiper position of a pot, with zero output at half-scale; a Preset control input sets all DACs to this "zero" position. Figure 4 describes this serial input CMOS octal D/A converter in greater detail.
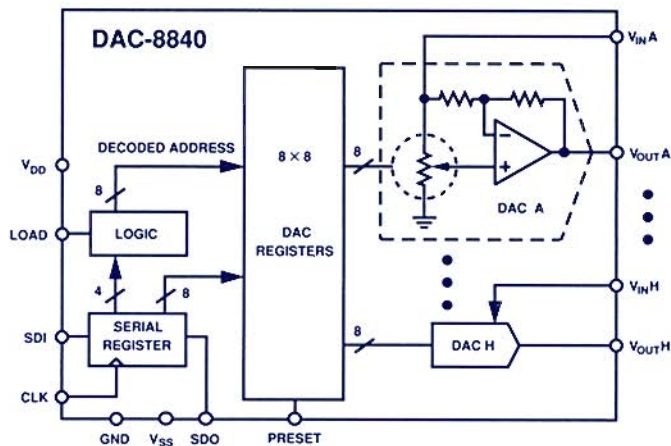

Figure 4. DAC-8840 block diagram. Note the 3-wire input and serial data output pin (SDO) for daisy-chaining additional packages.

The gain transfer function of a DAC-8840 channel is:

$$V_{OUT}(D) = (D/128 - 1) \ V_{IN}$$

where D is the value of the binary input, a decimal integer between 0 and 255. At full-scale, $V_{OUT} = 127/128 \times V_{IN}$; when $D = 128$ (also the Preset condition), V_{OUT} equals zero volts; and when D = zero, $V_{OUT} = -V_{IN}$.

In the DAC-8840, eight DAC registers store the output state; they are updated from an internal serial-to-parallel shift register loaded from a standard 3-wire serial-input digital interface. The data word clocked into the serial-input register (SDI) consists of 12 bits; the first four determine the address of the DAC register to be loaded with the 8 data-bits. A serial data output pin at the other end of the shift register (SDO) allows simple daisy-chaining in multiple DAC applications without additional external decoding logic (Figure 5). The fourth address bit, which decodes as a NOP for the package, makes it possible to select a single DAC in one of the packages to be updated when all the packages receive the common LD DAC strobe signal.
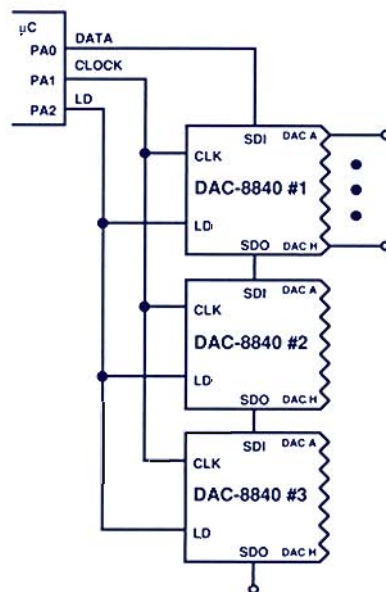

Figure 5. DAC-8840s in a serial daisy chain minimize chip decoders.

The DAC-8841, a mask option of the DAC-8840, offers an ideal octal DAC for +5-V single-supply applications. The DAC and

amplifier of each channel are configured as shown in Figure 6, with the amplifier connected for a non-inverting gain of two. This configuration is a 2-quadrant multiplying arrangement with a 1-MHz bandwidth. AC signals applied to the V_{IN} terminal can be attenuated to zero or amplified by a factor of up to two, with 256 possible level settings from zero to $2 \times (255/256)\,V_{IN}$:

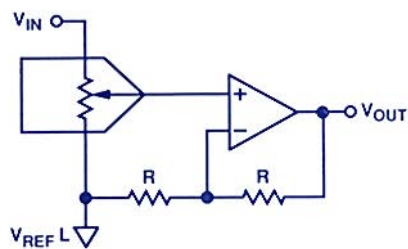$$V_{OUT}(D) = 2 \times (D/256) \times (V_{IN} - V_{REFL}) + V_{REFL}$$

Figure 6. Internal connections of the +5-V-only DAC-8841.

VARIABLE RESISTORS VERSUS TRIMDACS

From the above overview of the DAC-8800 and DAC-8840/41 TrimDACs, we can compare them to mechanically variable resistors (pots), reviewing the strengths and weaknesses of each.

Advantages of TrimDACs over Potentiometers: Better mechanical stability, improved product life, improved temperature coefficients, smaller size; computer control can eliminate technician costs; remote operation, constant output resistance, and low output resistance with low power dissipation.

Advantages of Potentiometers over TrimDACs: Voltage range usually much greater, no separate power supply required, simple human interface, no memory required, no "zipper noise" (the sound heard when using a DAC to adjust audio levels).

Another useful advantage of the potentiometer at present is a nonvolatile memory. That is, in a vibration-free environment, the wiper of the potentiometer stays where it was last set, even with the power off. The TrimDAC™ devices described here do not contain nonvolatile memory; for them, the required memory is generally supplied by system E^2PROM. Since in many of today's systems a low-cost high-density E^2PROM holds system set points for current time, date, mode, parameters and so on, it is an easy matter to share this nonvolatile memory with the TrimDAC calibration set points; they are reloaded at system powerup.

Figure 7. Setting gain of a voltage-controlled amplifier in professional audio equipment. One DAC-8800 can serve 8 channels. The damping capacitor at the voltage-control point minimizes zipper noise by slowing rates of gain change to subaudio frequencies.

TYPICAL APPLICATIONS

In professional audio equipment, voltage-controlled amplifiers (VCA) are used to set gain, fade, pan and mix signals. The dc

control inputs of these VCAs are ideally controlled by the DAC-8800 (Figure 7). The addition of the capacitor at the VCA voltage control port, VC, helps to limit the slew rate, reducing the clicking to a subaudible level. One DAC-8800 can control 8 channels of logarithmically set gain and attenuation levels.

Figure 8 shows a selection of output configurations of a DAC-8800, including simple buffers, summing circuits with coarse/fine control, and adding gain for increased output swing. A DAC-8800 can be used in system offset nulling by connecting its output to the summing node of any convenient op amp, using an appropriate value of summing resistance or a T-network.
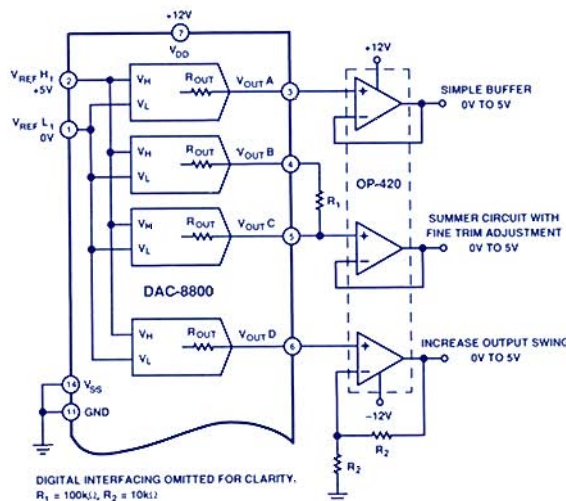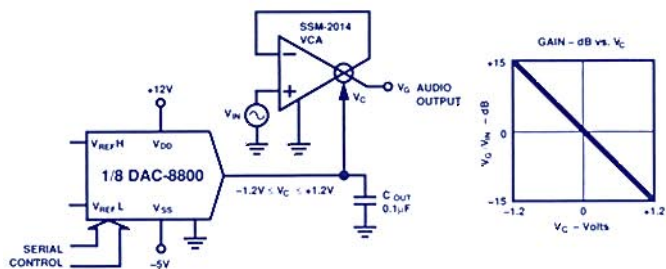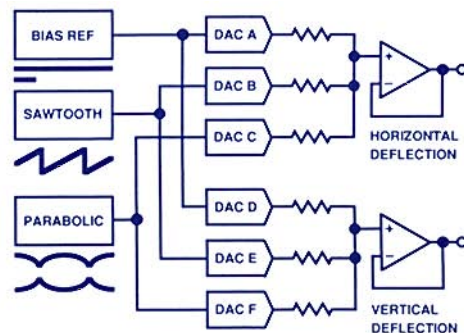

Figure 8. Some ways of buffering the DAC-8800 output.

For video convergence and deflection control, especially in multi-sync displays, the DAC-8840 can be used to adjust the sawtooth waveform amplitudes, their reference bias voltages, and the parabolic waveforms used to linearize them as they are summed together to drive the CRT deflection. Figure 9 shows a block diagram of a typical arrangement.

Figure 9. DAC-8840's four-quadrant multiplying capability simplifies amplitude adjustment of waveform components in video deflection.

Availability

The 20-pin DAC-8800, and the 24-pin DAC-8840 and DAC-8841 are available for two temperature ranges—extended industrial (−40°C to +85°C) and military (−55°C to +125°C). Packaging includes plastic and ceramic DIPs and SOL surface-mount packages. DAC-8800 pricing starts at $7.50 (100s) and DAC-8840/41 start at $9.95.

The DAC-8800 was designed by Patrick Copley, who also—with Jim Brubaker—designed the DAC-8840 & DAC-8841 at the Precision Monolithics Division of Analog Devices, Santa Clara, CA. ▶

Two Precision Dual-Op-Amp Families
$V_{os} <$ 50 μV, $I_{os} <$ 100 pA, $I_{sy} <$ 625 μA/channel
AD706 & OP-297 trade gain & I_{bias}

The AD706* and OP-297* dual low-noise op-amp families are designed for use in precision dc and low-frequency instruments. They combine low offset voltage (V_{OS}) and drift (100 μV max over temperature), plus low offset current (I_{OS}); this suits them well for amplifying signals from strain-gage bridges and other sensors, low-frequency active filters, and general-purpose linear and nonlinear operational circuitry. At the same time, their low quiescent supply current (I_{sy}) makes them ideal for battery-powered equipment.

The amplifiers are similar in many ways, differing principally in that the OP-297 family have higher minimum gain (2,000 vs. 300 V/mV) and CMR (120 dB vs. 114 dB), while the AD706 has lower maximum bias-current drift specs (200 pA vs. ±450 pA). If all else were equal, this tends to favor the OP-297 in differential and high-closed-loop-gain applications, while the AD706 would
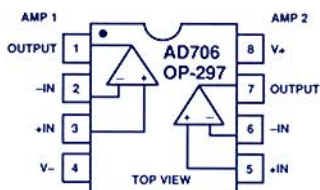
be used to meet matching requirements and with higher-resistance operational circuitry. The AD706 and OP-297—paired AD705s* (*Analog Dialogue* 24-1, p. 18) and OP-97s* on a single chip—can also save space and cost in applications designed for numerous single devices. [Quads are also available. See page 27.]

Typical slew rate is 0.15 V/μs for both families. Grades are available for all popular temperature ranges, including −55 to +125°C (and /883). Both families are available in plastic miniDIPs, 8-pin cerdip, and SO, and OP-297 is available in LCC. Prices for both devices start at $2.01 in 1,000s. ◣

Low-Noise, Low-I_B FET-Input Op Amp
AD645: 9 nV/$\sqrt{Hz}$ at 1 kHz, 1 V p–p 0.1 to 10 Hz
1.5 pA max I_B ; 0.6 fA/$\sqrt{Hz}$ I_{noise} (0.1 Hz–20 kHz)

The AD645* is a low-cost high-precision monolithic op amp combining the low current noise of FET inputs with the low voltage noise associated with bipolar inputs. It is available in both a plastic mini-DIP and a hermetic TO-99. Its low noise and errors make it especially suitable for photodiode preamplifiers and other uses in sensitive medical and analytical instruments—and for applications where OPA-111 is considered.

Maximum dc error specs (K grade) include 250-μV V_{OS}, 5 μV/°C drift, and 1.5-pA I_B (after warmup), combined with a minimum voltage gain of 1,000 V/mV (120 dB). These are accompanied by low peak-to-peak voltage noise (2.5 μV max, 1 μV typical, 0.1 to 10 Hz), with low midband spectral density (12 nV/$\sqrt{Hz}$ max, 9 typical at 1 kHz)—and comparably low J_{NOISE} values: 15 fA max p–p, 11 fA typ, 0.1 to 10 Hz, with 0.8 fA/$\sqrt{Hz}$ max, 0.6 typical at 1 kHz.
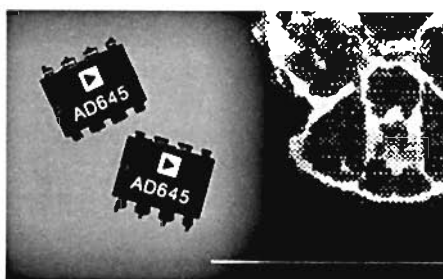

Dynamic performance is good—2 MHz unity-gain bandwidth and 2 V/μs slew rate (1 V/μs max), with full-power response to 16 kHz min, and settling time of 8 ms to 0.01%. THD at 1 kHz (3 V rms output into a 2 kΩ load) is a low 0.0006% (−104 dB).

J/A and K/B grades are available for 0 to +70°C/−40 to +85°C operation, and S grade is for −55 to +125°C (/883 is also available). Prices (1,000s) for the plastic-packaged J/K grades are $2.51/$3.76. ▶

Video Op Amp
AD829: 120-MHz BW
Low noise—2 nV/$\sqrt{Hz}$
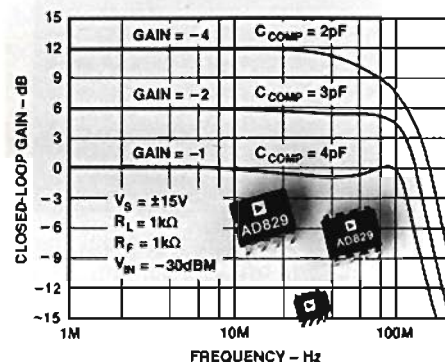
The AD829*, a high-speed, low-noise operational amplifier, is designed for both audio and wideband applications. Low differential gain and phase errors make it especially useful in amplifying and buffering video signals; however, its low noise is also helpful in preamplifiers, and its wide bandwidth and low output impedance make it a good input buffer for high-speed a/d converters.

The AD829 needs no compensation when connected for closed-loop "noise" gains greater than 20 V/V. For lower gain values, the C_{COMP} terminal is used for tailoring the compensation for optimum bandwidth, using either traditional *shunt* compensation or *current-feedback* compensation.

Noise is low: voltage noise spectral density of 2 nV/$\sqrt{Hz}$ from less than 1 kHz to beyond 10 MHz, and—for current—1.5 pA/$\sqrt{Hz}$ at 1 kHz.

Small-signal bandwidth is 120-MHz for gain of −1 and 50-MHz for +1; full-power bandwidth is 25 MHz, (V_o = 2.2-V p–p, 150-Ω R_{LOAD}). Differential gain and phase errors are 0.02% and 0.04° (at 3.58 MHz, NTSC; 4.43 MHz, PAL and SECAM).

In addition, dc precision is excellent: 1-mV max input offset voltage over temperature, with 0.3 μV/°C average drift.

Specified for ±5 to ±15-volt supplies, AD829 delivers ±3 V into a 150-Ω load (±5 V). All three ranges of temperature are available; packages are plastic miniDIPs, SOICs, and cerdip. Prices for the plastic AD829JN/JR start at $2.51 in 1,000s. ◻

*Use the reply card for technical data.

±10-V Reference
AD688: tracking-outputs
±2-mV absolute error (B)
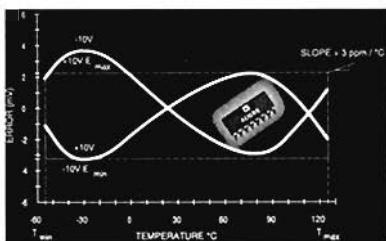
The AD688,* the first low-cost monolithic ±10-V reference with tracking outputs, is ideal as a high-precision dual-reference for systems applications where low tracking error, low initial offset, low drift, and low noise are required. Examples: transducer excitation, systems with 10-to-16-bit data converters, autocalibration systems, power-supply controllers, and precision I sources.

Like the AD588 (*Analog Dialogue* 21-1, 1987, pp. 12-13), the AD688 uses a buried Zener diode for stability and low noise—and laser trimming to minimize initial error and temperature drift. Similarly, it uses three laser-trimmed amplifiers with the basic reference cell; the first is used for ground sensing, while the other two buffer the +10 and –10-volt outputs. The amplifiers are configured to permit Kelvin connections to the load and/or boosters for driving long lines or high-current loads without losing accuracy due to line drops.

Accuracy specifications (AD688BQ) include an initial error of ±2 mV maximum, with ±1.5-mV max tracking error and drift less than ±3 ppm/°C (–40 to +85°C) and ±1.5 ppm/°C (0 to 70°C). Line regulation is ±200 μV/V max, and load regulation is ±50 μV/mA max for both outputs over a 10-mA swing of current. Output noise is 6 μV p-p, 0.1 Hz to 10 Hz, with rms noise spectral density of 140 nV/$\sqrt{Hz}$ at 100 Hz. Long-term stability is 15 ppm over 1,000 hours.
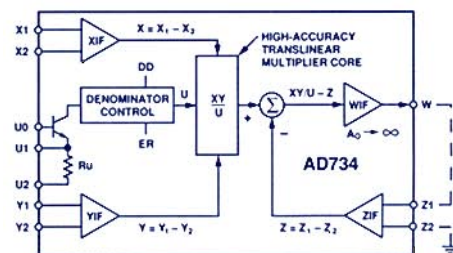
In addition to the B grade, there are a lower-cost A grade (same temperature range, somewhat looser specifications) and an S grade for –55 to +125°C; an /883B version is also available. All grades are housed in a 16-pin hermetic cerdip package. Prices (100s) start at $12.75/$21.50 (A,B). ▶

*Use the reply card for technical data.

Low-Distortion Analog Multiplier
AD734 has 94-dB SNR and 0.25% FS error
10-MHz full-power bandwidth and low cost

The AD734* is a high-accuracy, low-distortion, four-quadrant monolithic analog multiplier with 10-MHz full-power bandwidth. It is pin- and function-compatible with its predecessor, the venerable AD534 (*Analog Dialogue* 11-1, 1977, pp. 6-9). With its high accuracy (0.1% typical error, 0.25% max), 450-V/μs slew rate, 200-ns settling time to 0.1%, and low distortion (–80 dBc from any input), the AD734 may well be the most accurate and lowest-distortion IC analog multiplier on the market. Its cost is low, too, starting at $10.55 in 100s (AD734AQ).

It will multiply, divide, square, and root, and can be used in precision AGC and voltage-controlled amplifiers, filters, and oscillators. It also functions as an ultra-low-distortion mixer, with a +43-dBm 3rd-order intercept. Audiophiles will love its 94-dB SNR (10 Hz to 20 kHz—and still 70 dB at 10 MHz). Other application areas include RF and IF signal processing, avion-


ics, video, and analytical instrumentation.

Like the AD534, the AD734 continuously performs the operation, $W = XY/U$, where X and Y are positive or negative differential inputs. The AD734 allows direct division, with U controlled directly (preferred), as well as feedback division in the manner of the AD534.

Available grades include A and B, for industrial (–40 to +85°C) temperatures, and S for military (–55 to +125°), with devices available to /883B. Packaging is in hermetic cerdip. Price (100s) is $10.55 (AQ). ▶

Monolithic Unity-Gain Voltage Buffer
AD9620 has 600-MHz bandwidth, low distortion
Use it to boost current and transform impedances

The AD9620* is a monolithic unity-gain buffer with wide bandwidth (600 MHz) and low distortion. With its low gain error (–0.1 dB max) and the ability to drive 40-mA loads, it is ideal for impedance transformation in wideband analog circuits requiring low output impedance—e.g., as a driver for flash ADCs or in driving coaxial cables. Applications include instrumentation (oscilloscopes, spectrum analyzers, waveform generators), IF/communications systems (radar, ECM, C³I), and military.

Gain is 0.994 V/V typical, 0.989 (–0.1 dB) min. Small-signal bandwidth is 600 MHz typical, 320 MHz min, while large-signal bandwidth is 80 MHz typical, 60 MHz min (40 MHz min at T_{max}). Typical slew rate & settling time are 2,200 V/μs & 8 ns to 0.02% (1,500 V/μs min & 16 ns max). Noise spectral density is 2 nV/$\sqrt{Hz}$ at 10 MHz; and wideband (0.1 to 200 MHz) noise is 28 μV rms.
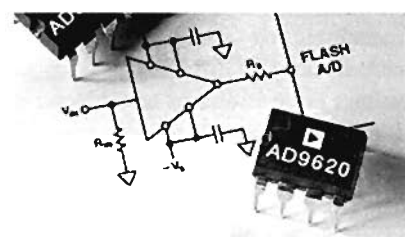
Distortion remains low for all rated load conditions: 2nd harmonic is –84 dBc min (–91 dBc typical) at 2.3 MHz, –67 (–73) dBc at 20 MHz, and –60 (–69) dBc at 60 MHz; and 3rd harmonic is only –72 (–81) dBc at 20 MHz

Two grades of the AD9620 are available with identical specifications; the A and S grades differ only in operating temperature range, A: –40°C to +85°C and S: –55°C to +125°C. Both grades are available in side-brazed ceramic DIP packages. The devices are also available in chip form. Prices (AD/SD) are $19/$29 (100s). ▶

Four-Channel 12-Bit A/D Converter
Samples all four channels simultaneously
Complete-on-chip: reference, mux, clock, ADC

The AD7874* is a complete four-channel sampling a/d converter, including four track/holds, multiplexer, 3-V reference, 12-bit ADC, and control logic. It can capture four input signals simultaneously, then perform four 8-μs, 12-bit conversions at a 29-kHz throughput rate for the sequence.

Unlike devices with a single track/hold, the AD7874's ability to sample simultaneously, with 4-ns max aperture-delay mismatch, means that the relative phase of the signals applied to the four channels is preserved (0.02° at 14.5 kHz). This is especially useful in observing aspects of one-shot phenomena, as well as in motor controllers, sonar, adaptive filters, and digital signal-processing applications in general.

The AD7874 has excellent ac specs. For example, at 29 ksps, a 10-kHz sine wave will have 71-dB minimum signal-to-noise ratio (SNR), with −80-dB max total har-monic distortion and peak spurs. Second- and third-order intermodulation distortion and worst-case channel-to-channel isolation errors are also −80-dB max.

Differential nonlinearity is ±1 LSB max, and relative accuracy error is ±1/2 LSB max for the B grade, ±1 LSB for the other grades. Acquisition time is 2 μs max to 0.01%, and droop rate (A & B versions) is 1 mV/ms max. −3-dB small-signal band-width for the track/holds is 500 kHz.

Available grades are A, B (−40 to +85°C), and S (−55 to +125°C); packages include plastic and hermetic DIPs and SOICs. Prices begin at $28 (100s). ▶

Quad 8-Bit DAC
Complete DAC-8426 has
10-V bandgap reference

The DAC-8426* is a monolithic 4-channel 8-bit parallel-input digital-to-analog con-verter, complete with 10-volt reference, latches, and four independent voltage-output DACs with output buffer amplifiers. It is in essence an upgraded, pin-compatible AD7226* quad multiplying DAC (*Analog Dialogue* 17-2, pp. 3-5) *with an internal reference*. It can operate from a single +15-volt supply, drawing only 210 mW.

The two performance grades have *total un-adjusted error* (TUE) over the operating temperature range of ±1 LSB (A,E) and ±2 LSB (B,F), *including the reference*. Temperature ranges are −55°C to +125°C for Grades A and B, and −40°C to +85°C for E and F.

These complete, ready-to-go devices save time and money in ATE, microprocessor-compatible circuitry, plug-compatible instrumentation for PCs, portable instru-ments, medical equipment, and other data-acquisition & control systems.

The 10-volt reference terminal is available with enough spare current to provide refer-ences for two additional PM7226As, making possible the 12-channel DAC system below.

Separate analog and digital grounds permit virtual-ground biasing in single-supply applications. The DAC-8426 accepts 8-bit parallel TTL or 5-volt CMOS inputs; its fast 50-ns Write time minimizes or eliminates Wait states with high-speed microprocessors.

Now available in 20-pin plastic DIP and cerdip packages, the DAC-8426 will soon be available in an SOL-20 surface-mount pack-age; a MIL-STD-883 version will also be available. Prices (100s) start at $14.50. ▶
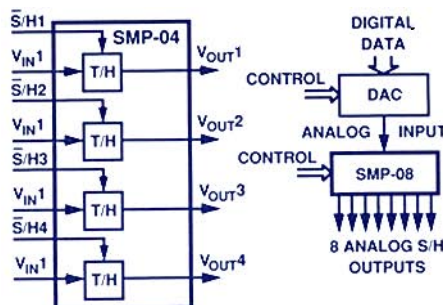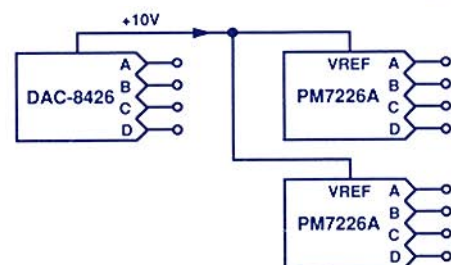
IC Multiple Track- & Sample-Holds
SMP-04 has 4 complete, independent T/H channels
SMP-08 has 8 multiplexed sample-hold channels

The SMP-04* quad low-cost, easy-to-use track-hold and the SMP-08* octal sample-hold, with multiplexed input, eliminate multiple packages. Both devices are com-plete and ready to go, with internal hold capacitors and 16-pin SO, plastic or epoxy DIP, and cerdip packaging—and are avail-able for both military (−55 to +125°C) and extended industrial (−40 to +85°C) temperatures.

The SMP-04 is useful wherever a number of independent signals require sampling, setting, or distribution; examples include automatic test equipment, engine controls, servo systems, and instrumentation. The SMP-08 efficiently distributes eight inde-pendent voltages from a single external d/a converter, saving cost and board space in multiple pin driving for ATE, in process control and robotics, and instrumentation.

The SMP-04 has typical acquisition time of 7 μs and droop rate of 2 mV/s, with a max-imum Hold step of 4 mV. It dissipates only 84 mW max and operates from a +5 to +12-volt single supply or ±7-V dual sup-plies. Pricing starts at $3.90 (100s).

The SMP-08 interfaces easily to micropro-cessors and will provide from 1 to 8 sampled outputs from a single-channel DAC's out-put. Typical specifications include 7-μs ac-quisition time, 2-mV/s droop rate, and a 2-mV hold step. Operation is from a +5 to +12-volt single supply or ±5 to ±7-volt dual supplies. Prices start at $6.25 in 100s (less than $1 per channel). ▶

12-Channel Voltage-Output System Using DAC-8426's 10-Volt Reference

*Use the reply card for technical data.

16-Bit Σ-Δ ADC
AD7701: 0.0015% nonlin.
Serial interface, auto-cal
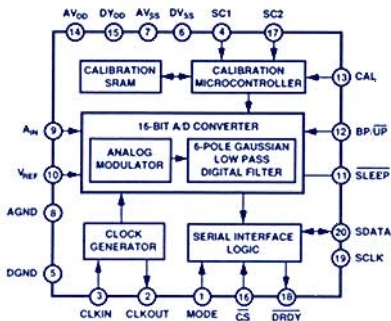
The AD7701* is a serial-output, low-dissipation monolithic CMOS 16-bit a/d converter in a 20-pin DIP. Employing sigma-delta conversion (see *Analog Dialogue* 24-2, pp. 6-7), it is designed for use in applications requiring precision low-frequency measurements. The on-chip digital filter's cutoff frequency can be varied up to 10 Hz —ideal for weigh scales and measurement of slowly varying parameters such as temperature and pressure in process controllers; the AD7701 also replaces the CS-5501.

The AD7701 performs 16-bit conversions over the entire temperature range (-40 to $+85°C$—A,B and -55 to $+125°C$—S,T) with 0.0015% maximum linearity error (B,T) and no missing codes. The device has on-chip self-calibration, which can be extended for external system elements, to remove offset and gain errors in the input channel. The output is available via a flexible synchronous/asynchronous interface, for connection to UARTs or serial ports of industry-standard microcontrollers.

The AD7701 has low dissipation: 40 mW max in normal operation—and 20 μW max (A, B) in a standby "sleep" mode, useful in portable and remote battery-powered instrumentation. An on-chip 6-pole Gaussian digital filter reduces normal-mode and quantization noise, with corner frequency proportional to the chip's clock—e.g., 10 Hz at 4 MHz and 5 Hz at 2 MHz (with 55 and >90-dB respective attenuation at 60 Hz). With a 4.096-MHz clock, the output sample rate is 4 kHz. The analog input range is 0 to $+2.5$ V or ±2.5 V. All grades are available in cerdip, A,B are also in SO and plastic DIPs. Price is from $15 (100s).

*Use the reply card for technical data.

100-kSPS 14-Bit Sampling ADCs
have ac/dc specs; AD779 interfaces to 16-bit bus;
AD679, for 8-bit bus, is 14-bit upgrade for AD678

The AD679* and AD779* are 14-bit monolithic sampling a/d converters capable of sampling at rates up to 100 ksps. Each is complete with sample/hold, reference, and clock; both use a subranging flash design. With identical performance specs, they differ only in their interface: the AD779 has a broadside 14-bit output; the AD679 interfaces with 8-bit buses in 2 bytes.

The 14-bit AD679 has the same architecture and pinout as the 12-bit AD678* (Analog Dialogue 24-2, p. 19), but it converts in 10 μs (vs. 5 μs); this permits a user to optimize a given application for speed or accuracy while retaining the same pinout and interface.

Specified for both ac and dc performance, both devices have 500-kHz minimum full-linear bandwidth, 1-MHz full-power bandwidth, 0.008% max harmonic distortion over temperature, and -84 dB max peak
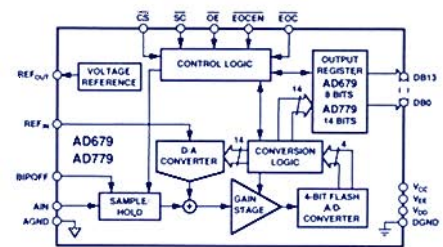
spurious noise. K/B/T grades have 80-dB minimum signal to noise-plus-distortion (10.009 kHz, sampled at 100 ksps).

DC specs (K,B,T) include ±2-LSB max integral nonlinearity and 14-bit no-missing-codes over temperature. Aperture delay is 10 ns, with jitter of 150 ps.

Both the AD679 and AD779 are available in two performance grades for each temperature range, J/K for 0 to $+70°C$, A/B for -40 to $+85°C$, and S/T for -55 to $+125°C$. Prices start at $29.70 in 100s.

+5-V-Supply ADC Has Idle Mode
12-bit monolithic AD7880 features ac & dc specs
57-ns max data access time serves μPs and DSPs

The AD7880* is a 12-bit monolithic 66-ksps sampling analog-to-digital converter capable of operating from a +5-V (±5%) supply. A powerdown (idle) mode reduces dissipation from 50 mW max to 5 mW max at any temperature in the operating range, and from 37.5 mW max to 3.75 mW max at +25°C.

With its single supply, low dissipation, comprehensive ac and dc specifications, 15-μs conversions, and rapid bus access time, the AD7880 is attractive for any application that requires a combination of excellent performance and low power. Examples include battery-powered portable systems, DSP, speech recognition, modems, and any application with constraints on power availability.

The AD7880 can convert signals with 5-volt, 10-volt, and ±5-volt ranges, using a single +5-volt supply. It is a *ratiometric* converter, using an external fixed or variable reference in the range from VDD to +2.5 volts; it can, for example, use the +5-volt
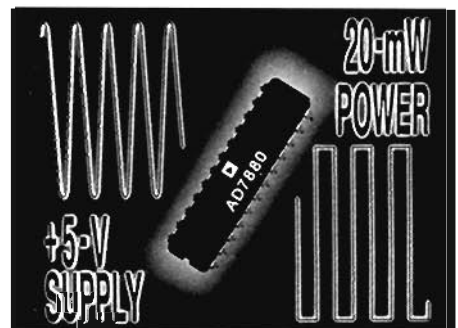
VDD supply as a reference.

For all versions, ac specifications include 70-dB min SNR, and -80-dB typical total-harmonic & intermodulation distortion, and peak spurs. DC errors include ±1-LSB max integral and differential nonlinearity. C versions have ±5-LSB max full-scale error, bipolar zero error, and unipolar offset error.

Two grades are available (B,C) for the -40 to $+85°C$ temperature range in 24-lead "skinny" plastic and cerdip and 24-lead SOIC. Pricing starts at $14 (100s).

Serial I/O Port Has 12-Bit DAC & ADC

For modems, control, DSP interfacing
AD7868 has independent Vout DAC, 83-ksps ADC

The AD7868* is a complete 12-bit analog input-output system consisting of a voltage-output d/a converter and a sampling a/d converter—with references—interfacing independently and either synchronously or asynchronously—with no extra glue logic—to a μP's serial data Transmit (DAC) and Receive (ADC) lines. Standard control signals allow serial interfacing to most DSP machines. Typical applications with digital signal processors are in speech recognition and synthesis, spectrum analysis, servo control, and high-speed modems.
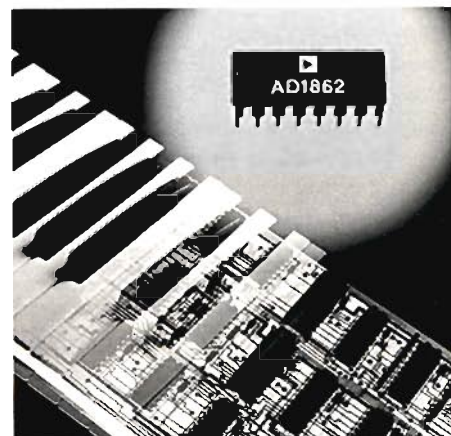
The 12-bit a/d converter, with its input track/hold amplifier, has an 83-kHz throughput rate with 71-dB signal to noise-plus-distortion—SNR—minimum over temperature (B grade), for a 10-kHz sine-wave input (typically 71.5 dB for sine waves from 0 to 41.5 kHz).

The 12-bit d/a converter has 3-μs max settling time to within 1/2-LSB of final voltage, operating at an 83-kHz update rate —
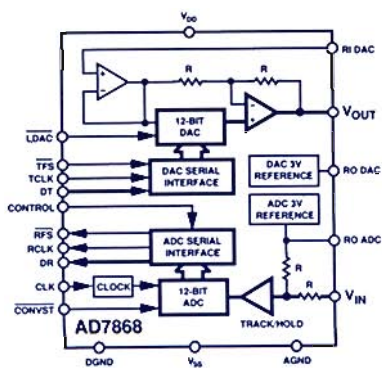
with 71-dB min SNR over temperature for a 1-kHz sine wave (B grade), and typically 71.5 dB for sine waves from 0 to 20 kHz (external deglitching sample/hold).

The AD7868 has complete specs for both dc and ac parameters. Three performance grades are available: A and B for −40 to +85°C operation—and T for −55 to +125°C. The AD7868 is available in 0.3"-wide plastic and ceramic 24-pin DIPS and in a 28-pin SOIC package. Price starts at $24 (100s). ▶

High-Accuracy, High-Speed M-DAC
## 12-bit AD668 has 1/4-LSB linearity error
FS Settling to 1 LSB in 90 ns (I) and 120 ns (V)

The 12-bit AD668* is a 2-quadrant multiplying DAC combining high accuracy and high-speed in a 0.3" skinny DIP package. A multiplying version of the AD568* (*Analog Dialogue* 21-2, 1987, p. 8), it combines current- and voltage settling times of 90 and 110 ns with linearity error of 1/4 LSB (K grade). Monotonicity is guaranteed over the full operating temperature range.

Applications include SAR- and subranging-type a/d converters; its high-speed multiplying capability makes it ideal for waveform-generation and digital attenuation. It will find applications in test equipment, medical instruments, waveform analyzers, r-f modems, data transmission, and high-speed data acquisition.

It accepts variable reference inputs, with a bandwidth of 15 MHz (10-MHz large-signal); its reference input can be pin-

*Use the reply card for technical data.
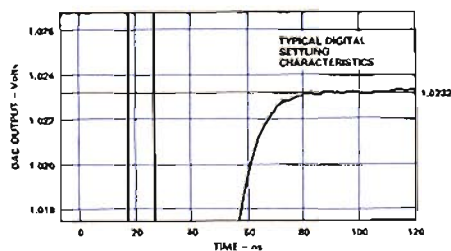
strapped for 1, 1.25, and 5 volts full-scale. FS current output is 10.24 mA, and an on-chip 200-Ω load resistor can be pin-strapped to choose a ±5.12-mA bipolar current range and these voltage ranges: 0 to +1.024 V, ±0.512 V, & ±1.024 V. With the addition of an external amplifier, like the AD840*, buffered output ranges of 0 to −10.24 V and ±5.12 V are also possible.

Three grades are available, J & K for 0 to +70°C, and S for −55 to +125°C; devices qualified to /883B are also available. Prices start at $33 (100s). ▶

20-Bit Audio DAC
119-dB signal-to-noise
−98-dB THD + noise

The AD1862* is the industry's first monolithic 20-bit d/a converter designed specifically for high-performance digital audio applications, such as electronic musical instruments, CD players, and digital audio signal processing systems. Packaged in a 16-pin plastic DIP, it operates from ±12-volt supplies, typically dissipates less than 288 mW, and easily interfaces to popular digital filters.

Measured according to EIAJ standards (CP-307), the AD1862 achieves 119-dB signal-to-noise (113-dB min), −96-dB (0.0016%) total-harmonic-distortion-plus-noise (THD+N), and a minimum 102-dB D-range (an EIAJ distortion spec). Gain linearity is within ±1 dB at −90-dB amplitude.

Proprietary digital offset circuitry is used to enhance signal linearity at low levels and eliminate the need for deglitching circuitry. An external midscale trim-pin permits optimization of distortion performance for small-signal (<60 dB) amplitudes. Low-stress packaging minimizes stress-induced parametric shifts.

Fabricated on a high-density BiMOS process, the AD1862 integrates CMOS logic, MOS and bipolar linear devices, and laser-trimmed thin-film-resistor networks. It is specified for operation from −25 to +70°C and 100% tested and graded for THD+N and SNR. The AD1862N guarantees maximum THD+N of 0.0025% and minimum 110-dB SNR; the AD1862N-J guarantees 0.0016% THD+N and 113-dB SNR. Pricing in 100s begins at $17.20. ▶

Ask the Applications Engineer—8
by James Bryant

OP-AMP ISSUES
(Noise, continued from the last issue, 24-2)

Q: What is "noise gain"?

A. So far we have considered noise sources but not the gain of the circuits where they occur. It is tempting to imagine that if the noise voltage at the input of an amplifier is V_n and the circuit's signal gain is G, the noise voltage at the output will be GV_n; but this is not always the case.

Consider the basic op-amp gain circuit in the diagram. If it is being used as an inverting amplifier (B), the non-inverting input will be grounded, the signal will be applied to the free end of R_i and the gain will be $-R_f/R_i$. On the other hand, in a non-inverting amplifier (A) the signal is applied to the non-inverting input and the free end of R_i is grounded; the gain is $(1 + R_f/R_i)$.
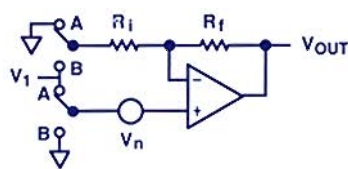
	SIGNAL GAIN	AMPLIFIER NOISE GAIN
A:	$\left(1 + \frac{R_f}{R_i}\right)$	$\left(1 + \frac{R_f}{R_i}\right)$
B:	$-\frac{R_f}{R_i}$	$\left(1 + \frac{R_f}{R_i}\right)$

The amplifier's own voltage noise is always amplified in the non-inverting mode; thus when an op-amp is used as an inverting amplifier at a gain of G, its voltage noise will be amplified by the noise gain of $(G+1)$. For the precision attenuation cases, where $G<1$, this may present problems. (A common example of this is an active filter circuit where stop-band gain may be very small but stop-band noise gain is at least unity.)

Only the amplifier voltage noise—and any noise developed by the noninverting-input current noise flowing in any impedance present in that input (for example, a bias-current compensation resistor)—is amplified by the noise gain. Noise in R_i, either Johnson noise or arising from inverting input noise current, is amplified by G in the same way as the input signal, and Johnson noise voltage in the feedback resistor is not amplified but is buffered to the output at unity gain.

Q: What's "popcorn" noise?

A: Twenty years ago this column would have spent a great deal of space discussing popcorn noise, which is a type of low frequency noise manifesting itself as low level (but random amplitude) step changes in offset voltage occurring at random intervals. When played through a loudspeaker it sounds like cooking popcorn —hence the name.

While no integrated circuit process is entirely free from the problem, high levels of popcorn noise result from inadequate processing techniques. Today its causes are sufficiently well understood that no reputable op-amp manufacturer is likely to produce op-amps where popcorn noise is a major concern to the user. [Oat-bran noise is more likely to be an issue in situations where cereal data is concerned.]

Q. Pk-pk noise voltage is the most convenient way to know whether noise will ever be a problem for me. Why are amplifier manufacturers reluctant to specify noise in this way?

A. Because noise is generally Gaussian, as we pointed out in the last issue. For a Gaussian distribution it is meaningless to speak of a maximum value of noise: if you wait long enough any value will, in theory, be exceeded. Instead it is more practical to speak of the rms noise, which is more or less invariant—and by applying the Gaussian curve to this we may predict the probability of the noise exceeding any particular value. Given a noise source of V rms, since the probability of any particular value of noise voltage follows a Gaussian distribution, the noise voltage will exceed a pk-pk value of 2 V for 32% of the time, 3 V for 13% of the time, and so on:

Pk-pk value	% of time pk-pk value is exceeded
$2 \times$ rms	32%
$4 \times$ rms	4.6%
$6 \times$ rms	0.27%
$6.6 \times$ rms	0.10%
$8 \times$ rms	60 ppm
$10 \times$ rms	0.6 ppm
$12 \times$ rms	2×10^{-9} ppm
$14 \times$ rms	2.6×10^{-12} ppm

So if we define a peak value in terms of the probability of its occurrence, we may use a peak specification—but it is more desirable to use the rms value, which is generally easier to measure. When a peak noise voltage is specified, it is frequently 6.6 × rms, which occurs no more than 0.1% of the time.

Q. How do you measure the rms value of low-frequency noise in the usually specified band, 0.1 to 10 Hz? It must take a long time to integrate. Isn't this expensive in production?

A. Yes, it is expensive, but— Although it's necessary to make many careful measurements during characterization, and at intervals thereafter, we cannot afford the time it would take in production to make an rms measurement. Instead, at very low frequencies in the 1/f region (as low as 0.1 to 10 Hz), the peak value is measured during from one to three 30-second intervals and must be less than some specified value. Theoretically this is unsatisfactory, since some good devices will be rejected and some noisy ones escape detection, but in practice it is the best test possible within a practicable test time and is acceptable if a suitable threshold limit is chosen. With conservative weightings applied, this is a reliable test of noise. Devices that do not meet the arbitrary criteria for the highest grades can still be sold in grades for which they meet the spec.

Q. What other op-amp noise effects do you encounter?

A. There is a common effect, which often appears to be caused by a noisy op amp, resulting in missing codes. This potentially serious problem is caused by ADC input-impedance modulation. Here's how it happens:

Many successive-approximation ADCs have an input impedance which is modulated by the device's conversion clock. If such an ADC is driven by a precision op amp whose bandwidth is much lower than the clock frequency, the op amp cannot develop sufficient feedback to provide a stiff voltage

source to the ADC input port, and missing codes are likely to occur. Typically, this effect appears when amplifiers like the OP-07 are used to drive AD574s.

It may be cured by using an op amp with sufficient bandwidth to have a low output impedance at the ADC's clock frequency, or by choosing an ADC containing an input buffer or one whose input impedance is not modulated by its internal clock (many sampling ADCs are free of this problem). In cases where the op amp can drive a capacitive load without instability, and the reduction of system bandwidth is unimportant, a shunt capacitor decoupling the ADC input may be sufficient to effect a cure.

Q. Are there any other interesting noise phenomena in high-precision analog circuits?

A. The tendency of high-precision circuitry to drift with time is a noise-like phenomenon (in fact, it might be argued that, at a minimum, it is identical to the lower end of $1/f$ noise). When we specify long-term stability, we normally do so in terms of $\mu V/1,000$ hr or ppm/1,000 hr. Many users assume that, since there are, on the average, 8,766 hours in a year, an instability of $x/1,000$ hr is equal to 8.8 x/yr.

This is not the case. Long-term instability (assuming no long-term steady deterioration of some damaged component within the device), is a "drunkard's walk" function; what a device did during its last 1,000 hours is no guide to its behavior during the next thousand. The long-term error mounts as the square-root of the elapsed time, which implies that, for a figure of $x/1,000$ hr, the drift will actually be multiplied by $\sqrt{8.766}$, or about 3× per year, or 9× per 10 years. Perhaps the spec should be in $\mu V/1,000 \sqrt{hr}$.

In fact, for many devices, things are a bit better even than this. The "drunkard's walk" model, as noted above, assumes that the properties of the device don't change. In fact, as the device gets older, the stresses of manufacture tend to diminish and the device becomes more stable (except for incipient failure sources). While this is hard to quantify, it is safe to say that—provided that a device is operated in a low-stress environment—its rate of long-term drift will tend to reduce during its lifetime. The limiting value is probably the $1/f$ noise, which builds up as the *square-root of the natural logarithm* of the ratio, i.e., $\sqrt{\ln 8.8}$ for time ratios of 8.8, or 1.47 x for 1 year, 2.94 x for 8.8 years, 4.4 x for 77 years, etc.

A READER'S CHALLENGE:

Q. A reader sent us a letter that is just a wee bit too long to quote directly, so we'll summarize it here. He was responding to the mention in these columns (*Analog Dialogue* 24-2, pp. 20-21) of the shot effect, or Schottky noise (Schottky was the first to note and correctly interpret shot effect—originally in vacuum tubes[1]). Our reader particularly objected to the designation of shot noise as solely a junction phenomenon, and commented that we have joined the rest of the semiconductor and op-amp engineering fraternity in disseminating misinformation.

In particular, he pointed out that the shot noise formula—

$$I_n = \sqrt{2q\,IB} \text{ amperes,}$$

where I_n is the rms shot-noise current, I is the current flowing through a region, q is the charge of an electron, and B is the bandwidth—does not seem to contain any terms that depend on the physical properties of the region. Hence (he goes on) shot noise is a *universal* phenomenon associated with the fact that any current, I, is a flow of electrons or holes, which carry discrete charges, and the noise given in the formula is just an expression of the graininess of the flow.

He concludes that the omission of this noise component in any circuit carrying current, including purely resistive circuits, can lead to serious design problems. And he illustrates its significance by pointing out that this noise current, calculated from the flow of dc through any ideal resistor, becomes equal to the thermal Johnson noise current at room temperature when only 52 mV is applied to the resistor—and it would become the dominant current noise source for applied voltages higher than about 200 mV.

A. Since designers of low-noise op amps have blithely ignored this putative phenomenon, what's wrong? *The assumption that the above shot noise equation is valid for conductors.*

Actually, the shot noise equation is developed under the assumption that the carriers are independent of one another. While this is indeed the case for currents made up of discrete charges crossing a barrier, as in a junction diode (or a vacuum tube), it is not true for metallic conductors. Currents in conductors are made up of very much larger numbers of carriers (individually flowing much more slowly), and the noise associated with the flow of current is accordingly very much smaller—and generally lost in the circuit's Johnson noise.

Here's what Horowitz and Hill[2] have to say on the subject:

"An electric current is the flow of discrete electric charges, not a smooth fluidlike flow. The finiteness of the charge quantum results in statistical fluctuations of the current. *If the charges act independently of each other,** the fluctuating current is . . .

$$I \text{ noise (rms)} = I_{nR} = (2\,qI_{dc}\,B)^{1/2}$$

where q is the electron charge (1.60×10^{-19} C) and B is the measurement bandwidth. For example, a "steady" current of 1 A actually has an rms fluctuation of 57 nA, measured in a 10-kHz bandwidth; i.e., it fluctuates by about 0.000006%. The relative fluctuations are larger for smaller currents: A "steady" current of 1 μA actually has an rms current-noise fluctuation, over 10 kHz, of 0.006%, i.e., -85 dB. At 1 pA dc, the rms current fluctuation (same bandwidth) is 56 fA, i.e., a 5.6% variation! Shot noise is 'rain on a tin roof.' This noise, like resistor Johnson noise, is Gaussian and white.

"The shot noise formula given earlier assumes that the charge carriers making up the current act independently. That is indeed the case for charges crossing a barrier, as for example the current in a junction diode, where the charges move by diffusion; *but it is not true for the important case of metallic conductors, where there are long-range correlations between charge carriers. Thus the current in a simple resistive circuit has far less noise than is predicted by the shot noise formula.** Another important exception to the shot-noise formula is provided by our standard transistor current-source circuit, in which negative feedback acts to quiet the shot noise."

*Italics ours
[1]Goldman, Stanford, *Frequency Analysis, Modulation, and Noise.* New York: McGraw-Hill Book Company, 1948, p. 352.
[2]Horowitz, Paul and Winfield Hill, *The Art of Electronics,* 2nd edition. Cambridge (UK): Cambridge University Press, 1989, pp. 431-2. ▶

Worth Reading

FREE DATABOOKS*

ANALOG DEVICES LINEAR PRODUCTS DATABOOK
1990/91. 18 product categories, more than 1,200 pages.

PMI ANALOG INTEGRATED CIRCUITS DATABOOK
(Vol. 10). 14 product categories, more than 1,800 pages.

PMI SSM AUDIO PRODUCTS: AUDIO HANDBOOK.
Includes 26 data sheets and 19 application notes, 224 pages.

FREE DSP APPLICATIONS HANDBOOK*

ADSP-2100 FAMILY APPLICATIONS HANDBOOK, Volume 4: Data Communications. Includes V.32 modems (scrambling/descrambling, differential and convolutional encoding, Viterbi decoding); Quadrature amplitude modulation (QAM); Echo cancellation; Adaptive equalization; and Continuous-phase frequency-shift Keyed (CPFSK) modulation. Disk also available. For source code, call the DSP Bulletin Board, (617) 461-4258.

SELECTION CHARTS & DESIGNERS GUIDES

Resolver-to-Digital Converter (RDC) Selection Chart* — Single speed and multispeed resolvers, Resolver parameters, Analog Devices RDCs and resolver accuracy charts, Resolver charts for 8 manufacturers, Definition and terminology, etc., 38 pp.

Mixed-Signal ASIC Designer's Guide. Mixed-signal BiCMOS processes, Precision linear and converter functions, CMOS logic for control and DSP, Comprehensive cell libraries, Analog & digital systems on a chip. 16 pp. Write on letterhead for a copy.

Passive-component selection guide for the 2S80 resolver-to-digital converter*. Free diskette and 12-page application note, covering passive component selection; transfer-function computation/display; and step response.

FREE BROCHURES*

MOTION-CONTROL PRODUCTS — Innovations in real-world signal processing. A new generation of synchro/resolver conversion products. 6 pp.

FREE SERIAL PUBLICATIONS*

DSPatch — The DSP Applications Newsletter:
Number 17, Fall, 1990. Features: New floating-point DSP simulator; A new sigma-delta CODEC; Digital filtering of nuclear fusion data; Recording the California earthquake in the USSR; and Real-time software tools for the Logabex DX2100 board. Also: Q & A, How to talk analog (part 4 on Σ-Δ conversion); logic analyzers for ADSP-2100 & ADSP-2101; RMS calculation for power instrumentation; book review of Franklin, Powell, & Workman: *Digital Control of Dynamic Systems*, and much more.

Number 16, Summer, 1990. AEG Olympia's videophone, "Mike" multifunction ISDN communications terminal, ADSP-2100 C compiler, Image enhancement in Kodak's XL7700 digital continuous tone printer; Loughboro's ADSP-2101 system board; the AD766 as a companion DAC for the ADSP-2101. Plus the usual features: Q & A; How to talk analog (part 3 of Σ-Δ conversion); University of Padua's digit reversing routine; and much more.

REPRINTS AVAILABLE*

A DSP system on a chip, by Frank Goodenough, *Electronic Design*, April 12, 1990. "Breaking new ground, one chip can now perform real-world analog signal processing with digital resolu-

*Available free upon request.

tion, dynamic range, and accuracy." An analog-oriented editor's view of the ADSP-21msp50 mixed-signal processor.

18 bits on a budget, *CD Review*, March, 1990. Describing the AD1860 18-bit audio DAC.

ICs simplify LVDT interface, by John Sylvan, *Machine Design*, January 25, 1990. The AD598 LVDT conditioner.

Mixed-Signal ASICS. Five papers presented at the 1990 IEEE Custom Integrated Circuits Conference. Technologies and designs. 28 pp.

Off the shelf pin electronics — commercial devices fill high-speed ATE needs, *Electronics Test*, January, 1990. Describing the AD1315, AD1321/22 active load and pin drivers.

APPLICATION NOTES*

An improved T1 (1.544 MBit/s) PCM repeater design extends dynamic range from 0 dB to beyond −44 dB, by James Wong. Applying the RPT-86/87 Low-Power PCM Repeaters. With only a few external components, the RPT-86/87 perform as a complete PCM serial-data regenerative repeater. 4 pp., AN-140.

Considerations for selecting a DSP processor — ADSP-2101 vs. WE DSP16A, by Bruce Wolfeld. Compares these two approaches to 16-bit fixed-point DSP in terms of arithmetic capabilities, data addressing, program sequencing, and connection to other devices. Compares implementation of the stochastic gradient algorithm for updating taps in an adaptive filter on the two devices. 12 pp.

Simple circuit provides ratiometric reference levels for AD7820/21/24/28 family of half-flash ADCs, by John Wynne. The AD782X family lends itself very easily to conversion of input signal spans that do not include 0 volts. A very simple circuit generates ratiometric $V_{REF(+)}$ and $V_{REF(-)}$ reference levels from a standard ground-based reference voltage. 4 pp.

Using multiple AD1334 4-channel, 12-bit sampling ADCs in many-channel synchronous sampling, by Stephan Goldstein. Maintaining phase coherency across all input channels. 2 pp.

Voltage adjustment applications of the DAC-8800 TRIMDAC™, an octuple 8-bit D/A converter, by Joe Buxton. Architecture, reference considerations, ac multiplying mode, single +5-V supply operation, two-wire interfaces for process environments, stand-alone operation providing nonvolatile settings, test fixture, conditions to avoid, applications in: digitally controlled VCA, trimming op-amp offset voltage, trimming voltage references, coarse-fine control, and as an adjustable reference for ADCs. 16 pp., AN-142.

AUTHORS

James Bryant (page 24) is European Applications Manager for ADI, based in Newbury, England. A graduate of the University of Leeds, he earned a B.Sc. in Physics and Philosophy. He has 19 years of applications experience, both at Plessey and ADI. James has numerous publications on a wide range of topics and served as a technical advisor to Parliament on CB radio. His diverse interests include amateur radio (G4CLF), collecting science fiction (>3 k volumes), hypnotism, and parapsychology.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS—NEWLY ANNOUNCED PRODUCTS: . . . AD1317* Ultra-High-Speed Window Comparator with Latch for automatic testing of ICs is a companion to the AD1321* and AD1322* Pin Drivers and the AD1315* Active Load (*Analog Dialogue* 23-4 cover story) . . . AD9014* 14-bit, 10-MSPS ADC with 90-dB SFDR (min) . . . AD9058* Dual 8-bit, 50-MSPS ADC draws only 0.5 W per channel . . . ADSP-2102* and ADSP-2106* are monolithic DSP microcomputers which allow designers to *freely define program memory as segments of RAM and mask-programmable ROM*; otherwise they are identical to the ADSP-2101* and ADSP-2105* µCs . . . AD1674*, a low-cost 100-ksps (10-µs) single-chip *sampling* ADC is a "better, faster, cheaper" pin-compatible replacement for the AD574A and AD674A . . . For non-sampling applications, the 15-µs single-chip faster-access AD674B* replaces the AD674A and AD574A—and it's available in plastic! . . . AD1851* and AD1861* 16- and 18-bit audio DACs are higher-speed, lower-noise ±5-V only upgrades for the AD1856 and AD1860 . . . AD7242* and AD7244* are dual 12- and 14-bit serial-input, voltage-output DACs—complete with output amplifiers and reference . . . AD9950* 330-MHz phase accumulator drives a ROM and DAC to implement high-frequency functions for direct digital synthesis (DDS) . . . AD2S34* is a 14-bit two-channel tracking resolver-to-digital converter with built-in power oscillator circuit . . . AD2S46* is a low-cost hybrid 16-bit RDC in a 28-pin DIP with 1.3 arc-minute accuracy . . . AD1382* is a 16-bit, 500-ksps sampling ADC in a single package with guaranteed dynamic performance . . . AD1378* is a 16-bit hybrid ADC with reference & clock designed for MIL-temp applications. It uses the industry-standard AD1376 pinout . . . AD7837* and AD7847* are complete 4-quadrant 12-bit dual multiplying DACs with output amplifiers . . . AD704 is a quad low-drift, low-bias-current op amp,* based on the AD706 dual (see page 19).

ERRATA . . . AD9620 data sheet . p. 5, Small-signal pulse response diagram: 50-Ω resistor to ground should be at output end (i.e., in parallel with the 6-pF capacitor) . . . There are a number of errors in the AD9020 and AD9060 data sheets; revised versions* are now available . . . *Analog Dialogue*: 22-2, page 12, Table 1—slew rates should be in V/µs (not µV/s!); 24-2, page 13, Figure 6—chroma I and Q signals are interchanged . . . AD9696/AD9698 data sheet, page 4, mechanical dimensions: lead-width dimensions for AD9698KN and AD9696KN, 0.045 0.70 should read 0.045 0.070; millimeter values shown are correct . . . In the 1987 and 1989 Military Databooks, the AD7578 is indicated as available in the D24 (0.6") package; the correct package designation is D24A (0.3"). The Conversion Products Databook does not have these errors . . . The AD386's input logic threshold voltages are incorrect in the AD386 data sheet, the Data Conversion Products Databook 1989/90, and the 1990 Military Products Databook—they should be $V_{ih} = 3.5$ V min; $V_{il} = 0.9$ V max . . . An Errata sheet is available† for Models 1B41/1B51; it also introduces new higher-performance "BN" grades.

PRODUCT NOTES . . . Analog Devices and BMW collaborated in developing an *automotive IC (replacing and improving upon a board-level design) to continuously monitor lamps and fuses* and automatically detect the failure of headlamps, fog lights, and other lights, whether *off* or on. A device based on this circuit, the AD22001, is now available on the open market† . . . SPECIFIX, an IBM PC software package from Intellution supports our RTI®-, µMAC- and 6B data-acquisition and process-control hardware† . . . An ICONview version of LABTECH NOTEBOOK allows users to easily build their applications graphically on a "drawing board" with a mouse, using IBM PCs with EGA or VGA graphics) . . . A few minor glitches in current embodiments of ADSP-2101, -2105, and -2111 are described in individual *Anomaly Sheets*. CWYLSO† . . . DSP Applications Assistance Line: (617) 461-3672 (staffed 8 AM-5 PM ET, leave recorded message at other times). Call for information about Version 2.02 of the ADSP-2101 software for the IBM PC . . . DSP Bulletin-Board service (new users validated on Wednesdays): (617) 461-4258—set your modem to 8 data bits, 1 stop bit, no parity, 300/1200/2400 baud . . . The "A" revisions of the 2S80, 2S81, and 2S82 are here, with Class 2 ESD protection and circuit changes to prevent latchup† . . . There are changes in velocity output specs of current embodiments of 1S24/460, 1S44/460, 1S64/460, and 1S74/460. CWYLSO† . . . There's a new data sheet for the AD96685/87 high-speed comparators, *now available in* 20-pin PLCC and 16-lead SOIC.* . . . An Applications Corner brief from James Wong is available (CWYLSO†), "How to achieve 40-MHz video bandwidth using the OP-260" . . . CWYLSO† for information about evaluation boards for sophisticated high-performance ICs, such as AD9020, AD9060, AD9617/18 . . . The ADV476 is available in a 44-pin PLCC. CWYLSO† for a data-sheet addendum with ordering info . . . For information on CONTROL EG support of µMAC-1050 and 6B modules, CWYLSO† . . . The RTI-850 has been replaced by RTI-850-F with a *top conversion rate of 77 kHz, up from 55 kHz* . . . The 4-quadrant, 500-MHz AD834 analog multiplier is now available in plastic at low cost. For industrial and avionics applicatins, the −40 to +85°C AQ version is also available in cerdip . . . A Bitbus-compatible communications controller for the 6B Series is now available from Datem, Ltd., Ontario, Canada. CWYLSO† . . . The AD9901 Phase Detector is now available in a 20-lead PLCC and at a lower price. CWYLSO† . . . An Addendum sheet is available for the AD1315, discussing *output leakage current in Inhibit.* CWYLSO† . . . New and updated op-amp data sheets are now available. Ask for AD707,* AD743,* AD829,* AD842,* AD844,* AD845,* AD846,* AD848/49* . . . RTI-Series DOS Drivers, Rev 2.0, have just been released. CWYLSO† . . . The RTI-827 counter-timer board is now available to plug into IBM PCs. *Measure frequencies, count events, or output pulse trains.*

MILITARY ROLL CALL: . . . Five new Class S listings (Precision Monolithics): PM139SY5 has Jan part no. 11201SCA; DAC08SO5 is 11301SEA; DAC08SAO5 is 11302SEA; OP27SAJ5 is 13503SGA; and OP27SAZ5 is 13503SPA. *There are many others already on the list.* CWYLSO† . . . Our ultrahigh-speed comparators are now available on Standard Military Drawings—8600804 (AD96685) and 7801903 (AD96687) . . . Reliability reports are available for many of our new products. CWYLSO† . . . The AD674A 12-bit fast ADC is now qualified to /883B standards . . . The AD705 and AD645 precision op amps are also qualified to /883B . . . The AD9617/18 high-speed op amps and AD9901 phase detector are now '883-qualified. CWYLSO†.

SEMINARS & SHOWS . . . Our 1990 High-Speed-Design Seminar program was an unqualified success. (If you didn't get to attend, you can still get the 496-page *High-Speed-Design Seminar* Notes for only $20. Use the book purchase card or phone (617) 461-3392 with your Visa number.) Now we're readying some new seminars. Look for publicity on the Mixed-Signal Design Seminar in early 1991 . . . Are you just starting out with DSP? Our DSP Group holds an invaluable hands-on 3-day System Development & Programming (with the ADSP-2100 Family) Workshop at least twice a quarter. For details, call (617) 461-3881 or CWYLSO†; ask about ADDS-2190 . . . Here are a few of our 1991 trade shows. If you're in the neighborhood, come see us: Feb. 19-22—Audio Engineering Society, Paris; February 26-March 2—SAE'91, Cobo Hall, Detroit; May 12-15—CICC'91, Town & Country Hotel, San Diego; May 15-17—ICASSP, Sheraton Centre, Toronto; July 30-August 1—SIGGRAPH'91, Las Vegas.

PATENTS RECEIVED: . . . 4,904,921 by Lawrence DeVito and A. Paul Brokaw for *Monolithic interface circuit for linear variable differential transformers* . . . 4,924,227 by Christopher Mangelsdorf for *Parallel analog-to-digital converter* . . . 4,926,178 by Martin Mallinson for *Delta modulator with integrator having positive feedback* . . . 4,928,103 by Charles Lane for *Parallel analog-to-digital converter using 2^{n-1} comparators* . . . 4,929,909 by Barrie Gilbert for *Differential amplifier with gain compensation* . . . 4,940,980 by Thomas E. Tice for *Input stage for flash A/D converter* . . . 4,957,583 by Roy Buck and Darrell Adams for *Apparatus for etching patterned substrates* . . . 4,962,325 by Gerald Miller and Christopher O'Connor for *Sample-hold amplifier circuit.*

*Use the reply card for technical data.
†CWYLSO = Check with your local sales office

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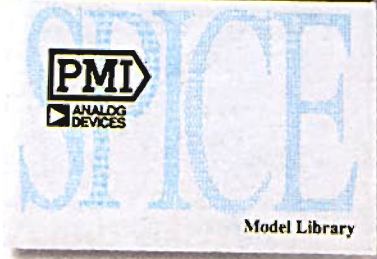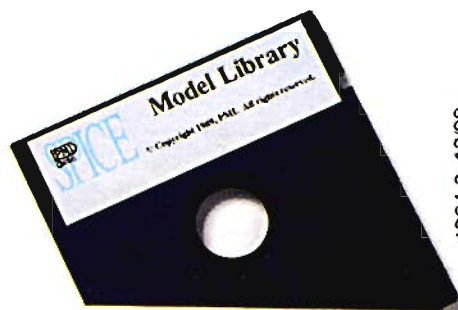
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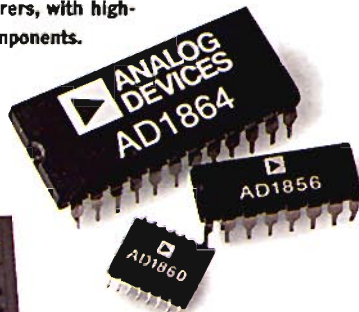
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