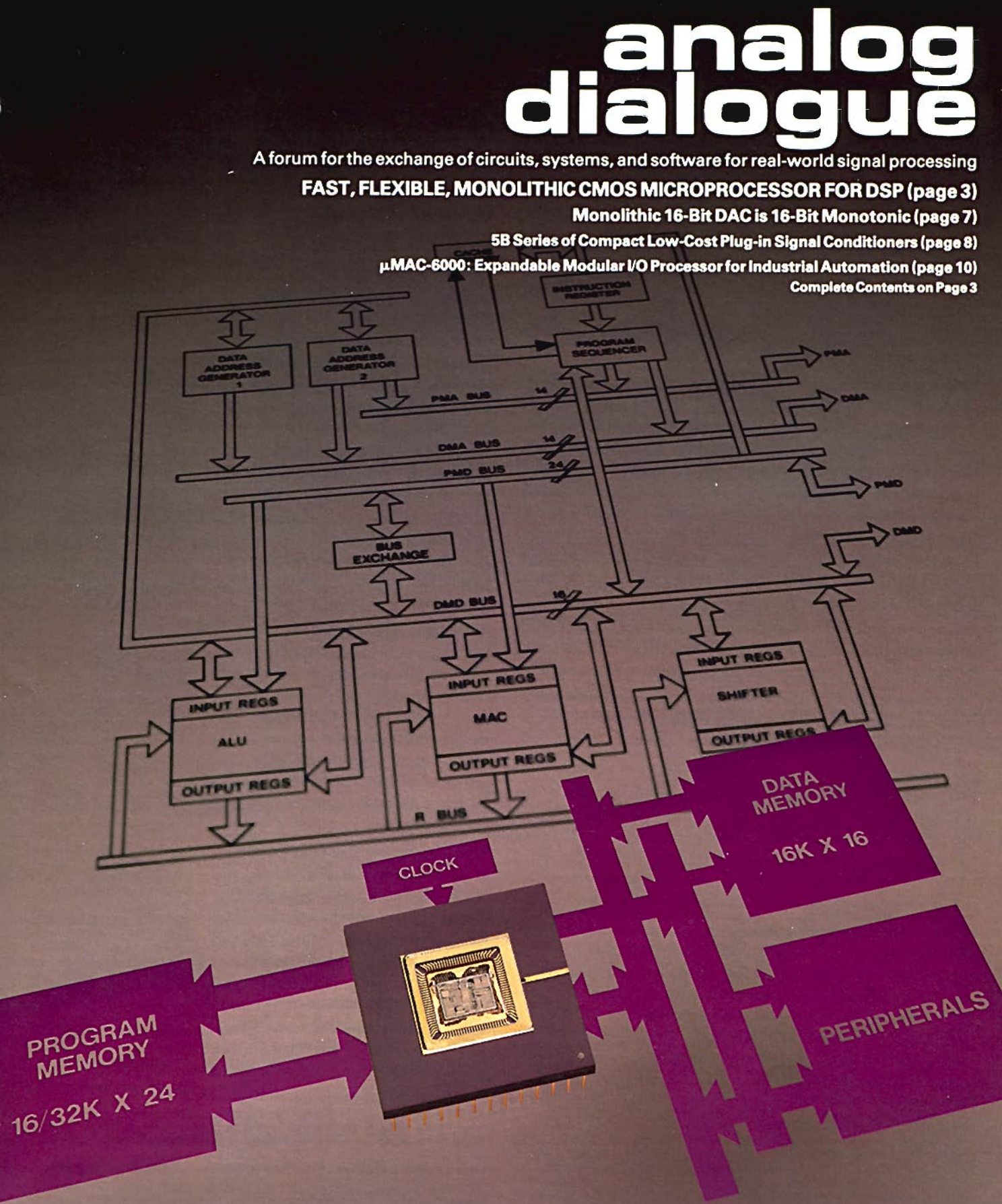
analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 20, Number 2, 1986

ANALOG DEVICES

Editor's Notes

ANALOG & DIGITAL

"Microprocessor?" we hear you ask. "Isn't it a bit unseemly for a nice 'Analog' IC company to be designing a microprocessor? (What could be more digital?)"

Good question.

Our objective has always been to design and manufacture cost-effective components that are key elements of the signal path for processing real-world (i.e., *analog*) data and for which performance is maximized and errors minimized.

The signal path? *Real-world data* almost always starts out as *analog* (i.e., parallel, non-numeric) variables, which are measured by sensors that provide *analog* electrical signals—voltage and current. The signals must be accurately and speedily amplified, conditioned, (almost always in parallel) and converted to digital for processing. Once in digital form, they must be processed rapidly. Often, they again wind up as analog signals.

Key elements of the signal path include preamplifiers, analog signal processors, data converters to and from digital, and—when the signal is in digital form—a digital processor. Inadequacy in any one of the key elements—amplifier, analog processor, data converter, or microprocessor—can cause poor performance of the overall system.

Obstacles in the signal path include noise, drift, nonlinearity, and measurement lag at the analog stages, similar obstacles in conversion—and throughput delays in digital processing, often because of the lack of parallelism in von Neumann architectures.

Throughout our history, our role in the signal path has been to initiate new products (or product lines) when dissatisfied with the cost-effectiveness of what's available (which is often limited to user-assembled kludges, when nothing else is available). At this point in time, we (and our competitors) have virtually eliminated the user-assembled amplifier, signal-conditioner, and data converter by designing and marketing families of cost-effective products.

We have always been dissatisfied with the cost, power dissipation, and slow throughput in the digital domain; this concern led to our pioneering development of CMOS multipliers and other digital signal-processing ICs (note that because we were already familiar with analog multipliers, digital multipliers became just another analog signal-processing tool; note also our commitment to *signal processing*—not payroll, desktop publishing, or order-handling products). Our dissatisfaction with the complexity of systems using Bit-Slice parts led to the powerful and compact Word-Slice™ microcoded system parts.

And finally our dissatisfaction with insufficient throughput in DSP processors led to design of the ADSP-2100, which stresses the use of that *analog* characteristic, parallelism, to minimize instruction cycles, whether in processing, data transfer, or interrupt handling. It's neat! We invite you to read about it. ▶

Dan Sheingold

THE AUTHORS

James Conant (page 14) is a Senior Marketing Engineer in the Interface Products Division of Analog Devices. A biographical sketch and his photo appear in the last issue (20-1, 1986).

Daniel Denaro (page 19) is a Senior Design Engineer for ADI's Memory Device Division, in East Molesey, England. He received a BEE with honors from the University of Queensland (Brisbane, Australia) in 1979. Before joining ADI, he was working on radar detection systems at EMI Electronics; he has been working on hybrid converters since 1983.

Bob Fine (page 3) is the Applications Engineering Manager for ADI's Digital Signal Processing Division. He has been with the DSP division for four years, mostly in applications. Earlier, Bob worked for the Systems Division of ADI, designing both analog and digital circuits. Bob has a BSEE from Northeastern University and has specialized in data-acquisition circuits, analog and digital signal processing.

Amer Iqbal (page 18) is a Marketing Engineer at ADI's Interface Products Division. Before joining Analog Devices, he worked at Qualogy (San Jose, CA), designing DEC-compatible disk- and tape controllers. Amer holds a BSEE degree from MIT and an MBA from Wharton. He enjoys camping, sailing and squash.

Kathryn Kasper (page 8), a Marketing Engineer with ADI's Interface Products Division, has an SM in Management from M.I.T. and a BES in Chemical Engineering from the Johns Hopkins University; she is now working towards an MSEE at Northeastern University. Kathryn joined Analog Devices in 1984 as a Marketing Analyst in Corporate Strategic Information and moved to IPD in 1985.

(Continued on page 26)

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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FAST, FLEXIBLE CMOS SINGLE-CHIP μP FOR DIGITAL SIGNAL PROCESSING

High-Performance ADSP-2100 Has Multiple-Bus Architecture, Parallel Operations
Available Development System Speeds Program Development and Verification

by Mike Nell and Bob Fine

The ADSP-2100* is a single-chip CMOS microprocessor designed specifically for DSP applications and high-performance number crunching. Combined to utilize its 125-ns cycle time efficiently, its multiple-bus structure, substantial external program- and data-memory capacity, powerful instruction set, and independent on-chip computational units—including a multiplier-accumulator/subtractor (MAC), arithmetic-logic unit (ALU), and full-function barrel shifter (for floating-point computations)—deliver performance far exceeding that of earlier single-chip DSP microcomputers. In fact, its performance approaches that of multi-chip (multiwatt!) bit-slice systems, but with power consumption less than 0.6 W. It can perform a 1K-point complex fast Fourier transformation (FFT) in 7.2 ms, or a 64-tap FIR filter operation in 8 μs per output sample. Table 1 lists these and a selection of other key benchmarks.

TABLE 1. Benchmark Performance of the ADSP-2100.

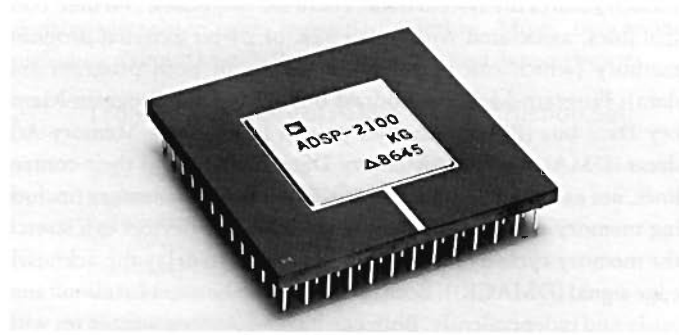
ROUTINE	EXECUTION TIME
64-tap FIR filter (pipelined rate)	8 μs/sample(125 ns/tap)
64-tap *complex* FIR filter	32 μs/sample(500 ns/tap)
Biquad filter section	0.88 μs/section
Normalized lattice filter section	0.63 μs/section
Two-dimensional convolution (3 × 3)	1.25 μs/output sample
Matrix multiply (10 × 10 matrices)	0.22 ms total
1,024-point complex FFT	7.2 ms
4,096-point complex FFT	33.3 ms
256-tap LMS adaptive filter update	64.9μs
Tenth-order LPC analysis (240-pt. rectangular window)	0.56 ms

Because of its speed and flexibility, it has become the DSP microprocessor of choice for such real-time and near-real-time applications as adaptive filtering, image processing, speech recognition and synthesis using linear predictive coding (LPC), and modem systems.† It can also be used in multiple-processor systems or as an accelerator to offload computations under control of a host computer.

To facilitate applications, Analog Devices makes available—in addition to an experienced applications staff and the usual support publications—a development system to speed program development and verification. Software tools include: a System Builder, Assembler, Linker, Simulator, and PROM Splitter; in addition, an Emulator provides the necessary hardware to debug user-developed programs in the "target system." In these pages, you will find a brief overview of the ADSP-2100 and its development system. For more information, use the reply card or get in touch with our DSP Division in Norwood, Mass.

WHY THE DSP MICROPROCESSOR?

The spectrum of DSP systems ranges from large, flexible micro-



programmed arrays assembled with such chips as multiplier-accumulators, address generators, sequencers, etc.‡—and a potentially large complement of modular memory—to self-contained compact devices, such as dedicated function chips (FIR filters, etc.) and monolithic DSP microcomputers (μPs with a substantial complement of memory). When designing general-purpose DSP chips, there is a tradeoff between memory and computing power—both compete for chip area. If sufficient memory is on-chip to handle significant problems without off-chip memory transfers, processing capability is usually far from optimum.

Since memory requirements for different applications vary widely, and external memory is cheap, the designers of the ADSP-2100 concluded that (a) memory should remain off-chip and (b) the bulk of design effort on a general-purpose chip should be invested in *maximizing computing power* and *optimizing the memory inter-*

*Use the reply card to obtain technical data.

†A few typical applications are described in some detail in a series of articles that appeared in *Electronic Design* magazine early in 1986. The series has been collected and is available as a reprint "Advanced Chips Launch a New Age of Digital Signal Processing." Use the reply card to obtain a copy.

‡For a description of a typical chip set for such arrays, see *Analog Dialogue* 20-1, pp. 7-9, "Fast 64-Bit IEEE-754 Floating-Point Multiplier and ALU," and pp. 10-11, "Fast, Flexible Word-Slice™ CMOS ICs Simplify Design of Microcoded DSP Systems."

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face to minimize delays in communication with external memory. Thus, with the exception of stacks, a small program cache, and a generous assortment of registers associated with on-chip functions, it has no memory on chip.

MEMORY

Figure 1 shows how the ADSP-2100 communicates with the outside world. *Program memory* holds the application program, *data memory* stores the system data. There are two buses, and their control lines, associated with up to 32K of 24-bit external *program* memory (which can be used for storage of both program and data): Program-Memory Address bus (PMA) and Program-Memory Data bus (PMD). Another pair of buses, Data-Memory Address (DMA) and Data-Memory Data (DMD), and their control lines, are associated with up to 16K of 16-bit *data* memory (including memory-mapped I/O peripherals—slower devices can stretch the memory cycle by inserting WAIT cycles to delay the acknowledge signal (DMACK)). Both memories can be accessed simultaneously and independently. Both can be read from or written to, with single-cycle direct access. Access time is 55ns for DM and and 50ns for PM if the processor is running at maximum speed.

Linked to two external memories in this way, the chip can access instructions and data simultaneously. However, *both* memories can store *data* if a computation uses two operands. In digital filtering, for example, a user can keep the chip's multiplier-accumulator running at full throttle by storing samples in one memory and coefficients in the other, and retrieving them simultaneously; a Data Access signal (PMDA) indicates that data, not an instruction, is being retrieved from program memory.

When the program memory is used to furnish data, it is important that extra memory cycles not be used for the data fetch, since that would negate the advantage of storing the data in program memory. Fortunately, most time-critical computations are repetitive in nature; thanks to the DSP chip's *cache memory*, those operations can be written in the form of program loops. The cache memory maintains a short history of previously executed instructions. When the program enters a loop, the cache stores the loop instructions on the first pass, then feeds the instruction register on all subsequent passes. While the cache is providing instructions, the program memory bus is free to supply data without incurring overhead cycles; thus, the processor's performance is equivalent to that of a three-memory system.

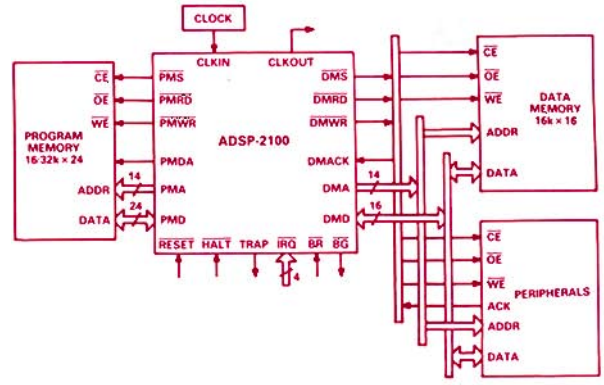


Figure 1. The ADSP-2100 in a basic system environment, with program and data memories and I/O peripherals.

Bus request and grant signals allow the ADSP-2100 to run under the control of a host processor. When another processor requests access to one of the system memories, the chip responds by halting program execution and releasing the address, data, and control lines. The chip's four interrupt-request lines can be individually programmed to respond to a signal's logic level or its edge.

COMPUTING POWER

Figure 2 shows the internal structure of the ADSP-2100. Five major buses speed the internal transfer of information. In addition to the internal extensions of the four data and program buses, a fifth, the R (results) bus, handles intermediate computational results within the chip. By providing the necessary signal paths, these buses make possible complex, multifunction instructions that can be executed in one machine cycle.

The chip's computational capabilities revolve around three functional units: an ALU, a multiplier-accumulator/subtractor (MAC), and a barrel shifter. They sit side-by-side, function independently of one another, and operate on 16-bit input data with provision for multiprecision operations. While they rely for fast interconnection on the flexible use of the R bus, each also has a feedback register to permit it to make use of its own result in its next computation while leaving the R bus free for other uses. Thus, a sequence of arithmetic operations can be performed smoothly without excessive juggling of intermediate results.

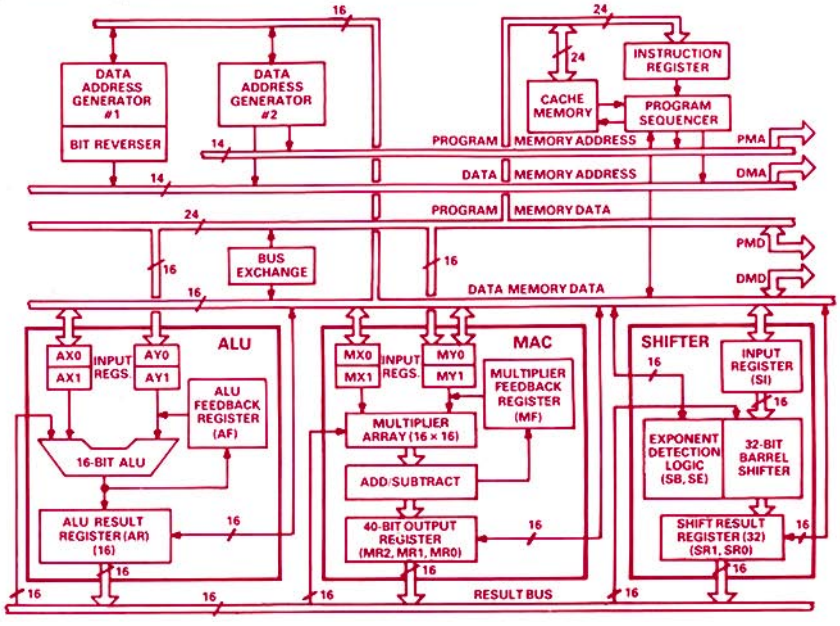


Figure 2. Basic chip architecture of the ADSP-2100. The independent MAC, ALU, and barrel shifter sections—plus the dual bus and addressing structure, the internal R-bus, and microcoded instruction cache—are central to its processing power.

Two independent address generators keep data flowing freely to the computational units, and the program sequencer has provisions for executing looped code without incurring overhead cycles. A set of background "shadow" data registers that duplicates the on-chip registers makes possible rapid *context switching* (i.e., new tasks, such as interrupt service routines, can be executed without taking time to transfer current states to storage).

ALU The 16-bit-wide ALU performs addition, subtraction, division, and logical functions. It can provide both double-precision and saturation (to eliminate rollover-type overflows) arithmetic. As a useful

option, the ALU—and the other math units—can be programmed to perform an operation *conditionally* (i.e., if a specified test is met).

MAC The MAC's repertoire includes multiply, multiply-accumulate, and multiply-subtract. Its 16 × 16 array feeds a 32-bit product into a 40-bit adder-subtractor. The final 40-bit result leaves plenty of room for overflow. The multiplier will accept any combination of signed or unsigned input formats, thus making double-precision possible. Users can also choose options for unbiased rounding and saturation of the final result.

Shifter The barrel shifter efficiently implements the numerical scaling operations needed for floating-point and block floating-point (BFP) arithmetic. It also supports double-precision shifting, normalization, denormalization, shifting by a constant, and the derivation of an exponent for an individual number or block of numbers (BFP). The shifter's array accepts a 16-bit input and produces a 32-bit output. Unfilled high-order positions in the result can be padded with zeros or extensions of the sign bit.

Registers Each functional unit contains a set of input and output registers that act as stopover points for data traveling between the external memory and the computational circuitry. In effect, the registers introduce a single level of pipelining into the data flow. Consequently, the processor's instruction set overlaps computations and register-memory transfers. Computational operations, which take their operands either from a local input register or from an output register via the R bus, load their results into a local output register.

Addressing Fast number-crunching hardware is wasted if it must frequently sit idle, waiting for data. To make this situation unlikely, especially for operations that require two operands (like addition or multiplication), a powerful memory-addressing scheme is used; the chip's two independent data address generators compute memory-reference locations at the processing rate. One of the address generators has a bit-reversing capability for scrambling or unscrambling fast-Fourier-transform data. While both can supply data-memory addresses, one of them also addresses program memory, allowing access to *data stored in program memory*.

Each address generator has four Index registers (for the memory pointers), four Modify registers (for the offset values, which move the pointers by a specified amount each time they are used), and four Length registers, which define the size of the data structures being addressed and allow *circular*—or *modulo*—addressing (for example, if an index register is pointing to the last location in a circular data structure of length 5, moving the pointer ahead by 1 will actually move it back by 4, to the first location in the structure—and vice versa). Circular addressing helps to efficiently implement digital filters, FFTs, matrix manipulations, and many other DSP routines.

A large portion of the ADSP-2100 chip is devoted to the program sequencer, which streamlines the program flow and reduces overhead when looping, branching, and responding to interrupts. It has four stacks, full interrupt capabilities, single-cycle conditional branch, and zero-overhead looping. "Do-until" loops can be any length, and the loop stack allows them to be nested four deep.

INSTRUCTION SET

Every instruction is coded into a single 24-bit word, using high-level algebraic notation, and operates in one cycle. There are four basic categories of processor instructions (Table 2): *Move* instructions encompass register-to-register and register-to-memory transfers, as well as immediate loading of registers and data memory. Memory addresses are supplied either by the data address generators or from a field in the instruction word. *Computational* instructions exercise the ALU, multiplier-accumulator, and shifter. The instructions can be executed conditionally based on the contents of the status register. They can also be combined with register-to-register and register-to-memory Move operations, including a simultaneous Read of program and data memories.

Table 2. Summary of ADSP-2100 Instruction Set.

Move Instructions
Register ⟷ Register
Register ⟷ Data Memory
Register ⟷ Program Memory
Immediate Value → Register
Immediate Value → Data Memory

Computational Instructions
ALU Operations: Add, Subtract, Divide, Negate, Increment, Decrement, Absolute Value, Logical Operations, Clear to 0.
MAC Operations: Multiply, Multiply and Add, Multiply and Subtract Clear to 0; formats: signed, unsigned, or mixed.
SHIFT Operations: Arithmetic Shift, Logical Shift, Normalize, Derive Exponent, Block-Exponent Adjust, Immediate Shifts, Denormalization and Normalization, Derive Block Exponent.
Conditional ALU/MAC/SHIFT Operation
ALU/MAC/SHIFT Operation with Register ⟷ Register
ALU/MAC/SHIFT Operation with Register ⟷ Data Memory
ALU/MAC/SHIFT Operation with Register ⟷ Program Memory
ALU/MAC Operation with Data Memory → Register and Program Memory → Register

Program Flow Control
Conditional Jump
Conditional Subroutine Call
Conditional Return
Conditional Trap
Conditional Do . . . Until

Miscellaneous
Saturate Accumulator
Modify Index Register
Push Status Stack
Pop Status/Loop/Counter/Program Stack
Mode Control
No Operation

The *program-flow* instructions direct the activities of the program sequencer. Their execution can be either unconditional or dependent on count expiration or current status-register contents. *Miscellaneous* instructions include saturation of the MAC output register, manual modification of address-generator index registers, and manual pushing and popping of the various internal stacks.

AIDS TO SYSTEM DEVELOPMENT

Hardware and software development tools for the ADSP-2100 shorten the system design cycle. The software tools consist of five modules: an *assembler*, a *linker*, a *simulator*, a *PROM splitter*, and a *system builder* (that defines the target hardware). In addition, an ADSP-2100 Emulator provides the necessary hardware to debug user-developed programs in the target system.

Modular design eases software development by permitting a complicated program to be divided into easier-to-handle modules. Programmers develop code for the ADSP-2100 by writing *assembly-language modules* with the ADSP-2100's assembly instructions. Modules can be assembled separately, then connected together with the *Linker*, which generates a complete executable program by linking together program modules that were assem-

bled separately. The linker uses the hardware environment model specified by the user with the *system builder*. The system builder specifies important details of the target hardware, like the address range of program memory, data, and I/O ports.

Before committing to final hardware, the designer can test the system's software by calling up the *simulator*. The simulator has a friendly, interactive user interface, to permit the user to monitor the simulated status of all internal and external hardware as well as the current program instruction. Programmers can display the contents of all on-chip registers (Figure 3), cache memory, and external program and data memories. In addition, the simulator permits programmers to step through code on a line-by-line basis to track all internal and external conditions.

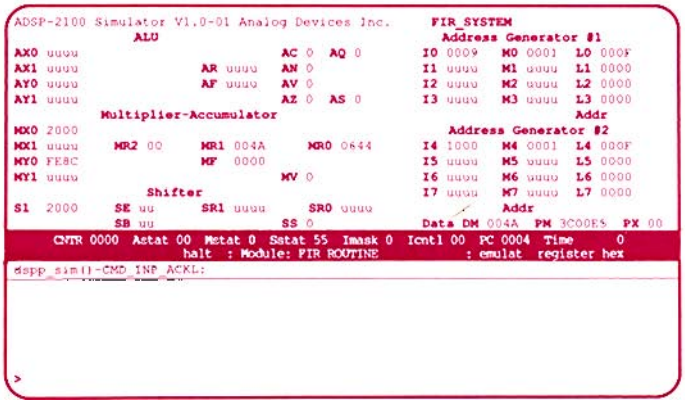


Figure 3. Basic simulator screen, showing the state of the ADSP-2100's registers at a given instant; data is in hexadecimal notation. Note the registers associated with each section of the processor. The values labeled "uuuu" are undefined.

The software tools are available for VAX computers running under the VMS operating system and for IBM PC personal computers running under MS-DOS.

When the target system reaches the hardware stage and is ready for debugging, the stand-alone in-circuit *emulator* provides full-speed (8-MHz) execution, monitoring, and control. The emulator can run executable code from its own 32K words of program RAM or from the target system's memory. Its user interface is identical to that of the simulator. The emulator also allows multiple-processor configurations and can supply trigger signals to external instruments.

EXAMPLE—FIR FILTER

The FIR filter, perhaps the simplest subsystem one might use the ADSP-2100 for, demonstrates the chip's power by implementing a discrete convolution between a series of input samples and a set of coefficients in fewer than 10 instructions. In this example (Figure 4), written in assembler syntax, the availability of a new data point from an a/d converter creates an interrupt; the service routine, when called, fetches the data point, performs an FIR calculation—using coefficients stored in program memory and the requisite number of recent data points (equal to "taps__less__one") stored in data memory, outputs the new data point through a d/a converter, and returns from the interrupt.

FIR FILTER EQUATION: $y(n) = \sum_{k=0}^{t-1} h(k) \cdot x(n-k)$

```
.MODULE/ROM     fir_routine;  {relocatable fir_routine interrupt}
                {module}

.INCLUDE        <const.h>;  {include constant declaration file}
.PORT           ad_sample;
.PORT           da_data;
.ENTRY          fir_start;
.CONST          taps_less_one = taps-1

FIR_START:      {subroutine code section}
                CNTR = taps_less-one;
                SI = DM(ad_sample);   {read from port}
                DM(I0,M0) = SI;
                MR=0, MY0=PM(I4,M4), MX0=DM(I0,M0);

                DO convolution UNTIL CE;
convolution:       MR=MR+MX0*MY0(SS), MY0=PM(I4,M4), MX0=DM(I0,M0);
                MR=MR+MX0*MY0(RND);
                IF MV SAT MR;
                DM(da_data) = MR1;   {write to port}

                RTI;   {return from interrupt}

.ENDMOD;
```

Figure 4. Summary of FIR filter interrupt service routine, showing program steps. The actual convolution occurs during successive repetitions of the one-line DO...UNTIL loop.

In the assembler description of the module, "FIR__ROUTINE", the file, "CONST", contains "taps__less__one", equal to the number of taps* minus 1. Memory-mapped locations for I/O ports are referenced as AD__SAMPLE (input port) and DA__DATA (output port). This interrupt service routine is entered at the point FIR__START. (Elsewhere, in the main__routine, the interrupt vector address is loaded; data buffers, coefficient addresses, and the counter are initialized; the address generator Modifier registers (M0 and M4) are set at 1, so that during loops the addresses are incremented by 1 on each pass, and the data buffer is cleared.)

When "FIR__START is called, the counter is set to the constant, taps__less__one; in the next cycle, the value of ad__sample is read from its memory-mapped port to register SI; then that data is moved from SI to the data memory address stored in register I0, modified by the contents of M0; then, the multiplier output register, MR, is cleared (i.e., set to zero), and—at the same time—the data (i.e., filter coefficient) stored in program memory at address (I4) is written to multiplier input register MY0, and the input data at (I0) is written to multiplier input register MX0.

The next instruction, DO convolution UNTIL CE (count expires), initiates the loop (indented) in which the contents of register MR are added to the signed product of MX0 and MY0, while—during the same cycle—the next values of data and coefficients are fetched to MX0 and MY0 from memory locations determined by the incremented address generators, as the counter counts down. When the counter reaches zero, the next instruction (multiply and add, with rounding) is executed. Then the overflow flag is checked; if an overflow has occurred, the output is saturated (viz., set to full-scale). Finally, the value stored in register MR1 (the most-significant word) is written to the d/a converter, and the program returns from the interrupt.

Portions of this article are drawn from an earlier article by John Roesgen and Sayuri Tung, "Moving Memory Off Chip, DSP µP Squeezes in More Computational Power," ELECTRONIC DESIGN, February 20, 1986.

*Note that the powerful use of symbolic references, such as "taps" and "taps__less__one" makes it easy to change the number of taps without changing the program.

16-BIT DAC IS 16-BIT MONOTONIC—ALL GRADES & TEMP RANGES

Low-Noise, Voltage-Output, Single-Chip AD569 Is µP-Compatible, Double-Buffered

High DC Stability with 100-kHz Analog Bandwidth, 3 µs 16-Bit Settling Time

The AD569* is a monolithic voltage-output 16-bit multiplying d/a converter with true 16-bit resolution: all grades are monotonic over temperature. Its double-buffered digital input is compatible with 8- or 16-bit microprocessor buses. The analog output, via a buffer follower (Figure 1), delivers ± 5 volts at up to 5 mA and can stably drive up to 1000 pF of capacitive load. Its analog (reference) input terminals are in force-sense pairs to preserve gain and offset accuracy in the presence of wiring and ground resistance.

The AD569 is useful for the many instances where one of 64K possible words of digital data must be converted to an analog output, with unique and monotonically increasing analog values corresponding to binary data. Typical applications include closed-loop process control, position servo applications, building block for 16-bit-resolution a/d converters, and high-precision waveform generation†. Its multiplying capability permits digitally controlled scaling to be applied to analog input signals, analog inputs to control the gain of digitally generated waveforms, and—in conjunction with the AD588 monolithic precision voltage reference‡—the implementation of a high-stability fixed-reference DAC (Figure 2).

Figure 1 shows the unique two-stage voltage-segmented architecture of the AD569. There are two cascaded tapped strings of 256 (= 2^8) equal resistors in series, buffered by unity-gain followers. The reference voltage, $V_{REF} = +V_{REF} - (-V_{REF})$, is divided into a series of (ideally) equally spaced voltages appearing at the taps of the first string.

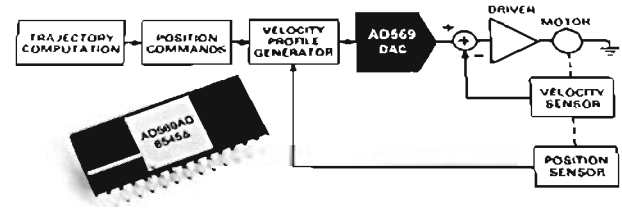
When a 16-bit digital word, of value 256 M + L, is latched in, the (M)ore-significant 8-bit byte is decoded, and the difference voltage, $V_{REF}/256$, across the (M + 1)th resistor, is buffered and applied to the second voltage divider. The (L)ess-significant 8-bit byte is decoded and the output voltage at the Lth tap, referred to $-V_{REF}$, is equal to the voltage at the lower tap of the first string, V_{REF} (M/256), plus the product of the output difference of the first string ($V_{REF}/256$) and the divider ratio of the second string, V_{REF} (L/256), i.e.,

$$V_{OUT} = V_{REF}\left[\frac{M}{256} + \frac{L}{256^2}\right] = \frac{256M + L}{65{,}536}$$

The dividers are inherently monotonic; and monotonicity at segment boundaries is preserved, despite offsets in the difference amplifiers, by a leapfrogging switching scheme that lets each amplifier work on both sides of alternate taps. In order to obtain the advantages of cool (200 mW dissipation), compact, fast CMOS logic and nonloading switches, and at the same time retain the low drift and noise of fast-settling (3 µs to 0.001% FS) bipolar amplifiers, the Analog Devices BiMOS II process is used.

The result is a maximum differential nonlinearity specification of ± 1 LSB over temperature for all grades. Integral nonlinearity is ± 0.024% max over temperature for the K/B grades; however, it is *stable over both time and temperature* (typically < ± 0.25 LSB per 1,000 hours), owing to the untrimmed architecture of the DAC. This permits 16-bit linearity over temperature to be achieved and maintained with software error correction alone.

Packaging is in ceramic (plastic available soon). Prices start from $28.00 (AD569AD in 100s).



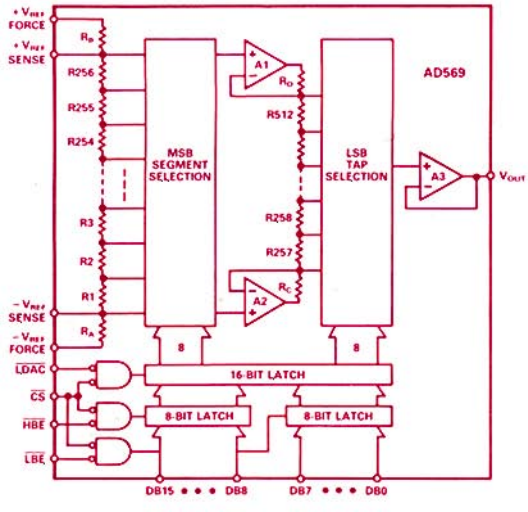


Figure 1. The AD569 is a pair of cascaded 8-bit tapped voltage dividers, buffered by unity-gain followers.

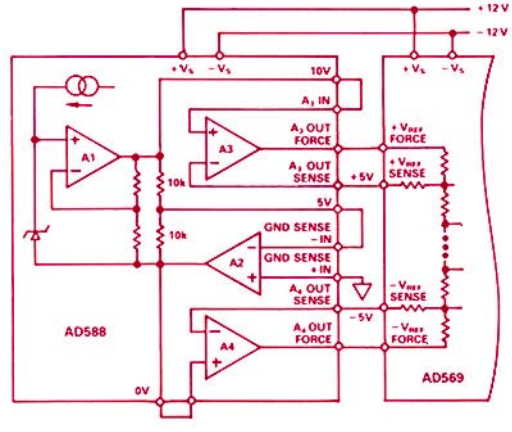


Figure 2. Kelvin connections (complementary use of force-sense terminals) with ultra-low drift tracking reference puts the reference voltage precisely at the active ends of the first resistor string, in the same way the buffer followers' feedback puts the tap difference voltage across the second string.

*Use the reply card for technical data.

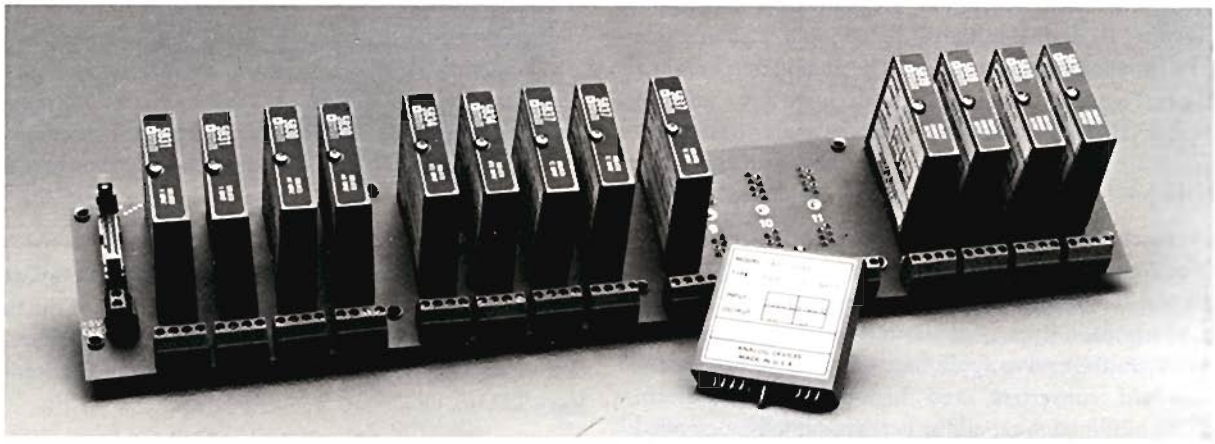
†For a typical user application, see "Plug-in Card Generates Arbitrary Waveforms," *Electronic Design*, Oct. 2, 1986 (pp. 49-50).

‡The recently announced AD588 will be covered in some detail in the next issue of this Journal.

COMPACT LOW-COST SIGNAL-CONDITIONING MODULES

The 5B Series Features Direct Sensor Interface, 1,500-V rms Isolation, High Noise-Rejection, −25°C to +85°C Operation, No Adjustments

by Kathryn Kasper



The 5B Series modules* are a family of plug-in single-channel signal conditioners for sensors. Readers familiar with the 3B Series subsystem (*Analog Dialogue* 16-3, 1982, pp. 7-9) will recognize the 5B Series modules as a new generation characterized by even higher performance, smaller size, and lower price; we expect that users will take to them as enthusiastically as they adopted the 3B Series for monitoring analog signals such as pressure, temperature, and flow in industrial data-acquisition applications.

A new circuit design using transformer-based isolation combines with automated surface-mount manufacturing technology to provide compactness and high performance at low cost. Joining these features with operation on a single +5-V supply, 1,500-V rms isolation and ±0.05% calibration accuracy, the 5B Series is an attractive alternative to expensive commercial signal conditioners and in-house designs for industrial applications. Substantial discounts in quantity encourage OEM use in systems; the 5B Series modules are priced at less than $80 in quantity.

In addition to the 5B Series modules, physically and electrically compatible backplanes are available to make it easy to assemble the modules into complete signal-conditioning subsystems. As many as 16 modules can be placed in a 19" rack-mountable backplane that requires only 3 ½" of panel space.

RUGGED, COMPLETE, HIGH-PERFORMANCE

All modules are identical in pinout and size (2.25" × 2.25" × 0.60"). Users can mix and match them to meet the specific needs of the application, and they can be changed without disturbing field wiring. Each module provides complete signal conditioning, optimized for the nature of its input. Signal-conditioning functions include input protection, filtering, chopper-stabilized low-drift amplification, isolation, linearization for RTD inputs, and excitation for sensors when required. Table 1 is a summary of module types available at this printing.

The specifications and packaging of the 5B Series were designed for industrial applications. Each module has factory-calibrated ±0.05% accuracy and features 1,500-V rms isolation, ±1 μV/°C input drift, and 240-V protection for all field terminations. All modules feature excellent common-mode rejection, meet IEEE 472-1974 surge-withstand specs, and operate over the −25°C to +85°C temperature range. Physically, the 5B Series is rugged: The modules are hard-potted and have sturdy 0.04-inch pins; there are no adjustment potentiometers. The inaccuracies that could be introduced by these mechanically sensitive devices are avoided, and system integrity is improved since there are no exposed field adjustments.

TABLE 1. 5B Series Modules and Backplanes Available in Late 1986.

Input Type/Span	Output	Model
INPUT MODULES		
DC, ±5 mV to ±500 mV	0-5 V or ±5 V	5B30,5B40
DC, ±500 mV to ±10 V	0-5 V or ±5 V	5B31,5B41
Process Current, 4-20 mA or 0-20 mA	0-5 V	5B32
Thermocouple types J,K,T,E,R,S,B	0-5 V	5B37
2,3,4-wire RTDs:		
100-Ω Pt, 10-Ω Cu, 120-Ω Ni	0-5 V	5B34
OUTPUT MODULES		
0 to +5 V or ±5 V	4-20 mA/0-20 mA	5B39
BACKPLANES (WITH COLD-JUNCTION SENSORS)		
16 channels, pin-compatible with 3B Series		5B01
16 channels, with "analog 3-state" output multiplexing		5B02
1 channel, DIN rail compatible		5B03

ISOLATED INPUT MODULES

The modules listed in Table 1 are available in standard ranges that address most input requirements. However, the flexible laser-trim process that ensures calibration accuracy to within 0.05% can be used for calibration of other input spans. This custom ranging capability allows you to map any input range into the full output span, thereby improving system resolution within that narrow range. The 5B Series input modules require only a single +5-volt supply; they consume about 0.15 W typically.

Example: 5B37 Thermocouple input module Figure 1 is a diagram of the 5B37 transformer-isolated thermocouple input module. The

*Use the reply card for technical data.

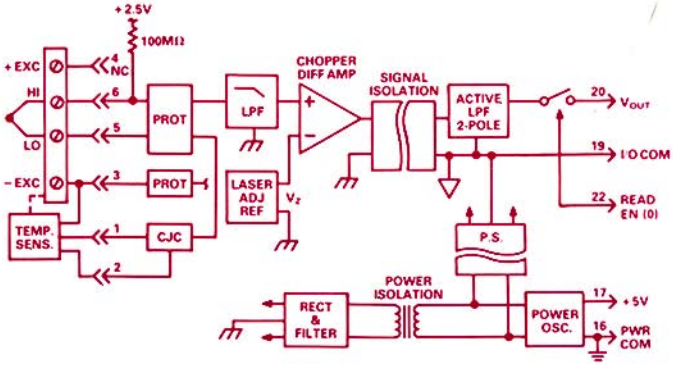


Figure 1. Block diagram of 5B37 thermocouple module.

1,500-V isolation provides both protection and 160 dB of common-mode rejection and assures compliance with IEEE 472-1974:SWC. As is the case with all modules, 240-V normal-mode input protection prevents damage if line voltage is accidentally connected to its input terminals. Cold-junction compensation circuitry corrects for ambient temperature and its variations.

Like all the input modules, the 5B37 includes a self-multiplexed output—a low-resistance series output switch (much like digital 3-state), controlled by a TTL-compatible Enable input. If the switch is not used (single channel or conventionally multiplexed applications), the Enable input can be grounded.

OUTPUT MODULE

The 5B39 Output Module (Figure 2), provides an isolated 0-20-mA or 4-20-mA process-current output. It provides the same level of protection as the input modules, 1,500-V rms isolation and 240-V rms continuous output protection. Maximum load resistance is 750Ω and power consumption is 0.85 W.

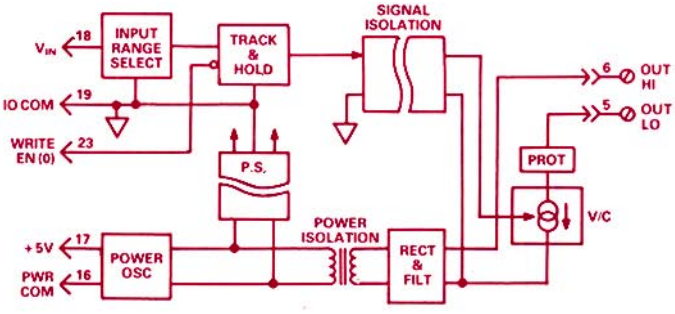


Figure 2. 5B39 output module.

The voltage input to this module is latched—if need be—in a track-hold circuit. When each module is updated by its track-hold under logic control, one d/a converter can serve numerous output channels. With the Enable lines grounded, the modules can be used with one DAC per channel.

Figure 3 shows a general application of input and output modules in a system.

SYSTEM DESIGN

The functionally complete 5B Series modules are easily applied in the designer's own circuit board or backplane. The modules have a simple pinout; they plug into widely available sockets; and they are secured with self-contained mounting screws. The output

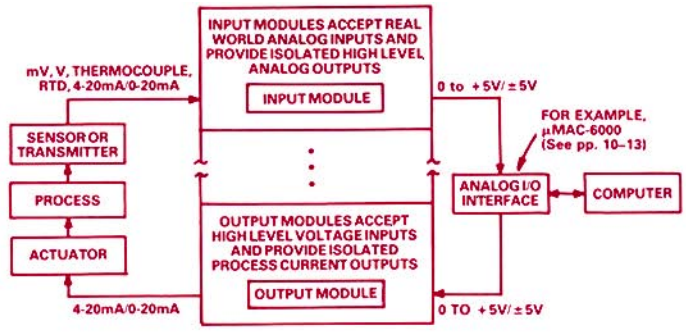


Figure 3. General measurement-and-control application.

switch eliminates the need for an external multiplexer with input modules and the track-hold in each output module allows a single DAC to serve numerous output channels. For thermocouple applications, cold-junction-compensation sensors are available as one-piece pre-calibrated units. An example of an *integrated system* is shown in the following pages, where the modules are used with the μMAC-6000 backplane.

5B SERIES SUBSYSTEMS

Complete 5B Series subsystems reduce user design effort. A family of backplanes, precalibrated plug-in modules, direct sensor interface via screw-terminal connections, standardized high-level outputs, and ribbon-cable system interface result in easy integration into any system. For thermocouple applications, high-accuracy cold-junction compensation sensing is inherent on each channel.

To address diverse applications, the 5B Series includes a growing family of backplanes (Table 1). The 5B01, a 16-channel backplane that can be mounted in a 19" × 3.5" panel space, provides 16 single-ended *input/output plugs* on the system connector; it is pin-compatible with the 3B Series (note, however, that the 5B Series has a ±5-V output swing, while the 3B Series has a ±10-V output swing). The 5B02 (Figure 4) has *input and output buses*, which take advantage of the built-in switching in the modules. With the 5B02, external input multiplexers are not needed for inputs, and only a single output DAC is needed. For *single-channel* applications, the 5B03 DIN-rail-compatible socket is available.

The 5B Series delivers, for the first time, a low-cost solution to industrial signal conditioning. The family will continue to evolve, as backplanes and modules are added to meet user demand.

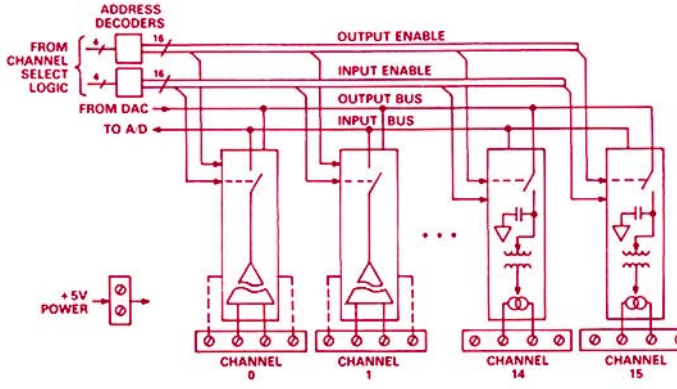


Figure 4. Diagram of the 5B02 backplane.

EXPANDABLE MODULAR I/O PROCESSOR FOR INDUSTRIAL AUTOMATION

µMAC-6000 Handles Real-World Analog and Digital Signals Provides Isolation, Signal Conditioning, Conversion, Processing, Communications

By Bill Schweber

The µMAC-6000* is a modular multiple-input/output processor system for analog signals and digital decisions. It combines computing, communications, and sophisticated software. Alone, or with a host computer, it monitors and controls processes and machinery. Designed for OEM use, it finds applications in equipment monitoring, continuous control, test-stand automation, and energy management. Each plug-in signal-conditioning module addresses one channel; thus users can custom-configure inputs and outputs. Expansion with extra processing power makes it possible to increase the number of channels with little effect on performance.

This newest member of the µMAC family of programmable systems for real-world measurement and control evolved from the technical and product experience gained by Analog Devices and its customers with the earlier µMAC-4000 and µMAC-5000 systems [*Analog Dialogue* 15-1 (1981) and 17-3 (1983)]. The µMAC-6000 is manifestly similar to, yet better—faster, more modular, and more configurable—than either of its predecessors.

A BRIEF HISTORY OF THE µMAC FAMILY

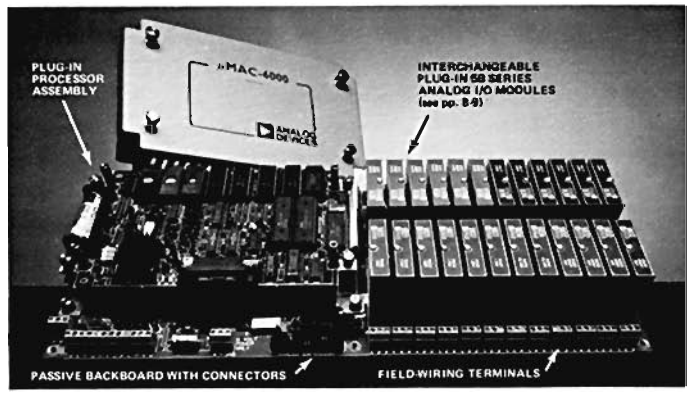
In the fall of 1980, Analog Devices introduced the µMAC-4000 system. This "Micro Measurement-And-Control" system endows virtually any computer with real world input and output capability (thermocouples, currents, voltages, on/off signals). Connected to the RS-232 or 20-mA current-loop serial ASCII port of any computer, and operating in a command/response mode, the µMAC-4000 uses ASCII characters to pass data. The host computer generates an ASCII string with a request (for the temperature of the signal on Channel 1, for example), and the µMAC-4000 returns the value, e.g., 47 degrees.

Besides the serial interface and the analog-to-digital converter, the main circuit board of the µMAC-4000 contains all the electronics needed for high-quality, isolated signal conditioning of the analog inputs. This single board (which could be expanded with additional boards)—and such computers as the HP-85, Apple II, IBM PC, and PDP-11—form data-acquisition, measurement, and control systems for such applications as laboratory automation, temperature monitoring, and water treatment. All of the µMAC-4000's acquired data is processed at the host, which also makes the decisions and requests the necessary outputs.

User needs and requests, along with technology advances, led to the announcement of the µMAC-5000 in late 1983. While the µMAC-5000 resembles the µMAC-4000 (and uses many of the same expansion cards) there is a major difference: the µMAC-5000 is user-programmable in µMACBASIC, a real-world-I/O version of BASIC (see below). The advantages of user programmability are vital:

The user application program can reside on and execute from the µMAC-5000 board, allowing it to perform data acquisition & processing and to make decisions, functioning independently of the communications link between the µMAC-5000 and the host.

*Use the reply card for technical data.



Also, the overall integrity of the system is increased. The link to the host is used mainly for transmitting overall application parameters (such as loop constants) to the µMAC-5000 system on start-up or summary data back to the host. If the communications link to the host is down, the µMAC-5000 can continue to function and perform the application.

The entire applications program can be burned into programmable read-only memory (PROM), which is then installed on the board, fully resident and ready to execute as soon as power is applied, making the µMAC-5000 ideal as a stand-alone, dedicated controller for machinery (such as extruders and testing) or for dedicated data logging and fixed-function control applications. No host computer is needed in these applications; the µMAC-5000 can drive a local operator terminal or annunciator screen.

µMACBASIC: THE LANGUAGE OF THE µMAC-5000

A key feature of the µMAC-5000 (and µMAC-6000) is the µMACBASIC language, developed by Analog Devices for the system's real-world, real-time applications. Standard BASIC, though easy to use and familiar to both programmers and non-programmers, lacks several features that are necessary for good, effective real-world applications programs. µMACBASIC adds them:

With *integral I/O statements*, an analog or digital input or output can be incorporated into the applications program. Keywords were added to BASIC; for example, to input an analog signal simply requires using the keyword AIN, along with parameters that define the analog signal's physical input (connection location and type). Once the system executes this keyword, all of the internal details needed to find the input channel, connect the a/d converter to the appropriate input channel through the multiplexer, make the conversion, and translate the converted value to engineering units are done automatically and transparently to the user.

Procedures and Functions were added for a more structured BASIC. Traditionally, BASIC programs result in intertwined "spaghetti" code because programmers, using GOTO statements, have difficulty efficiently structuring the flow chart and corresponding program. In addition, the requirement to use a single set of line numbers and unique variable names makes it hard for more than one programmer at a time to work on a single application,

without causing conflicts. μMACBASIC's Procedures and Functions allow programmers to develop independent modules of code; they can be called from the main program by name.

Real-time operation is a necessity for most applications where real-world signals must be measured and controlled, since timing is critical to the process. It is important to update the control loop at exact intervals, e.g., 100 ms, rather than approximate intervals variable from 50 to several hundred ms, depending on program flow. With μMACBASIC's real-time interrupt capability, the user application program can specify that certain activities occur at a desired rate; unplanned events (such as characters arriving via a communications port) are handled efficiently but do not delay time-sensitive events.

μMAC-6000—THE NEW GENERATION

The μMAC-6000 was designed to incorporate preferred features of the previous μMAC models and maintain the high level of system integration, which makes the μMAC attractive in so many applications. Key goals included improved performance, attractive pricing, and an architecture that was:

- *more modular*, in hardware and I/O, with rugged, removable major assemblies
- *more configurable*, so that the end user could tailor the final configuration to fit system needs
- *more flexible*, to meet the needs of a wide range of applications
- *more expandable*, to grow as users' needs grow, yet maintain the required level of overall performance
- *more powerful*, using today's highly integrated ICs.

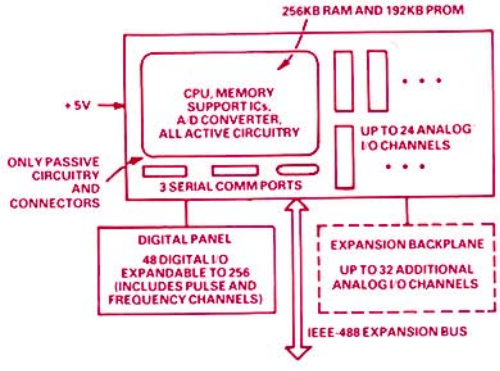


Figure 1. Basic configuration of the μMAC-6000.

Figure 1 shows the functional block diagram of the μMAC-6000. A single backplane supports the major building blocks:

- a 16-bit 80188 *CPU* with support chips, *memory*(256K bytes RAM, 192K ROM, and 2K EEPROM), a/d and d/a *converters*, and *communications-support* ICs
- *interchangeable* low-cost *analog I/O* modules, all electrically isolated. They are the new 5B series (see pp. 8-9), which provide 1,500-volt isolation, excellent performance, and a wide choice of analog input and output conditioning for thermocouples, valves, current loops, voltage signals at various levels, and other transducers. Each channel's unique requirements are met by an appropriate module—the ultimate in flexibility and modularity.
- connectors for the *digital I/O*. They can connect directly to low-level (TTL) digital points, or via solid state relays to higher-voltage, higher-power points. Examples of digital I/O include switch closures, relays, counters, frequency inputs, and time-proportional outputs with varying duty cycles.
- *communications ports*, both serial-type (two RS-232 and one isolated RS-422) and IEEE-488 (GPIB).
- screw terminals for the *+5 Vdc power supply*, which is the only power needed to run the entire μMAC-6000 and I/O modules.

As with the μMAC-5000, the heart of the system is the CPU. But in the μMAC-6000, the *backplane* plays a critical role in meeting the design objectives; it is the physical support for the CPU, I/O field-wiring connectors, communications connections, and power. It is entirely passive, containing *no active components*.

The active blocks of the system—the CPU module—in its protective metal enclosure—and the I/O modules—are all easily removable from the backplane, without disturbing the field wiring; and they can be installed after the rack- or panel-mounted backplane has been wired completely and the field wiring checked out. Any 5B-series analog I/O module can be changed easily by loosening a single screw. Should a CPU unit require changing, it can be removed by loosening 4 screws.

Interchangeability means that any one of the 24 analog I/O locations on the backplane can be used for any 5B module—input or output. Users can change input sources at any channel or turn it into an output channel simply by putting the appropriate 5B module into a socket and identifying the module in software. As I/O needs vary, the I/O can be quickly changed.

The μMAC-6000 system supports three serial-communications ports and one high-performance IEEE-488 port. The serial ports are used for connection to host computer, local terminal, and printer—and multidrop configurations with other μMAC-6000s.

The IEEE-488 port has two purposes. First, it can be used as the internal bus to connect dedicated intelligent expansion units (called μMAC-6000E) to the main unit (Figure 2). It can also be

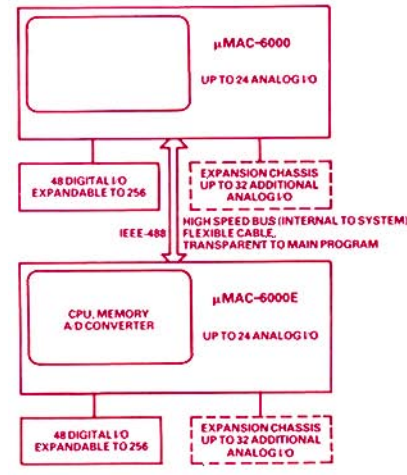


Figure 2. Expanded μMAC-6000 systems using expansion chassis and μMAC-6000E.

used to connect a μMAC-6000 to a host (using the IEEE-488 interface standard) or a specialized electronic instrument, such as a gas analyzer or high-resolution voltmeter (Figure 3).

a. Host and μMAC-6000. b. μMAC-6000 and instrument.

Figure 3. IEEE-488 communications.

EXPANSION

In many application the number of channels is large but the rate at which these channels have to be sampled is relatively low. A good example of this is a large temperature-monitoring installation, which has many thermocouples attached to critical points on an engine. The µMAC-6000 is designed for the number of channels of analog I/O to be increased beyond the basic 24; each µMAC-6000 backplane has an analog expansion connection for two additional 16-channel backplanes, which can hold up to 32 5B Series modules of any type. Effectively a physical extension of the main backplane, it doesn't have a CPU, ADC, memory, or any other processor components; it brings the total number of channels that a single µMAC-6000 can support by itself to (24 + 32 =)56.

The overall throughput and performance decrease as the CPU and A/D converter must service the increasing number of channels (dashed curve in Figure 4). For applications where this is intolerable, *intelligent expansion* is available using the *µMAC-6000E*. Each µMAC-6000E brings another CPU and ADC into the system, so that more I/O channels can be handled without severe degradation in performance (solid curve).

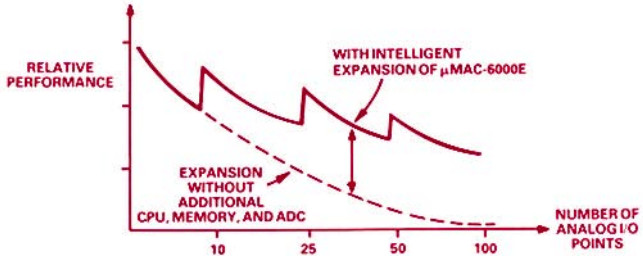


Figure 4. Avoiding performance deterioration in expanded systems by *intelligent* expansion. Performance vs. number of I/O points.

Up to three such units, acting as IEEE-488 talker/listener devices, can be connected via the IEEE-488 bus to the main, master µMAC-6000, acting as the IEEE-488 controller.

The user's ability to add modular CPU and A/D units to the system as the number of I/O channels increases makes the µMAC-6000 unique. Unlike most data acquisition and control systems, the µMAC-6000 architecture allows the channel expansion—when necessary—to include an additional CPU and a/d converter via the µMAC-6000E, so overall performance degrades much more slowly.

Each µMAC-6000E is physically and electrically very similar to the basic µMAC-6000; it can handle the same amount of real-world analog and digital I/O as the basic µMAC-6000, including "dumb" expansion. The result of this design is that a user can start with a standard 24-analog-channel µMAC-6000, add up to 32 more analog channels, and/or use additional µMAC-6000E units to increase channel capacity and processor power as needed.

The digital I/O has not been neglected either; both analog and digital I/O can grow with the needs of the application (a typical installation has 1 or 2 digital points per analog point). Each µMAC-6000(/E) can directly interface with up to 48 digital I/O points. In addition, a multiplexed digital I/O panel is available; it allows the same physical connector of the µMAC system to handle up to 256 channels. The user can upgrade capacity in this way at any time, even in the field, by simply changing digital I/O panels; no changes are made to the basic µMAC-6000 system.

SYSTEM SOFTWARE

When the system is programmed in µMACBASIC, the statements for real-world I/O and real-time operation tie together all the hardware pieces of the system—I/O, CPU, memory, timers, etc., so that the user sees a fully integrated system, despite its building-block nature. One or more µMAC-6000E units can be added without affecting the level of integration; the µMACBASIC statements have a simple argument list which allows the user to identify whether the I/O channel is on the main µMAC-6000 board or an IEEE-488-linked µMAC-6000E. Handshaking and operating details for passing data over the bus are automatic; they are made transparent to the user by the µMAC-6000's operating-system software and programming language. The real-time clock keeps time accurately, even when power is off.

The user's program can be stored in the on-board RAM (256K bytes), fully backed up by a socket-mounted lithium battery, which can be replaced at the end of its 6 + -month life without turning off the power. For greater non-volatility, the program can be burned into PROM.

While the µMACBASIC language is convenient and flexible, many programmers want the benefits of more-powerful, standardized languages; accordingly, the µMAC-6000 is available with the C language instead of µMACBASIC. C is a transportable language that improves memory usage, speed, and efficiency with the existing hardware. Figure 5 compares a µMACBASIC program fragment with the same fragment written in C.

µMACBASIC

```
100 Value = (Ain(1) + Ain(2)) / 2
110 If Value > Hi_Val Then Print "ALARM"
    Else Print Value
```

C

```
ret1 = ain(1, &val1);
ret2 = ain(2, &val2);

value = (val1 + val2) / 2.0

if (value > hi_val)
  printf ("ALARM")
else
  printf ("%f", value);
```

Figure 5. Comparison of syntax in µMACBASIC and C: Sampling two input values, averaging them, and printing if in range or sounding alarm if not.

An IBM PC is used as the development tool for µMACBASIC-6000 C. In the C version of µMAC-6000, the compiled C object code is linked to its C libraries; the linked code is downloaded from the PC to the µMAC-6000, where a special C operating-system PROM allows this object code to execute properly and perform real world I/O, as called for by the user program. The C PROM on the µMAC-6000 requires less memory than the µMACBASIC PROM, leaving more PROM space for user programs.

The processor board of the µMAC-6000 is designed to accommodate an optional 8087 numeric co-processor IC, which increases the speed of numeric computations by factors from 20 to 100. The 80188-8087 µMAC-6000 system with C gives highest performance.

COMMUNICATIONS AND SOFTWARE TOOLS

The ability to effectively *develop* programs for a system like the µMAC-6000 depends on the right development tools. The usefulness of the µMAC-6000 when actually *running* the application is

related to the communications topologies and run-time software available.

The µMAC-6000 system can be connected to a host via RS-232 or RS-422 serial interface ports. The RS-422 port on the system backplane is specifically designed for noisy environments and *multidrop communications*; two twisted pairs of wires can link up to 10 µMAC-6000 systems, at distances of several thousand feet, to a host (Figure 6).

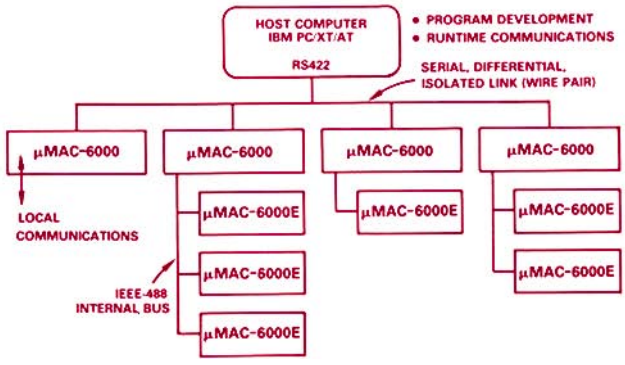


Figure 6. µMAC-6000s in various systems using multidrop topology.

The µMAC-6000 has two software tools available:
For *developing* the program, program-development software (PDS) is used. With PDS, the user types program lines of code on a terminal or IBM PC (acting as a workstation) connected to the µMAC-6000; they are edited and stored on floppy disks. Programs can be recalled and downloaded to the µMAC-6000. Any µMAC-6000 connected via the multidrop line can be addressed uniquely; new lines of code can be sent to it while other units continue to run.

For communications between the host and the µMAC-6000(s) while running the application program, a software package called *MCComm* is available. MCComm* is a master/slave protocol which allows a host computer program to transfer arrays of data or strings to the µMAC-6000, or request that a specified array or string be returned from the µMAC-6000 to the host. Through this mechanism, data transfer in both directions is achieved (Figure 7).

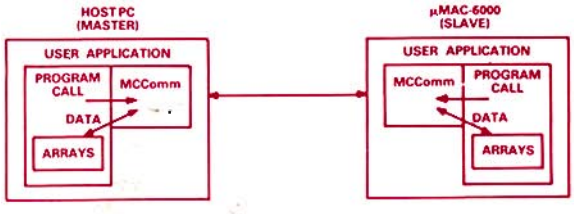


Figure 7. Master-slave operation using MCComm link.

SALIENT POINTS OF SYSTEM DESIGN

Figure 8 is a simplified block diagram of the CPU assembly. The analog inputs from the 5B-series modules can be read directly by the ADC or first passed through a 10-kHz filter to minimize high-frequency noise. The choice of filter-*in* or -*out* is made by a parameter in the argument list for analog input-conversions and can be changed as input noise conditions require. The a/d converter has software-selectable resolutions of 12 or 14 bits, using a 12-bit a/d converter, a 14-bit DAC, and subranging; the additional time for conversion to 14 bits is 1 conversion cycle. Either resolution can be called for at any time as needed.

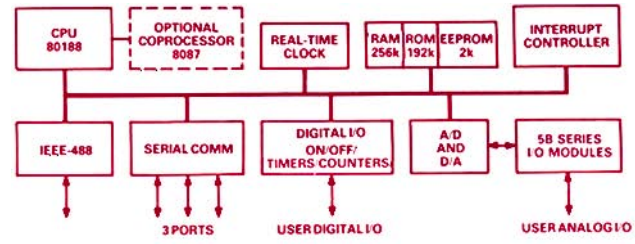


Figure 8. Block diagram of µMAC-6000's CPU and system architecture.

Among µMAC-6000's protective features, a simple software command permits the analog input subsystem to read the temperature of the CPU module, under its protective metal housing, in order to detect a potential heat problem and alert an operator. Similarly, the exact value of the +5 V dc supply at the CPU can be read by the program as part of a periodic self-check on the system status, especially if intermittent operation is suspected.

RAM is battery-backed. Special power-detection circuitry monitors the +5-V dc line. If system power should start to fail and supply voltage drops below a threshold, the processor is interrupted and critical register-saving routines are initiated. The user program is also interrupted to let the program know that there are milliseconds left in which to implement a special power-failing application routine, if present.

The CPU circuitry also has a "watchdog timer" function, calling for a periodic reset by the operating system. If a problem in the circuitry or software causes the reset to be missed, the watchdog output produces a state change of an open collector connected to a screw terminal on the system backplane. An alarm or indicator, if wired to it, can alert the operator to the problem.

CONNECTABILITY

A key factor in the µMAC-6000's usefulness is that it is designed to interconnect with a wide range of entities, from the broad repertoire of analog inputs and outputs available via the 5B modules, to communications with host processors and peripherals, to easy system expansion via the expansion chassis and the µMAC-6000E, to other instruments via the IEEE-488 bus (Figure 9). In this sense, µMAC-6000 is a *universal* input/output subsystem.

The µMAC-6000 includes the CPU enclosure—with µMAC-BASIC software in PROM—and the backplane. With discounts available for quantity, the µMAC-6000/6000E are priced at $3,395/$2,295.

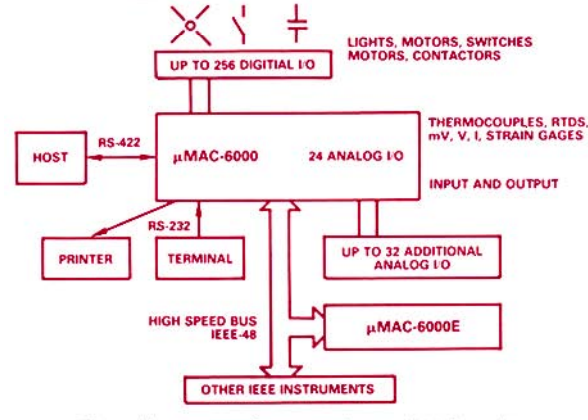


Figure 9. The diverse universe that µMAC-6000 connects with.

*For information on MCComm use the reply card.

PRECISION WIDEBAND THREE-PORT ISOLATION AMPLIFIER

AD210 Has 2,500-V Continuous RMS CMV rating, 0.012% Nonlinearity, 20-kHz BW Design Expertise, Surface-Mount Combine for Highest Performance & Low Cost

by James Conant

The AD210* is a complete high-performance three-port isolation amplifier in a 1.00" × 2.10" × 0.35" (25.4 × 53.3 × 8.9-mm) package. Its input, output, and power sections are isolated from one another for continuously applied common-mode voltages up to 2,500 volts rms at 60 Hz (±3,500 volts peak).

Salient features include: maximum nonlinearity specification of ±0.012% (AD210BN), 20-kHz full-power −3-dB bandwidth, and 2-μA-rms maximum leakage current at 240 V rms, 60 Hz. The input amplifier is an uncommitted op amp; the output stage is buffered by a unity-gain amplifier that can drive a 2-kΩ load to ±10 V.

Typical applications for isolators include multi-channel data acquisition, high-voltage instrumentation amplifiers, current-shunt measurements, and process-signal isolation. With its 120-dB common-mode rejection (60 Hz, gain of 100, 500-ohm resistive imbalance) the AD210's isolation performance allows it to maintain signal integrity when making safe measurements of low-level signals in harsh industrial environments, where signal interference, ground faults, and transients are commonplace.

The AD210 owes its unequalled performance and user-oriented features to surface-mounted components and state-of-the-art automated assembly technology, backed by Analog Devices' 15 years of experience in the design and manufacture of isolators. The high performance, small size, and low cost of the AD210 make it ideal for application in process controllers, data loggers, welders, power monitors, motor controls, and test equipment.

HOW IT WORKS

The AD210 (Figure 1) requires +15-volt dc (±10%) excitation, applied to the power section. A 50-kHz oscillator couples power to the input and output sections via isolation transformers T2 and T3. In both sections, the coupled power is rectified and filtered; ±15 V dc is made available to operate all of the AD210's internal circuitry—and to provide up to 5 mA at ±15 V dc at the power-output pins in both sections.

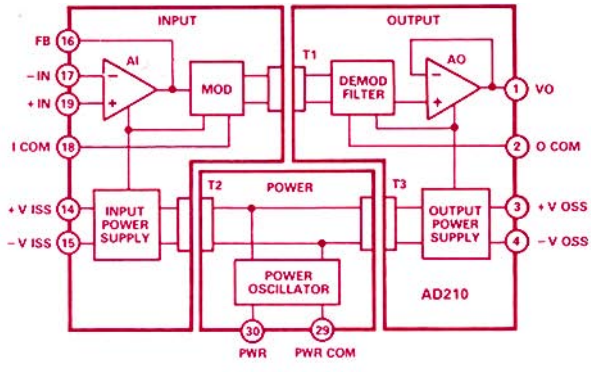
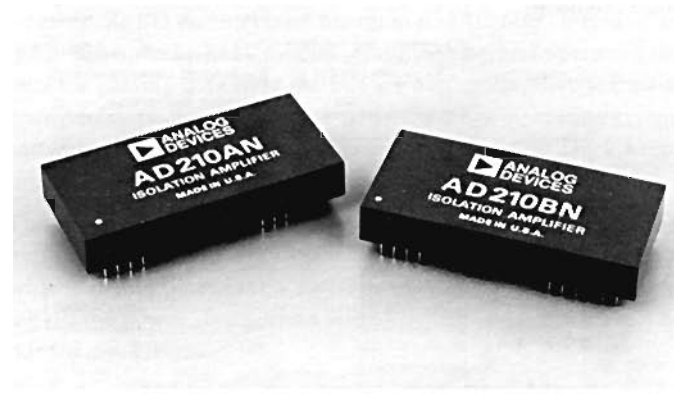


Figure 1. Input, output, and power sections are isolated from one another with 2,500-volt rms (3,500-V peak) common-mode ratings.

*Use the reply card for technical data.



The 50 kHz also serves as a carrier, modulated by the output of AI, coupled across the isolation barrier by transformer T1, synchronously demodulated and three-pole filtered (20-kHz cutoff) in the output section, and buffered by follower AO, which can drive low-impedance loads.

The three-port design permits the AD210 to be configured as an input *or output* isolator, in single- or multi-channel configurations. Besides eliminating the need for a separate dc-to-dc converter, the AD210 in fact serves as a pair of isolated power supplies (within its ratings) for circuitry sharing common ground returns with the input and output signals, for example, front-end preamps, remote transducers, etc.

The uncommitted input op amp can be configured by the user for buffering and gain, filtering, summing, voltage ranging, and current inputs. In the example of Figure 2, amplifier AI is used as a non-inverting gain-of-100 amplifier; the isolated input power supply serves the input offset adjustment circuit.

Two performance grades are offered for operation over the −25°C to +85°C temperature range, AD210AN and AD210BN. Specifications include: maximum gain drift ±50 ppm/°C (and ±25 ppm/°C, 0°C to +70°C); offset drift ±10 ± 50/G μV/°C (and ±10 ± 30/G μV/°C, 0°C to +70°C). Other maximum guaranteed specifications include (A/B): nonlinearity ±0.025%/0.012%; offset (±15 ± 45/G)/(±5 ± 15/G) mV; gain error ±2%/1%. Price in 100s is $47 for AD210AN and $56 for AD210BN.

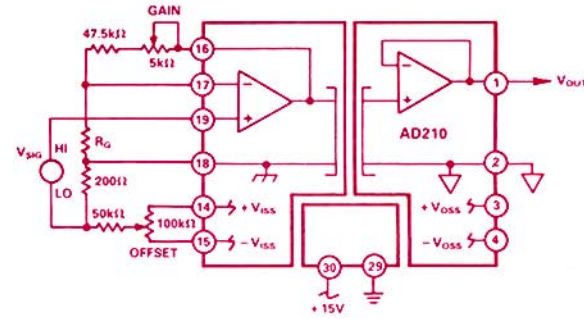


Figure 2. Noninverting gain is set in the same way as for an operational amplifier. Floating power is used for offset trim.

MONOLITHIC SYNCHRONOUS V/F CONVERTER: 0.005% MAX NONLINEARITY

Full-Scale Frequency (up to 2 MHz) Set by External System Clock

No Critical Components Required; 25 ppm/°C max Drift; Dual or Single Supply

by Paul Klonowski

The AD651* is a fast, high-precision single-chip charge-balance analog (voltage or current) to frequency converter. It is a *synchronous* VFC, in that its full-scale output frequency depends on an external clock frequency instead of the usual external capacitor in a one-shot oscillator circuit. The result is a stable, linear transfer function, with significant application benefits in both single- and multi-channel systems. Applications include a/d conversion, process control, analytical and medical instrumentation, isolated data acquisition, and frequency-to-voltage conversion.

The AD651 works with either single or dual power supplies and requires only a single non-critical integrating capacitor. Maximum nonlinearity is ±0.005%, for full-scale output frequency up to 1 MHz (B grade), increasing to only ±0.02% at 2 MHz, while maximum gain drift, over the temperature range, is only ±25 ppm/°C for frequencies up to 500 kHz, increasing to ±50 ppm/°C at 2 MHz. Corresponding figures for the A & S grades are 0.02% and ±50 ppm/°C, increasing to 0.05% and ±75 ppm/°C over their respective temperature ranges. It is available in a 16-pin Cerdip package; prices start at $7.95 (AD651AQ, 100s).

ABOUT VFCs

A typical charge-balance V/F converter[1] is based on an integrator that has two modes, *integration* and *reset*. The input signal (I_{IN}) is continuously integrated with respect to time, building up charge proportional to its average value; during the fixed reset period, $-I_{REF}$, an opposing fixed current (hence a fixed charge) is integrated and subtracted from the accumulated input charge, giving the characteristic triangular waveform. Whenever the integrated input exceeds a threshold, a reset interval starts; its duration is determined by an external capacitor, which establishes the period of a one-shot (T_{os}). Thus, the greater the input, the more often the reset phase occurs. The output pulse begins at the same time as the reset interval; therefore, the output frequency is equal to the number of Resets per second. The output relationship is:

$$f = \frac{I_{IN}(avg)}{I_{REF}\, T_{os}} \qquad (1)$$

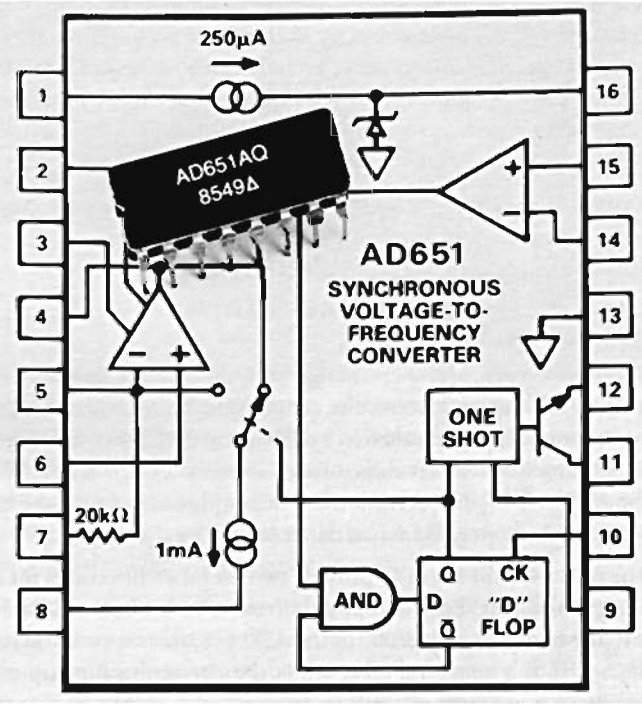
Since T_{os} depends critically on a capacitance, output frequency is subject to the external capacitor's temperature coefficient and dielectric properties.

The *synchronous* VFC differs in that the length of the reset interval is precisely equal to the clock period. Thus,

$$f = f_c \frac{I_{IN}(avg)}{I_{REF}} \qquad (2)$$

Since clock frequencies can be crystal-controlled, f_c may be eliminated as a source of error; thus, the major source of error has been removed. The remaining sources of error (which are present in both types)—reference, threshold, integrator, and switching errors—limit the performance, but are less significant than the one-shot's capacitor.

Besides accuracy, the synchronous VFC has other advantages: When used with a multi-phase clock, it can be multiplexed with similar VFCs to transmit several outputs over a single channel. In a/d conversion, where the digital output is determined by counting output pulses for a preset period, if the same clock drives the VFC and (through a suitable divider) sets the counting period, conversion accuracy is maintained independent of variations in clock frequency. Figure 1 shows how this is done in the design of a stable, low-noise a/d system with 16-bit resolution.[2]



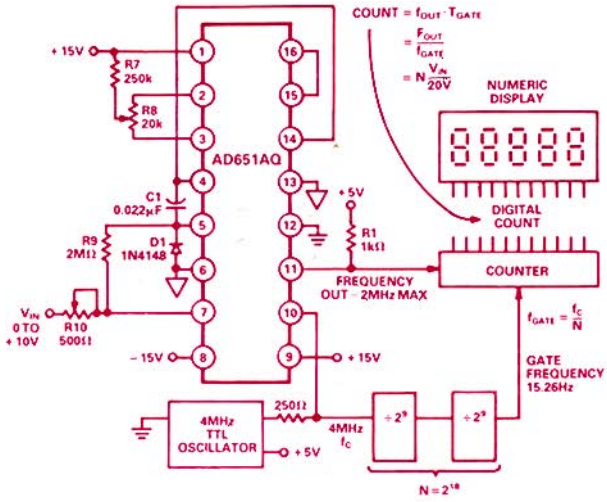


Figure 1. Synchronous VFC as high-precision a/d converter.

*Use the reply card for technical data.

[1]For more information on VFCs, see Chapter 15 of the *Analog-Digital Conversion Handbook* (1986), D. H. Sheingold, ed., published by Prentice-Hall and available from Analog Devices ($32.95).

[2]For full details, see the Analog Devices Application Note: "Analog-Digital Conversion Using Voltage-to-Frequency Converters, by Paul Klonowski.

HIGHEST-LINEARITY 16-BIT DAC IS DIGITALLY TRIMMABLE

AD1147 & AD1148 Are The Most Accurate Hybrid DACs You Can Buy

Internal 8-Bit Correction DACs Eliminate Offset- and Gain-Trim Pots

by Bill Sheppard

The AD1147 and AD1148* are hybrid 16-bit voltage-output d/a converters in a 32-pin package. Both have a pair of latched 8-bit internal DACs for adjustment of reference and offset voltage under digital control (Figure 1). The AD1147 has true 16-bit integral and differential linearity, to within ± ½ LSB (0.00076%), while the AD1148's linearity tolerances are ± 1 LSB.

Typical applications include adjustable precision reference voltage for equipment and laboratory applications, automatic test equipment, scientific instrumentation, beam positioners, and robotics.

Why correction DACs? Although the AD1147/48 have low initial offset and reference errors, the user's system often has initial offset and span errors, and they change with time and temperature. In a fixed-calibration system, the errors must be measured and the correction values computed in a calibration cycle; they must modify all subsequent data values on *each conversion instruction*. With the AD1147/48, the correction can be simply latched in to the correction DACs *once*; the actual data need not be changed.

The AD1147 and AD1148 provide two useful architectures for accomplishing this. Both accept data from a 16-bit bus and latch it into the main d/a converter. In the AD1148, the entire 16 bits are latched into a single register, while the correction bits are connected to a separate set of 8 terminals and multiplexed into the individual latched DACs for reference and offset. This allows for a separate 8-bit calibration interface, common in applications such as automatic test equipment.

In the AD1147, the correction inputs are multiplexed with the 8 least-significant bits of the 16-bit bus; Once the nominal input word is latched into the main DAC register, the 8 lesser bits can be used by the correction DACs for offset and reference adjustment.

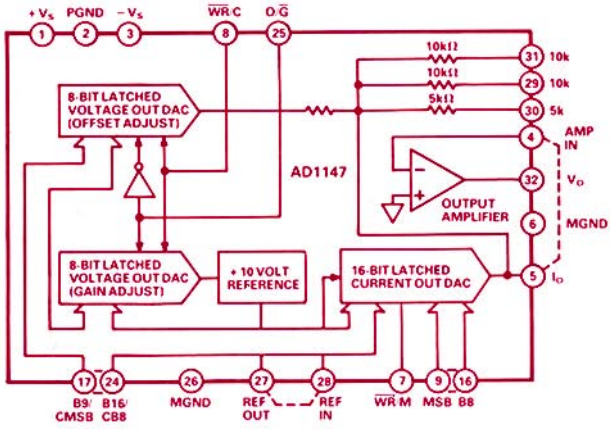
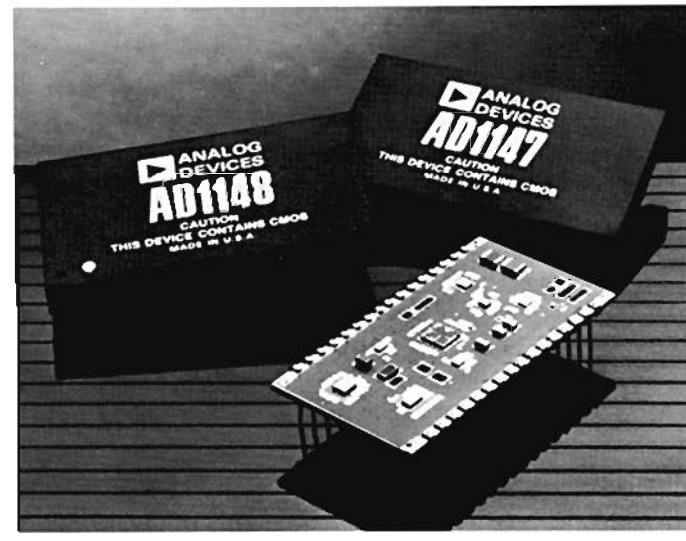


Figure 1. The AD1147 multiplexes a precision 16-bit DAC with a pair of 8-bit gain- and offset-correction DACs on a 16-bit bus.

*Use the reply card for technical data.



The AD1147 has a choice of four analog output ranges: 0 to +5 V, 0 to +10 V, ±5 V, and ±10 V—and two current ranges: 0 to −2 mA and ±1 mA (±0.5-V compliance). When it is not used as a fixed-calibratable-reference DAC, its reference input is available for use in four-quadrant multiplying DAC applications with digitally adjustable offset.

Since the AD1148's calibration bus uses up all the available pins, its analog gain options are somewhat less flexible: fixed-reference only, with fixed (digitally adjustable) ±10-volt output range. However, it does have a price advantage over the AD1147. Prices in 100s are $152 for the AD1147, $138 for the AD1148.

A typical application of the AD1147/AD1148 is in converter testing. For example, when the AD1147 is used as the source of analog voltage to test 12-bit converters, its error is less than 1/16 that of the device under test—essentially negligible. Figure 2 shows how an AD1147 would be used as a calibrated incremental voltage source in testing a 12-bit ADC under µP control. The AD1147's least-significant bits would be used as a "dither DAC" in finding transitions of the ADC, while the correction DACs compensate for the ADC's initial offset and gain errors.

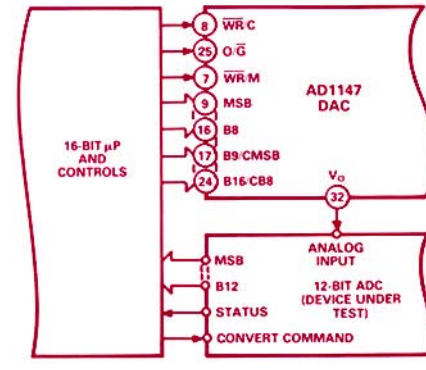


Figure 2. ADC testing.

SMALL, FAST, LOW-COST, HIGH-RESOLUTION INTEGRATING ADC

18-Bit µP-Based AD1170: Low Nonlinearity, 10-ppm Integral/4-ppm Differential Automatic Calibration, No Trims, Programmable Resolution and Integrate Time

by Bill Sheppard

The AD1170* is a microprocessor-compatible and programmable high-resolution (to18 bits) integrating a/d converter. Its small (1.24" × 2.5" × 0.55" max) modular package contains a complete microcomputer-based measurement subsystem comprising a high-linearity charge-balancing (V/F) converter, a single-chip microcomputer, and a custom CMOS controller chip (Figure 1). It requires ±15V and +5-volt power supplies, and an external 12-MHz crystal or system clock; no trim potentiometers, external references, or timing capacitors. Price in 100s is $98.

It periodically calibrates itself by reading a zero-input signal and a full-scale signal provided by an internal reference; using this data to compensate the converted data produces gain stability comparable to that of the reference—and negligible offset drift. Integral linearity error, which depends on the linearity of the charge-balancing converter, is a low ±0.001% at all resolutions.

Both resolution (7 to 22 bits) and speed (integrating time from 1 ms to 350 ms)are programmable. However, differential nonlinearity—which limits the effective resolution—is introduced by the uncertainty due to noise; hence there is a tradeoff between resolution and speed. The longer the integration time, the lower the uncertainty and the better the resolution; but also the lower the throughput. Here are some examples of effective resolution and throughput that can be achieved with the AD1170:

INTEGRATION TIME (programmable)	RESOLUTION (programmable)	THROUGHPUT RATE (conversions/s)	LINEARITY ERROR INTEGRAL (% of span)	LINEARITY ERROR DIFFERENTIAL (% of span)
1 ms	12 bits	250	±0.001%	±0.01%
16.667 ms (60 Hz)	16 bits	50	±0.001%	±0.008%
300 ms	18 bits	3	±0.001%	±0.00035%

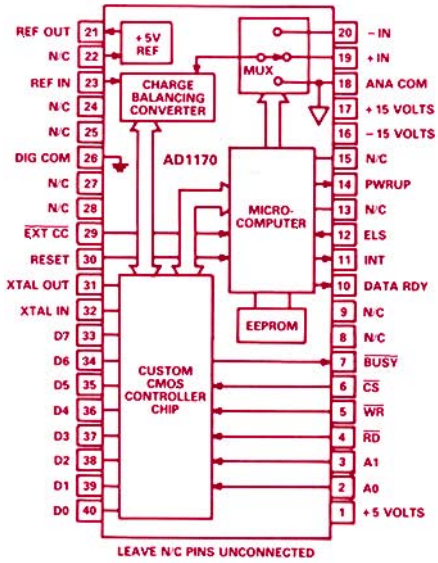
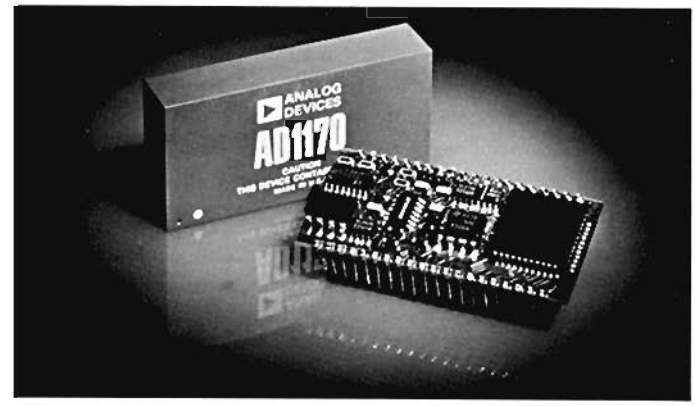


Figure 1. The AD1170 is a complete system, with a choice of external 12-MHz clock or crystal oscillator.

*Use the reply card for technical data.



Note that, in the second example, where integration time is tuned for 54-dB normal-mode rejection at 60 Hz, the throughput rate is still a hefty 50/second, a considerable improvement over dual-slope converters, which at best run at about 30 Hz. The reason is that the computer, combined with the 12-MHz clock, needs only 3 additional milliseconds to come up with the result.

In addition to automatic internal calibration, an external reference standard may be used to calibrate the internal reference upon command; the result is stored in nonvolatile memory (EEPROM). Other parameters can be saved, including arbitrary integration period, output data format, internal calibration period, and external line sample frequency. The AD1170's self-contained program routines significantly reduce the user's software, memory, and operation-time overhead.

The AD1170 interfaces to any µP-based system in either a memory-mapped or I/O-mapped mode via an 8-bit data bus. Key parameters and advanced features, such as those above, are independently programmable by simple commands sent over the bus; this enables the user to optimize system performance for a wide variety of application requirements. Figure 2 outlines a simple measurement application with the 1B31 signal conditioner.

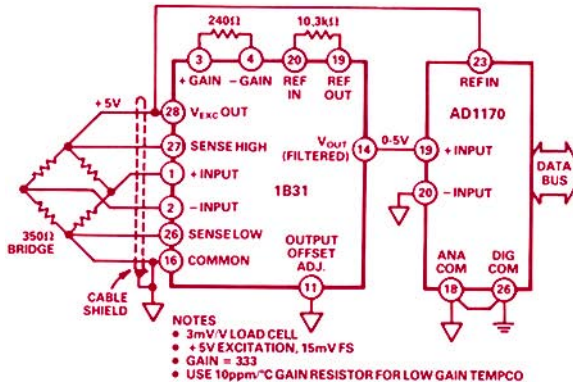


Figure 2. The AD1170 can null fixed offsets caused by bridge imbalance and normalize to full-scale in this isolated pressure-transducer data-acquisition application. Offset and full-scale correction data are computed and stored in EEPROM, eliminating repeated calibrations, pots, & software overhead.

LOW-COST HYBRID STRAIN-GAGE SIGNAL CONDITIONER

1B31 Has Adjustable Excitation, Filter, and Offset
Internal Half-Bridge Tracks to ±5 ppm/°C

by Amer Iqbal

Model 1B31* is a complete strain-gage signal conditioner that interfaces directly to a wide variety of strain gages and load cells to provide a filtered high-level output. A cost-competitive solution for in-house signal-conditioning system designs, it is ideal for OEM designers who want to use a device that can be flexibly positioned because of its compact size and has a set of default parameters that are typical for bridge transducers.

The 1B31 comprises a precision instrumentation amplifier (IA), a low-pass filter, and an adjustable excitation source in a compact 28-pin plastic double DIP (Figure 1). Its price (100s) is $45.

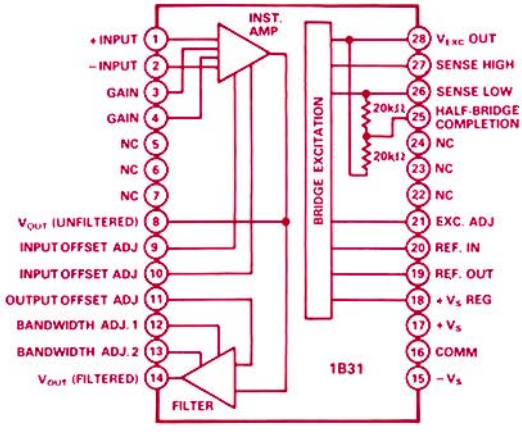


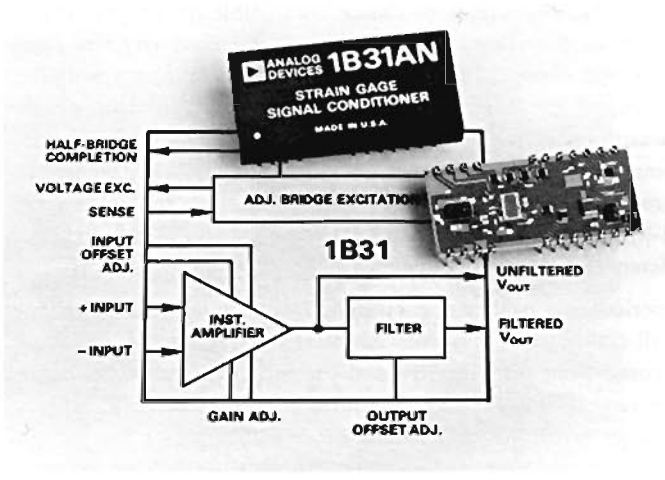
Figure 1. The 1B31 performs bridge excitation and completion, precision amplification, and pin-programmable filtering.

Instrumentation Amplifier The IA has a low offset temperature coefficient (±0.25 μV/°C at G = 1,000), low nonlinearity (±0.005% max), low input noise (0.3 μV p-p, 0.1 Hz to 10 Hz), and high common-mode rejection (140 dB min at 60 Hz, G = 1,000). Its gain is programmable from 2 V/V to 5,000 V/V with one external resistor.

Filter The two-pole low-pass filter has a preset corner (cutoff) frequency of 1 kHz, which is typical in dynamic measurements, for example, of torque and vibration. The corner frequency can be adjusted downwards (for example, to 10 Hz for low-frequency pressure measurements) by connecting two external capacitors; and it can be increased to up to 20 kHz by three external resistors. Normal-mode rejection is 40 dB per decade above the cutoff frequency.

Excitation Bridge excitation is provided by an adjustable-output regulated supply with an internal 6.8-volt reference, and a factory-set output of +10 volts. The gain of the regulator amplifier can be adjusted by an external resistor to set any output value from +4 V to +15 V. The 1B31 is rated to furnish up to 100 mA of output current at +25°C.

*Use the reply card for technical data.



Two features of the 1B31 that make it especially suitable for strain gages and load cells are *bridge-completion resistors* and *remote sensing*. An internal half-bridge, consisting of two 20-kΩ thin-film resistors that track to ±5 ppm/°C max, is available for forming a bridge with strain gages made up of two resistors in series (Figure 2). For applications where lead resistance causes significant voltage drops, the high-impedance SENSE inputs enforce the precise value of excitation voltage at the destination through feedback.

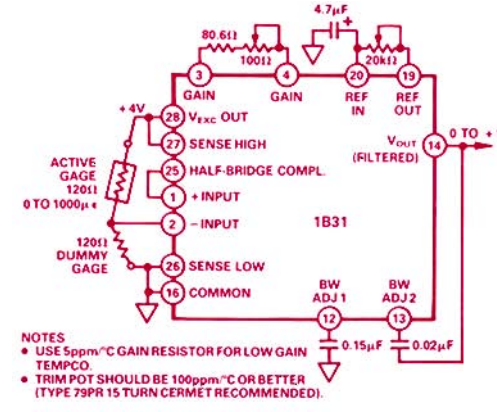


Figure 2. The internal half-bridge forms a complete bridge with the strain gage.

The 1B31 can be used in measurements of strain, torque, force, and pressure; in instrumentation, such as indicators, recorders, and controllers; and as a front end element of data-acquisition systems and microcomputer analog input/output circuitry.

Typical applications of the 1B31 are in process control systems, where the small package can in many cases be installed within the transducer housing; product and material testing, for conditioning dynamic signals from torque and vibration measurements; heavy equipment, such as cranes and forklifts, to measure hydraulic pressures and stress on steel cables; and for signal-conditioner designs employing plugin cards for personal computers, where space is at a premium.

THE EASY WAY TO INTERFACE AN LVDT TO DIGITAL

Hybrid ICs Provide Direct Transducer-to-Digital Conversion

Tracking Converters Are Amplitude-Insensitive—Have Resolutions to 16 Bits

by Daniel Denaro and John Sylvan

LVDTs (linear variable differential transformers) have been used for many years in the measurement of position—and quantities that can be represented by a linear displacement, such as pressure and force. A number of features make them nearly ideal as transducers: ruggedness, frictionless operation, long mechanical life, excellent repeatability, essentially infinite resolution, and input/output isolation. However, unlike devices that generate dc outputs directly, they have not been easy to interface to digital systems; until recently, when LVDTs were used as sensors for systems involving digital technology, kludges with demodulators, filters, preamplifiers, and general-purpose a/d converters were needed.

The situation has radically changed, thanks to the advent of direct LVDT-to-digital converters, employing tracking loops, in hybrid IC packages. The LVDT, and its close relative, the RVDT (R = "rotary," for angular measurements), can now be easily and accurately interfaced as inputs for digital control systems. In this article, we review the LVDT briefly for the benefit of readers unfamiliar with them, and then discuss recent advances in the technology.

WHAT IS AN LVDT?

A linear variable differential transformer is an electromechanical device consisting of two components: a hollow cylindrical *body* containing axial windings—usually a primary and two symmetrically disposed secondaries—and a rod-shaped *core*, which is free to move longitudinally within the coil (Figure 1). Since no part of the core needs to touch the body (and they can in fact be attached to different physical entities), the LVDT is friction-free.

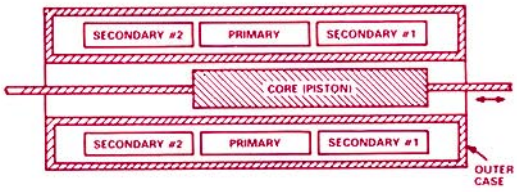
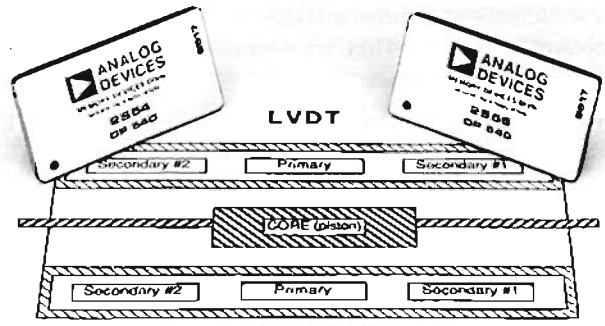


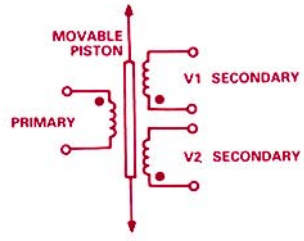
Figure 1. Cross-section of an LVDT.

An ac excitation/reference signal (typically from 50 Hz to 10 kHz, and usually specified at 2.5 kHz), applied to the primary, induces voltages in the secondary windings. When the core (or piston) is centered between the two secondaries, the voltages induced in both are equal; if they are connected in series opposing (Figure 2), the terminal voltage will be zero. As the core (or piston) moves in the direction of secondary 1, its voltage increases, and the voltage on secondary 2 decreases; thus the net terminal voltage ($V_1 - V_2$) will be of the same polarity as (in phase with) the reference. If the core moves in the opposite direction, $V_1 - V_2$ will be of opposite polarity (180° out of phase).

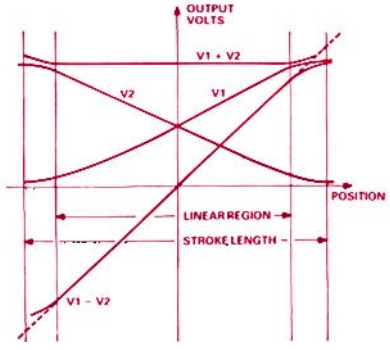
Thus, as the core moves along the axis, the output voltage starts at one polarity, decreases through zero, then increases in the opposite polarity, smoothly and continuously (Figure 2b). Devices are designed for output voltage linear about zero, typically to within

*Use the reply card for technical data.





a. Relationship of windings.



b. Outputs of individual windings and their sum & difference, as a function of position.

Figure 2. Equivalent circuit of LVDT.

±0.25% over a specified nominal linear range of travel; linearity may worsen beyond this range, but often not significantly—nonlinearity is generally specified for up to 150% of the nominal linear range. For a selection of typical LVDTs, the nominal linear range can be from ±0.05 inches to ±10 inches (±1.25 mm to ±250 mm); corresponding body lengths range from 1" to 30".

Sensitivity, expressed in millivolts out per volt of excitation per 0.001" (or per mm), is generally inverse with full-scale displacement; the range corresponding to the above range of displacements is from 6.3 mV/V/mil (250 mV/V/mm) to 0.08 (3.0).[1] From this, it is easy to see that LVDTs, though robust mechanically and

[1]Data from Schaevitz Engineering (Camden, NJ 08101) technical bulletin 1002C. Schaevitz also publishes a *Handbook of Measurement and Control*, "generally regarded as the authoritative treatise on the theory and application of LVDTs."

capable of high reliability, produce low-voltage outputs that require care in wiring—and amplification—in order to realize the benefits of their potentially high resolution.

WHERE ARE THEY USED?

LVDTs are very common transducers. In measurement and control, they are widely used for direct measurement of displacements from microinches to several feet. They are found in gauging and metrology systems. They are fitted on aircraft control surfaces and control levers; in jet engines they indicate vane and valve position. They are often found buried in dams, roads, and bridges, in order to monitor movement. They are even used in cash dispensers to measure banknote thickness.

Many other transducers use LVDTs internally, for example load cells and pressure transducers. They are also often combined with hydraulic actuators. In electronics, they are used in automatic wire bonders and inspection equipment.

INTERFACING THE LVDT TO DATA-ACQUISITION SYSTEMS

The transducer is essentially a transformer; therefore it must be driven from an ac source; and since the output may be of either polarity with respect to the reference, a phase-sensitive demodulator is necessary for a dc output.

In the past, LVDTs have been connected to dedicated instruments that provide position readout. However, computer-based data-acquisition systems are replacing specialized instruments in many applications. Typical computer systems use cards connected to a standard computer bus; since these cards are not very large, the electronic circuitry associated with the LVDT must be compact and introduce a minimum of additional error. Newly available hybrid circuits that perform the entire signal-conditioning and conversion function stably and accurately also conserve board area.

The Traditional Solution

Figure 3 outlines a typical system to provide signal-conditioning and conversion for an LVDT. In this instance, the LVDT primary is driven by an oscillator and the output is amplified, synchronously demodulated and filtered to provide a dc input to the a/d converter. If the signal calls for high resolution and involves rapid motion, a sample/hold will be needed; and if more than one channel is to be converted, a multiplexer will be necessary.

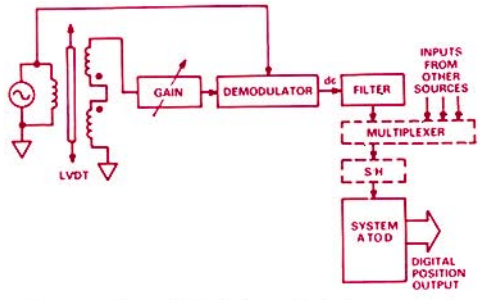


Figure 3. Conventional LVDT-to-digital conversion system.

Since the output depends on the amplitude of the oscillator voltage, perhaps the most serious drawback to this conversion method is the requirement for the oscillator voltage to be stable with time, temperature, and variations in load impedance. For example, if 16-bit resolution is required, a 1-volt oscillator output would have to be stable to within 60 microvolts for a repeatability of 1 LSB. Maintaining stability of the oscillator with time is itself not easy; the problem is further exacerbated by the variation of the load impedance of the LVDT (possibly at a remote location) with temperature. Clearly, it would be helpful if the measurement could be performed ratiometrically.

Another potentially serious problem is noise induced in the signal lines, especially if the transducer is at some distance from the conversion electronics. In addition to noise, gain or offset changes in the circuitry following the phase-sensitive demodulator will directly affect the output code. It is highly desirable for the conversion process to include integration, to filter out noise, and for the demodulation and conversion to be combined in a single operation, to eliminate interconnection-dependent error sources.

The Tracking-Converter Solution

Figure 4 is a block diagram of the signal conditioning and conversion scheme employed in the Analog Devices 2S54 and 2S56* 14- and 16-bit LVDT/RVDT-to-digital converters. Readers of this Journal will readily observe the basic similarity between these converters and resolver-to-digital converters, such as the 1S64*[2]; in fact, proven hybrid-IC tracking-converter technology is the key to the size, performance, and cost advantages of the 2S54/56.

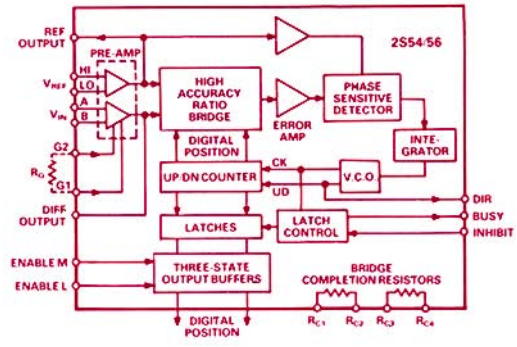


Figure 4. Block diagram of 2S56 LVDT-to-digital converter family.

Conversion is produced by a tracking feedback loop. Here's how it works: the reference signal and the difference signal from the LVDT are pre-amplified/buffered, and their ratio is compared with an estimate of the position, furnished by the digital output of an up-down counter. The error between this estimate and the actual ratio is detected and filtered, using an analog integrator. The dc output of the integrator drives a voltage-controlled oscillator, which clocks a counter either up or down, depending on the polarity of the integrator output, at a rate proportional to its magnitude. The counter output, as mentioned above, is the position estimate; if it is smaller than the input ratio, the error will cause the counter to count up - if it is larger, the counter will count down.

In the steady state (estimate = ratio), with the LVDT not moving, the counter is not counting, i.e., the input to the VCO is zero. In order for the integrator output to be constant (zero, in this case), its input, too, must be zero—and this can occur only when the estimate is equal to the ratio. It is not hard to see that this loop is a *tracking* loop—if there is any change in the input ratio, there is an error that causes the VCO to drive the counter to the new value to eliminate the error.

Not only does it track, it is a *Type 2 (second-order) tracking loop* (two integrations), which will also maintain zero *velocity* error in the steady state. Consider the case where the LVDT position

[2]"Resolver/Digital with Accurate Tachometric Output," by Paul Nickson and Geoffrey Boyes, *Analog Dialogue* 18-3, 1984 (16-17).

(measured by the input ratio) is changing at a constant velocity. In order to keep the velocity error at zero, the counter must be counting at a steady rate; this means that the VCO input must be constant, i.e., the integrator output must be constant. But it can be constant only if the integrator's input (i.e., the position error) is zero. Thus there is no position error or velocity error if the velocity is constant; dynamic errors can occur only for non-zero *acceleration*.

Because the loop tracks the *ratio* of input to reference, the conversion is not sensitive to changes in the actual magnitude of the reference signal that drives the LVDT. This has the great advantage of making the converter insensitive to oscillator amplitude drift and voltage drops in the signal lines. Because of the integrations, the converter tracks the average value of the ratio when there is high-frequency noise induced in the signal lines, making the converter less sensitive to noisy environments.

Quadrature signals, a source of null error in LVDT systems, do not introduce error in the tracking loop, because they show up as ac error signals from the phase detector and are averaged out. The low-noise amplifiers employed here make it possible to use larger, less-sensitive transducers over a smaller, more-linear portion of their range, without substantially increased errors due to noise. Transducer nonlinearity of the order of 0.05% can thus be achieved.

The loop tracks the signal continuously, so that the digital output of the counter is always either at the correct position value (within 1 count) or en route to it (when the system is subjected to acceleration). The accumulated count is latched, and the output from the latches is provided via two sets of three-state output buffers, which can provide a two-byte output to an 8-bit bus or a broadside output to a 16-bit bus, depending on when they are enabled. Busy and Inhibit lines make it possible to update the bus synchronously without disturbing the loop's asynchronous operation.

The continuous tracking conversion does not need a sample-hold for tracking speeds below the specified slewing rate. Multiplexing can be performed digitally on the bus, using one converter for each channel (with the virtues of availability and simplicity). If cost is an important consideration, the inputs of several LVDTs can be multiplexed on one converter, but it is necessary to wait for the loop to settle (35-60 ms) each time before reading out the data.

2S54/56 CONVERTER PERFORMANCE

As the block diagram indicates, gain can be programmed over a range of 1 to 10 V/V with an external resistor, to accommodate a wide range of transformation ratios and operating stroke lengths. Over the operating temperature range, and a 10% variation of reference amplitude, the basic gain accuracy of the converter is 0.05% max (gain = 1), and maximum integral linearity error is 0.02% of full scale. This level of accuracy would be quite difficult to achieve and maintain in a conventional conversion system.

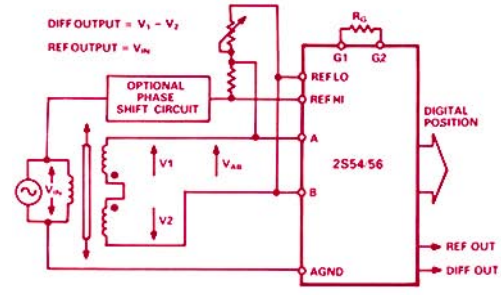
Dynamically, large-signal settling time is 160 ms (2S56) and 70 ms (2S54) for a full-scale step, and the maximum tracking (slewing) rate for both is 360 LSBs per millisecond.

ALTERNATIVE CONNECTION METHODS

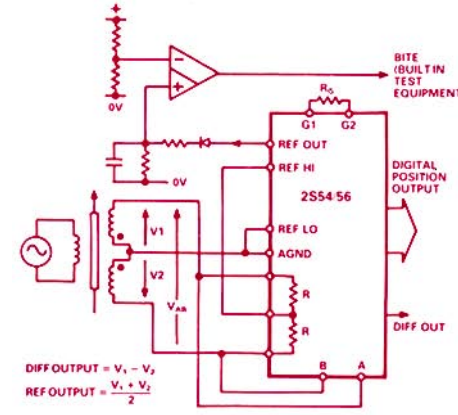
The availability of input amplifiers with fully differential inputs and variable signal gain, and an auxiliary uncommitted matched precision resistor pair (0.02% ratio match and 2 ppm/°C tracking tempco), makes the converter suitable for a wide variety of connection schemes. For example, Figure 5a shows a connection for a three-winding LVDT. The ac excitation is applied between REF HI and AGND, the signal is applied between differential inputs A & B, and provision is included for input gain adjustment to compensate for the LVDT's transformation ratio—which is a function of carrier frequency. Conversion accuracy is only slightly affected by transducer phase shift, which can in any event be corrected for.

In Figure 5b, the LVDT is again supplied from the primary side, but the converter reference is the secondary common-mode signal (see Figure 3) thus representing the primary voltage, but without the errors due to primary impedance and transformation ratio. It is derived, at the division point of the precision resistors, as ½ the sum of the voltages developed by the secondary windings. If this signal has constant amplitude with piston displacement, the system will have high resolution and exceptional stability, and be insensitive to temperature, frequency, and phase-shift effects.

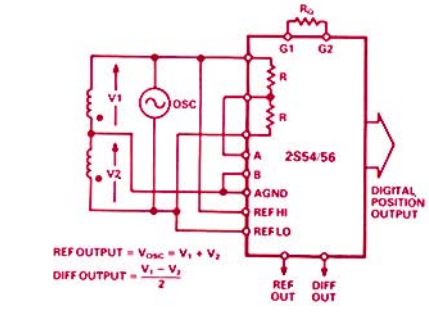
Figure 5c shows yet another scheme, in which only a pair of (secondary) windings are available, an autotransformer connection. The coils are connected in series aiding, and the excitation is applied across them. In this case, the difference is obtained by using the precision resistors in a bridge configuration to obtain a net signal equal to one-half the difference of the voltages.



a. Primary as reference ("two-wire system").



b. Derived reference for high stability. ("three/four-wire LVDT")

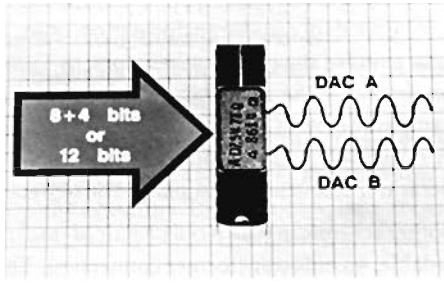


c. Eliminating the primary (autotransformer connection—"half-bridge LVDT").

Figure 5. Comparison of connection modes.

DUAL 12-BIT DACS

AD7537/7547 in 0.3" DIPs For 8/16-Bit Data Buses



The AD7537 and AD7547 are 12-bit CMOS dual 4-quadrant multiplying d/a converters in compact 0.3"-wide 24-pin "skinny" DIPs. The AD7537* is double buffered and designed to interface with 8-bit buses in two right-justified bytes (4+8); the AD7547* accepts full 12-bit digital inputs, interfacing easily with 16-bit buses. Both types are manufactured using the Analog Devices linear-compatible CMOS (LC^2MOS) process.

The dual-DAC construction occupies about one-half the area required by two separate 12-bit DACs; an added benefit is ladder-resistance matching to within 1.0% max and precise temperature tracking. Typical applications include automatic test equipment, programmable filters, stereophonic audio systems, synchro applications, process control, and designs with tight space constraints that would not permit two discrete devices.

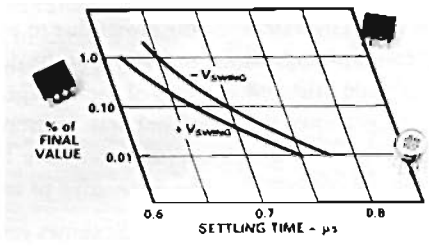
Both DACs operate on a single +12 to +15-volt supply with only 30 mW max dissipation (+15-V supply). Each DAC has its own reference input. Typical channel-to-channel isolation is −84 dB at 10 kHz, while digital crosstalk is 7 mV-μs. All grades guarantee monotonic behavior over temperature. Maximum relative accuracy error is ±1 LSB for the AQ, JN, and SQ grades (both types) and ± ½ LSB for the KN, LN, TQ, BQ, CQ, and UQ grades.

The AD7537 and AD7547 are both available in plastic packages, for operation over the 0°C to +70°C temperature range, and in hermetically sealed ceramic or Cerdip packages, for operation over the −25°C to +85°C and −55°to +125°C temperature ranges. Prices start at $14.50 (JN grade in 100s).

*Use the reply card for technical data.

HIGHEST-PERFORMING LOW-COST BIFET OP AMPS

AD711/712 for Speed; AD548/648 for Low I_Q, I_b Singles and Duals; Range of Packages, Performance



The AD548* and AD711* FET-input op amps, their various temperature- and performance grades, and their dual-amplifier equivalents (types AD648* and AD712*) form a complete family of moderately priced high-performance amplifiers.

The AD548(648) family draw only 200 μA of quiescent supply current per amplifier, with low bias current as an added bonus. They are best buys for low-power applications calling for superior dc and ac performance in (e.g.) battery operation.

The AD711(712) family are fast, typically settling to 0.01% in less than 1 μs (1.8 μs max), with minimum slew rates approaching 20 V/μs. Yet dc performance is not spared; offsets and drift are comparable to those of the AD548 family. Compared below are specs of the lowest-priced miniDIP-packaged grades. Premium grades, industrial and military temperature ranges, and hermetic and ceramic packages are also available.

	AD548(648 dual)		AD711(712 dual))	
	JN	KN	JN	KN
Offset (mV max)	2	0.5(1)	2(3)	0.5(1)
Offset drift (μV/°C max)	20	5(10)	20	10
Bias current (pA max)	20	10	50(75)	50(75)
Gain (V/mV min)	150	150:10V/5kΩ	150	200:10V/2kΩ
Slewing rate (V/μs min)	1	1	16	18
0.01% Settling time (μs)	8typ	8typ	1.8max	1.8max
Quiescent current(mA max)	0.2(0.4)	0.2(0.4)	3.4(6.8)	3.0(6.0)
Price (100s)	$.75(1.25)	$2.60(3.90)	$.80(1.25)	$1.90(3.75)

AD202/AD204 LINE OF ISOLATORS ENHANCED

K Versions offer ±2 kV Isolation, ±0.025% Nonlinearity Low-Profile DIP Packages Join Earlier SIPs: JN, KN

The revolutionary AD202/AD204* family of compact low-cost high-performance isolators was introduced in the last issue (Analog Dialogue 20-1). Originally packaged in high-density (4 to the inch) single-in-line packages, they are now available in a 0.35"-high (max) DIP package; in addition, they are joined by an increased-performance K grade with twice the linearity and CMV performance, and 1/3 the initial voltage offset.

All types have gain from 1-100 V/V, CMR of 130 dB (G = 100), 2 μA max rms leakage current, 10(1 + 1/G) μV/°C offset drift (RTI), and rated performance from 0°C to 70°C. AD202 is powered from dc, while up to 32 AD204s can run from a common AD246 25-kHz clock oscillator, for a per-channel saving in cost, plus wider bandwidth and more isolated power. Performance differences are summarized in the table.

	AD204J	AD204K	AD202J	AD202K
Power requirement	15 V p-p @ 25 kHz (from AD246 clock)		+15 V–5 mA dc	
Nonlinearity (max)	±0.05%	±0.025%	±0.05%	±0.025%
Max CMV in/out (60 Hz rms)	750 V	1,500 V	750 V	1,500 V
±DC (peak)	1,000 V	2,000 V	1,000 V	2,000 V
Bandwidth (G = 1-50 V/V)	5 kHz	5 kHz	2 kHz	2 kHz
V_{os} RTI max x(1 + 1/G)	±15 mV	±5 mV	±15 mV	±5 mV
Output resistance (ohms)	3 k	3 k	7 k	7 k
Isolated power out @ 7.5 V	2 mA	2 mA	400 μA	400 μA
Price, either package (100s)	$25	$29	$28	$32

HIGH-RESOLUTION PROGRAMMABLE-GAIN DAS

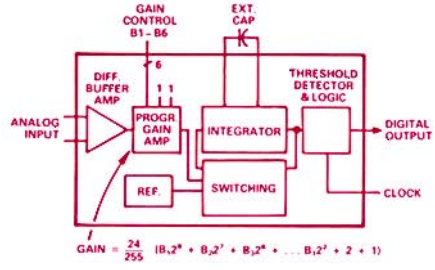
AD367 Has 15-Bit Resolution, 85:1 Gain Range

Voltage-to-Pulsewidth Conversion, External Counter

The AD367* is a data-acquisition front end with 21 bits of dynamic range in a compact 24-pin hermetic dual in-line package. It provides the essential analog circuitry for use wherever high accuracy is needed over a wide dynamic range; examples in laboratory instrumentation include blood analyzers, chromatographs, spectrographs, and other chemical-analysis instruments.

The AD367 comprises a differential-input (90-dB CMR) unity-gain buffer amplifier, a digitally programmable-gain amplifier with 64 gain values, and the front end of a dual-slope a/d converter (i.e., an analog to pulsewidth converter), with a −10-V precision reference. The output time interval, proportional to the input, can gate an external counter or μP from the end of the first (signal) integration to the instant at which the returning integrator output crosses the threshold. The user controls integrating time and digital resolution through choice of integrating capacitor and counter.

PGA gains range from 24 to 0.2824, in steps of 96/255; thus gain can be set for rated resolution of full-scale signals as small as 0.42 V. A shorting switch permits software calibration of offset. Integral linearity error is 0.003% max FSR, or 1 LSB of 15 bits. Operation is specified from 0°C to +70°C. Price in 100s is $105.



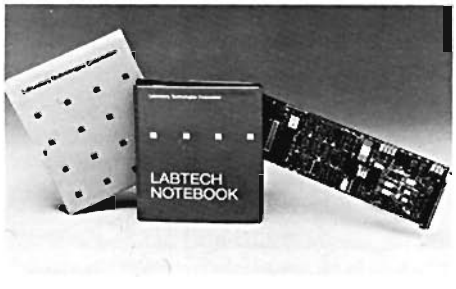
PC DATA-ACQUISITION & PROCESSING

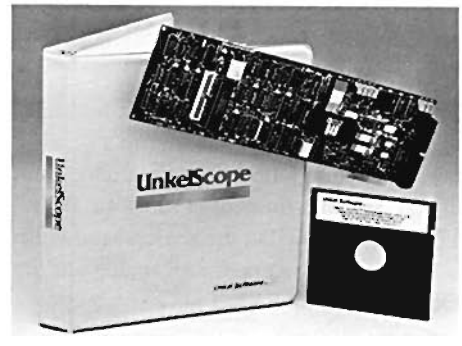
Use ADI's RTI-800 Series Boards and Commercial Software

Available from ADI: Unkelscope and Labtech Notebook

RTI-800 series plug-in data-acquisition boards for the IBM PC work with Labtech Notebook, (Laboratory Technologies Corp.) and Unkelscope (Unkel Software, Inc.) application software. Both packages are available directly from ADI.

Labtech Notebook, designed for data acquisition and control, performs such functions as P-I-D control, alarms, data logging, digital I/O control—and it provides graphics and analytical routines. It is available as AC1530.* Price: $895.





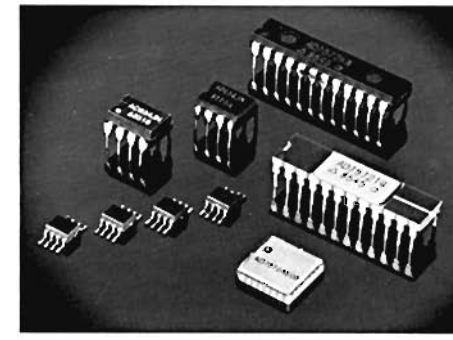
Unkelscope turns the PC into an oscilloscope for real-time data acquisition. It displays, stores, performs processing (e.g., low-pass and high-pass filters, FFTs, etc.) Ask for AC1507.* Price: $549.

Both operate with RTI-800* analog input board (16 analog & digital channels, 3 frequency timer channels) and RTI-815* multifunction board (same, but with two analog output channels). The boards are priced at $850 and $1,095 (1s).

*Use the reply card for technical data.

LCCs, PLCCs, & SOICs

Converter ICs Available in Surface-Mount Packages



Data converters and other IC products packaged for surface mounting are available from Analog Devices, with more coming. Some customers have already designed them into major new products. All popular types will become available in surface-mount packages during the coming months.

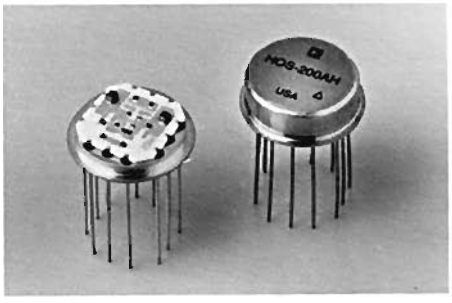
Why surface mounted devices? They save space; converters in PLCCs feature accuracy, speed, and resolution like those of their DIP-packaged counterparts, but they occupy only ¼ to ½ the space. They can reduce manufacturing costs through simpler, higher density, and double-sided boards, more-easily automated assembly and testing. They can improve electrical performance through closer spacing and shorter in-package lead lengths, with lower capacitance, inductance, and transit times.

Surface-mount packages now available or in the works include data converters in 20- or 28-terminal LCCs (leadless chip carriers) and PLCCs (plastic leaded chip carriers); coming are linear circuits in these packages and also SOICs (small-outline ICs).

Available products include VFCs, DACs (8-, 10-, 12-, 14-bit, some duals and quads) and ADCs (8-, 10-, and 12-bit—conversion times from 1.5 to 100 μs). Typical A/D ICs include the AD7572, a 5-μs 12-bit ADC with on-chip reference, the industry-standard AD574, and the 500-kHz AD654 VFC (in SOIC). DACs include the AD7549, a dual 12-bit multiplying DAC, and the AD667 complete 12-bit DAC. LCC and PLCC parts are slightly more expensive than DIP-packaged devices; prices, availability, and performance specifications vary according to device and grade.

BUFFER AMPLIFIER

HOS-200: G = 1, 200-MHz BW
1,000 V/μs min Slew Rate

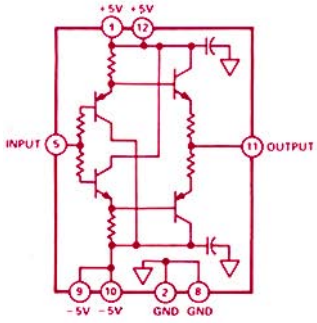


The HOS-200* is a wide-bandwidth high-speed voltage-follower buffer designed to provide high current drive at frequencies from dc to over 200 MHz.

Its applications include video impedance transformations, buffering a/d converters and comparators, and functioning as a high-speed line driver for either 50- or 75-ohm cables. It can be used as a yoke driver in high-resolution CRT display systems and raster-scan systems. Used inside-the-loop, it stably enhances the output capability of monolithic op amps.

Typical environments where it would be found include portable or remote equipment operating with low supply voltages, systems in which available (battery) power is at a premium, digital systems which include only +5V and −5.2-V power.

Operating from ±5-volt power supplies, it delivers high output current (100 mA continuous, 250 mA peak), with a 3-dB bandwidth of 200 MHz and 1,500 V/μs typical (1,000 min) slew rate. Housed in a hermetic TO-8 can, it is available in A (−25°C to +85°C) and S (−55°C to +125°C) grades. Prices (100) are $12.60 and $17.00.



*Use the reply card for technical data.

COMPLETE 12-BIT, 5-MHz ADC ON EUROCARD

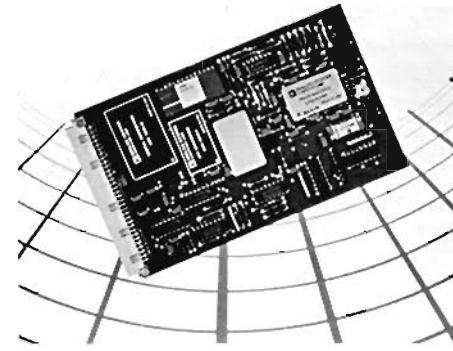
CAV-1205 Has T/H, A/D Encoder, Registers, Timing
Subranging-Type Converter Is TTL-Compatible

The CAV-1205* is a 12-bit a/d converter with 5-MHz throughput. Designed for a single-width Eurocard, it includes a track-hold, encoder, output registers, and all of the necessary timing circuits to generate 12 bits of digital output data.

Its design is based on the Level 2 requirements for printed-circuit board subunits; Like the CAV-1202 converter (*Dialogue* 20-1)—with which it is pin-compatible—it meets the physical standards established by DIN 41494, IEC 48D (sec)12. Two-step subranging with digital error correction is used for 12-bit accuracy.

Applications for the CAV-1205 include radar systems, medical instruments, transient analyzers, and other designs where high speed, high resolution, and small size are required.

Minimum in-band harmonics, generated at a 5-MHz encode rate, are 70 dB below full scale with a 500-kHz to 2.5-MHz input signal. Minimum signal-to-noise at 540 kHz input is 65 dB, decreasing to 62 dB at 2.3 MHz. With full-scale analog input ranges of ±1.024 or ±2.048 volts, the converter is guaranteed monotonic over temperature, 0°C to +70°C.



Dimensions are 167 mm × 100 mm × 13 mm. Specified power supplies are ±15 V, +5 V, and −5.2 V. Price is $1,795 (1-4).

12-BIT M-DAC WITH 110-ns SETTLING TIME

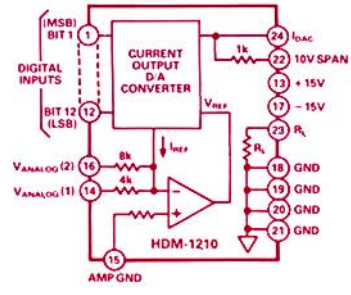
Current-Output HDM-1210 Delivers 10.24 mA Full-Scale
Guaranteed Monotonic over Temperature

The HDM-1210* is a fast 12-bit multiplying digital-to-analog converter in a ceramic or metal hybrid DIP. It features a maximum digital settling time of 110 ns to 0.1%, 170 ns to to 0.025%; the analog bandwidth is 10 MHz, with a maximum analog settling time of 120 ns to ±1% FS.

The HDM-1210 is a one-quadrant device, used in applications where the designer needs to multiply an analog input, or the sum of two inputs, by a scale factor which can be established with a digital input word. With two HDM-1210's, two- and four-quadrant multiplication can be performed with proper polarity.

The analog signal can be a sine wave, triangular wave, or an arbitrary waveform. The output is a digitally scaled version of the input. Applications include waveform generation, CRT display, vector generation, and MHz-rate analog and digital attenuation.

The HDM-1210 is guaranteed monotonic over temperature; its maximum gain error is 0.5% of full scale. Maximum differential and integral linearity errors are ±1 LSB. Two temperature ranges are available, −25°C to +85°C (BD) and −55°C to +125°C (SD and SDB). Prices start at $144 (100s).



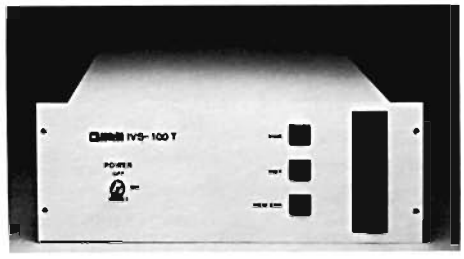
FAST, USER-REPROGRAMMABLE OCR READER

SPEED READER™: 45 Characters/s, 99.9% Accuracy
Reads Laser-Etched Code on Semiconductors

The fast SPEED READER™* optical character recognition (OCR†) system reads up to 45 characters per second with 99.9% accuracy in production applications. It can be field-programmed within hours to identify characters of a standard font.

The system excels in semiconductor and electronics manufacturing, where it can read the laser-etched code on semiconductor wafers, associate test results with ID numbers on DUTs, and read IDs of circuit boards and components.

SPEED READER easily handles variations in focus, lighting, and background color and can read characters accurately, even when poorly lettered or lit—as in some factories.



It recognizes 256 levels of gray-scale and has 512 × 512-pixel resolution. Menu-driven programming on-site minimizes loss of time and money.

Included are CPU, frame grabber, software, disk drive, and communications. Options include monitor, terminal, keyboard, and small, reliable, CCD camera.

ANALOG OUTPUT MODULE FOR μMAC-5000

QMXAO Provides 2-4 Channels of Analog Output
1,000-V Isolation per Channel, V or I Outputs

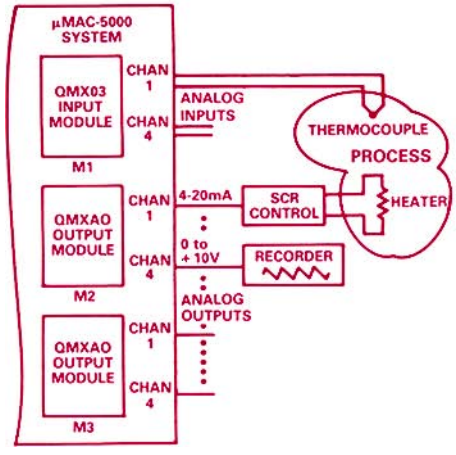
The QMXAO* is a two-channel analog output module that provides isolated voltage and current outputs in a μMAC-5000 system. Because a QMXAO can be plugged into any QMX *input* socket on the master board or the μMAC4010 expander board, an output expansion board is not needed to handle output functions.

Small-scale analog control applications for the μMAC-5000 with the QMXAO include low-cost multi-loop control, proportional control, furnace and oven control. The QMXAO (AOTX in software) may be used to position valves, operate set-point controllers, and to drive actuators, recorders, and indicators.

The QMXAO's d/a converters have 12-bit resolution and simultaneous voltage (0-10V or −10V to +10V) and current (0-20 mA or 4-20 mA) outputs, with 1,000-volt isolation.

In the voltage mode, the QMXAO provides enough current to be used as a programmable sensor excitation source.

Up to three QMXAOs may be used, for a total of 6 output channels. It may be ordered as an accessory or furnished with the board. Price: $295.

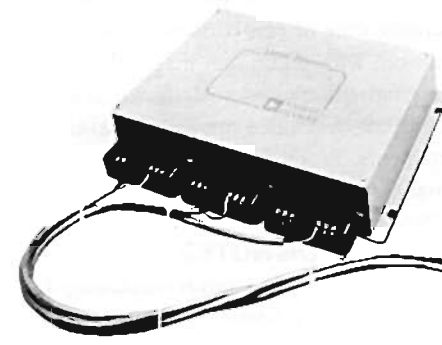


*Use the reply card for more information.

†OCR vs. bar code: OCR reads characters, not bars. Advantages: Human-readable, one set of characters will do; physically compact; carries more information; gray scale ignores poor contrast or lighting and no contact; non-standard fonts usable.

μMAC-5000 RUNS C

AC1836: Software Tools for New Programming Option



AC1836* is a library of software tools to allow users to program μMAC-5000 measurement-and-control systems in the C programming language. C is a popular, high-level transportable language which runs 2 to 5 times as fast as μMACBASIC.

The library includes program development tools, real-time interrupt service routines, and drivers for analog I/O, digital I/O, counting, timing, communications, and failure detection. It also includes routines for transferring executable code from an IBM PC, used as a C development system, to the μMAC-5000.

Programming options for the μMAC-5000 now include μMACBASIC, the standard language shipped with every system, and C. μMACBASIC, while highly integrated into the system design and easy to learn and use—has suboptimum performance. C is faster, occupies less space in memory (leaving more room for user programs) and is transportable from system to system.

μMACBASIC is recommended for programmers who are new or have simple program needs; C is intended for sophisticated users and OEMs who use many types of systems and want to standardize program development.

To program a μMAC-5000 in C, the user needs Manx Aztec C. The C libraries include a PROM for the μMAC-5000 board, an IBM-compatible disk containing libraries for I/O routines, a public domain file transfer program, and a manual. Price is $495.

Worth Reading

FREE APPLICATION GUIDE

RMS-to-DC Conversion Application Guide, 2nd Edition is now available upon request. 76 pages, with more than 80 illustrative circuits and diagrams, covering rms-to-dc conversion theory and practice. Topics include basic design considerations, rms application circuits, testing rms converters, and input buffer requirements. In addition there are two computer program listings for determining computational errors, output ripple, and 1% settling time of rms converters. An improved version of the first edition, with additional material, including detailed coverage of external offset- and scale-factor trimming, rms noise measurement, µP-controlled rms functional circuits, and rms power measurements. Products covered include ADI's family of monolithic analog rms-to-dc converters: AD536A, AD636, and AD637.

APPLICATION NOTES

"Analog-to-Digital Conversion Using Voltage-to-Frequency Converters," by Paul Klonowski (8 pages).

"Analog Panning Circuit Provides Almost Constant Output Power," by John Wynne (4 pages).

"Bipolar Operation with the AD7572," by John Reidy (4 pages).

"14-Bit DACs Maintain High Performance over Extended Temperature Range," by Mike Curtin & Robert Stakelum (6 pages).

"Interfacing the AD7572 to High-Speed DSP Processors," by John Reidy (4 pages).

"Low-Cost, Two-Chip Voltage-Controlled Amplifier and Video Switch," by Charles Kitchin, Andrew Wheeler, and Ken Weigel (6 pages).

"Temperature Measurement System to 10-Bit Resolution Using the AD7571 and the AD594/595," by John Reidy (4 pages).

"12-Bit Analog I/O Port Uses AD7549 and 8051 Microcomputer," by Mike Curtin (4 pages).

FREE NEWSLETTER FOR THE MILITARY/AVIONICS INDUSTRY

Analog Briefings, Vol. 2 – numbers 1 and 2, are available upon request. Free subscriptions are available through your local Analog Devices sales engineer. Number 2-1 discusses MIL-STD-883C, Notice 4, and MIL-M-38510F, Amendment 1; MIL-STD-1772 Certification—Substrate Fabrication; QPL status for analog multipliers AD532 and AD534; 883C products in surface-mount packages; and 17 new military products, including CMOS ADCs and single & dual DACs, bipolar ADCs and analog computational units. Number 2-2 covers Computer Lab Division's MIL-STD-1772 certification; MIL-M-38510 certification for our CMOS facility in Limerick, Ireland and QPL for their AD7520; military drawing system to replace DESC drawing system; JAN product status; 883 version of the AD651; and *Military Products Databook* errata.

µMAC-6000 BROCHURE (see pages 10-13)

Free brochure available, with specifications; an excellent introduction to the µMAC-6000's features, using color photography. Next best thing to having your hands on one.

MORE AUTHORS (Continued from page 2)

Paul Klonowski (page 15) is a Product Marketing Engineer in the Converter Group at Analog Devices Semiconductor (ADS), Wilmington, Mass. He was graduated from the University of Cincinnati in 1984 with a BSEE. Before joining Marketing, he was an Applications Engineer with ADI's Components Applications Group.

Mike Nell (page 3) is a Marketing Specialist in the Digital Signal Processing Division at Analog Devices. He has BS degrees in electrical and mechanical engineering and MS degrees in EE and management from M.I.T. Before joining DSP, he was a Strategy and Systems Analyst in Corporate Strategic Information. He has also worked at Texas Instruments as a Strategic Planning Analyst and at Draper Laboratories as a Research Assistant.

Bill Schweber is a Senior Marketing Engineer in ADI's Industrial Automation Division, with responsibility for the µMAC product line. He has a BSEE from Columbia University and an MSEE from the University of Massachusetts and has been with Analog Devices since 1980 in applications and marketing roles. Before that, he designed µP-based controls for materials-testing equipment. He has written two textbooks for McGraw-Hill.

Bill Sheppard (pages 16, 17) is a Marketing Engineer in the Interface Products Division (IPD) of Analog Devices. Since joining ADI in 1969, he has held positions as Test Supervisor and Quality-Control Supervisor. In his present position, he supports IPD's High-Resolution Converter product line. He received his ASET at Brevard Junior College in Cocoa, Florida. His hobbies include golf, fishing, and high-performance Buicks.

John Sylvan (page 19), Senior Technical Publicity Associate, has been with Analog Devices since his graduation from Colby College in 1980. Working in the Technical Communications Department for the last few years, John has written numerous articles on Analog Devices computer- and integrated-circuit technologies.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE

Volume 20, Number 1, 1986 – 28 Pages

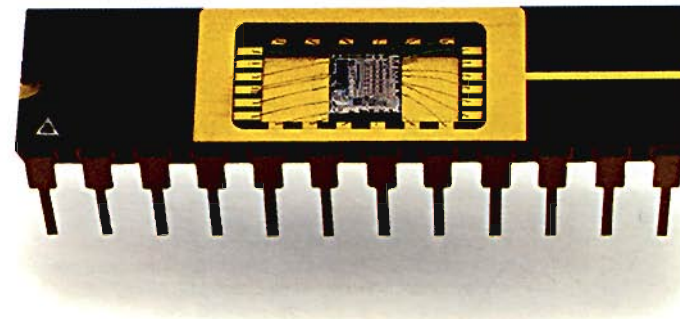
PRODUCT NOTES . . . Third-party development support exists for Word-Slice™ (ADSP-1401 and -1410) and floating-point (ADSP-3210 and -3220) DSP integrated circuits, in the form of meta-assembler and control store emulation from Step Engineering, HiLevel Technology, and Hewlett-Packard – and more is on the way; also Microtec Research has recently included definition files for the above parts in both its meta-assemblers . . . Specs for the ADSP-1010A 16 x 16-bit 1.5-micron CMOS Multiplier/Accumulator are now faster than ever: t_{MAC} for J/R/S/T versions is now 85/75/100/90 ns, down from 130/85/135/100 ns; similarly, the ADSP-1016A 1.5-micron CMOS multiplier specs have been speeded up – clocked multiplication time is now 85/70/95/80 ns, while unclocked multiplication time has been reduced to 105/90/120/105 ns . . . AD7528, AD7524, and AD7533 CMOS DACs are now available in user-friendly (automatically insertable) CERDIP packages; their side-brazed packages are being phased out . . . Prices have been reduced for many of our video-speed 12-bit converters; consult the nearest sales office; prices have also been reduced for many RTI- series board-level microcomputer I/O products . . . The AC2630 mating connectors for the AD2050/60/70 series of uP-based digital temperature meters should have solder tabs if they are to be soldered to. If you received wire-wrap and need to solder, the connectors should be returned for replacement . . . Model 289 specification erratum: OFFSET VOLTAGE, REFERRED TO INPUT (Initial, @ +25°C) should read: (+5 + 20/G) mV max . . . In the 1S74 R/D Converter, the resolution control pins, when driven from TTL circuits using normal pullup resistors, may not always succeed in generating a "logic 1" input state; Three suggested solutions are: direct connection to +5-V rail (if resolution is not under software control), drive from +5-volt CMOS logic, or drive with an "active" pullup (emitter follower) . . . The earliest AD202/204 data sheet (C946-9-10/85) had several errata. These have been corrected in the data sheet for the extended AD-202/204 family (see page 22) . . . Analog Dialogue 20-1 Erratum: Page 25, 3rd column, AD7536 block diagram, the inequality is reversed.

MORE NEW PRODUCTS: . . . AC1307 Triple-Output Power Supply for 3B Series provides 800 mA at +15 V, 225 mA and -15 V, and 350 mA at +24 V . . . ADSP-1012A: High-Speed (50-ns) replacement in 1.5 um CMOS of the ADSP-1012 12x12-bit multiplier-accumulator, fully pin-compatible with the MPY012HJ1, available in all grades, including plastic . . . 5S70 Series of transformers for resolver/digital conversion feature 1,000-volt isolation and small size . . . DSS605 MACSYM 120 and IEEE-488 Interface Software . . . Run-time communications from the IBM PC (DOS) to the uMAC-5000 and uMAC-6000 via MCComm . . . Program development software (WOS): Write uMACBASIC programs with a PC, PC XT or PC AT . . . DAIS (Analog Dialogue 17-3) with P-I-D control option and version 2.0 of DAIS data-acquisition software (ASP150-XX) are now available – runs under CCP/M with MACBASIC 150/200, retains all the functions and capabilities of Version 1.0, adding user-definable graphics and direct access to the MACSYM 150's hard disk drive . . . Merge software program for DAC testing on the LTS-2020 Benchtop Tester combines the former DAC CREATE and DAC TEST programs into one consolidated program. This allows the user to create, edit, and run DAC device files, all from one program . . . LTS-1240 is a new network interface option capability for the LTS-2020 Benchtop Tester; it provides a link to transmit and receive data between the test system and a host computer, through a bidirectional RS232 port operating at 19.2 kbaud. The new networking system permits the LTS-2020, using the X/ON, X/OFF protocol, to upload or download an ASCII file to and from a host computer, such as the DEC MicroVaxII™ (running Bolt Beranek and Newman's RS/1™ statistical analysis and graphics software package).

DEFENSE NEWS . . . The Certification of our CMOS facility in Limerick, Ireland by the Irish government's Institute of Industrial Research and Standards has been accepted by DESC for MIL-M-38510 under an agreement between the two countries . . . As an immediate result, the AD7520UC/883B has become the first 10-bit CMOS d/a converter to be listed on the Qualified Parts List (QPL-38510), as M38510/12702BEC, legally required for use in new designs or redesigns of military hardware, under MIL-STD-454J . . . 4 versions of the AD532 and AD534 analog multipliers, produced at Analog Devices Semiconductor, in Wilmington MA, are now listed on the QPL . . . Our hybrid facility at the Computer Labs Division, in Greensboro NC, is now certified under MIL-STD-1772, joining our already-certified Microelectronics Division, in Wilmington MA.

U.S. PATENTS . . . 4,565,000 and 4,586,019 to Adrian P. Brokaw, for "Matching of Resistor Sensitivities to Process-Induced Variations in Resistor Widths" . . . 4,586,155 to Barrie Gilbert for "High-Accuracy Four-Quadrant Multiplier Which Also Is Capable of Four-Quadrant Division" . . . 4,590,456 to David P. Burton and Peter Real for "Low-Leakage CMOS D/A Converter" . . . 4,596,976 to Christopher W. Mangelsdorf and Adrian P. Brokaw for "Integrated Circuit Analog-to-Digital Converter" . . . 4,601,760 to Steven M. Hemmah and Richard S. Payne for "Ion-Implanted Process for Forming IC Wafer with Buried-Reference Diode and IC Structure Made with Such Process" . . . 4,604,532 to Barrie Gilbert for "Temperature Compensated Logarithmic Circuit."

REVOLUTION BY ANALOGY.



REVOLUTION BY ANALOG.

Our revolutionary new 12-bit, 5µs CMOS A/D converter eliminates specification compromises. It gives you the speed and resolution you need without the power, size and cost penalties of hybrids.

Made possible by our advanced monolithic BiMOS technology, the AD7572 features: low 135 mW power dissipation; 0.3" 24-pin DIP or 28-pin LCC packages; on-chip buried zener reference; and 90 ns bus access time.

The most revolutionary specification of all is the price: 5µs versions from $39.10 (1,000's) and 12.5 µs versions from $29.75 (1,000's).

The AD7572 is one of our hundreds of innovative data acquisition components, all aimed at making it easier to design signal processing subsystems.

For more information, call Applications Engineering at (617) 329-4700 ext. #3596 or #3597. Or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.

ANALOG DEVICES

Use the reply card for Technical Data.