analog dialogue

A forum for the exchange of circuits and systems for measurement, control, and test

D/A CONVERTERS FOR GRAPHIC DISPLAYS (Page 3)

Measurement and Control System with Mass Storage

Slam Package: Key to Superior Hybrids

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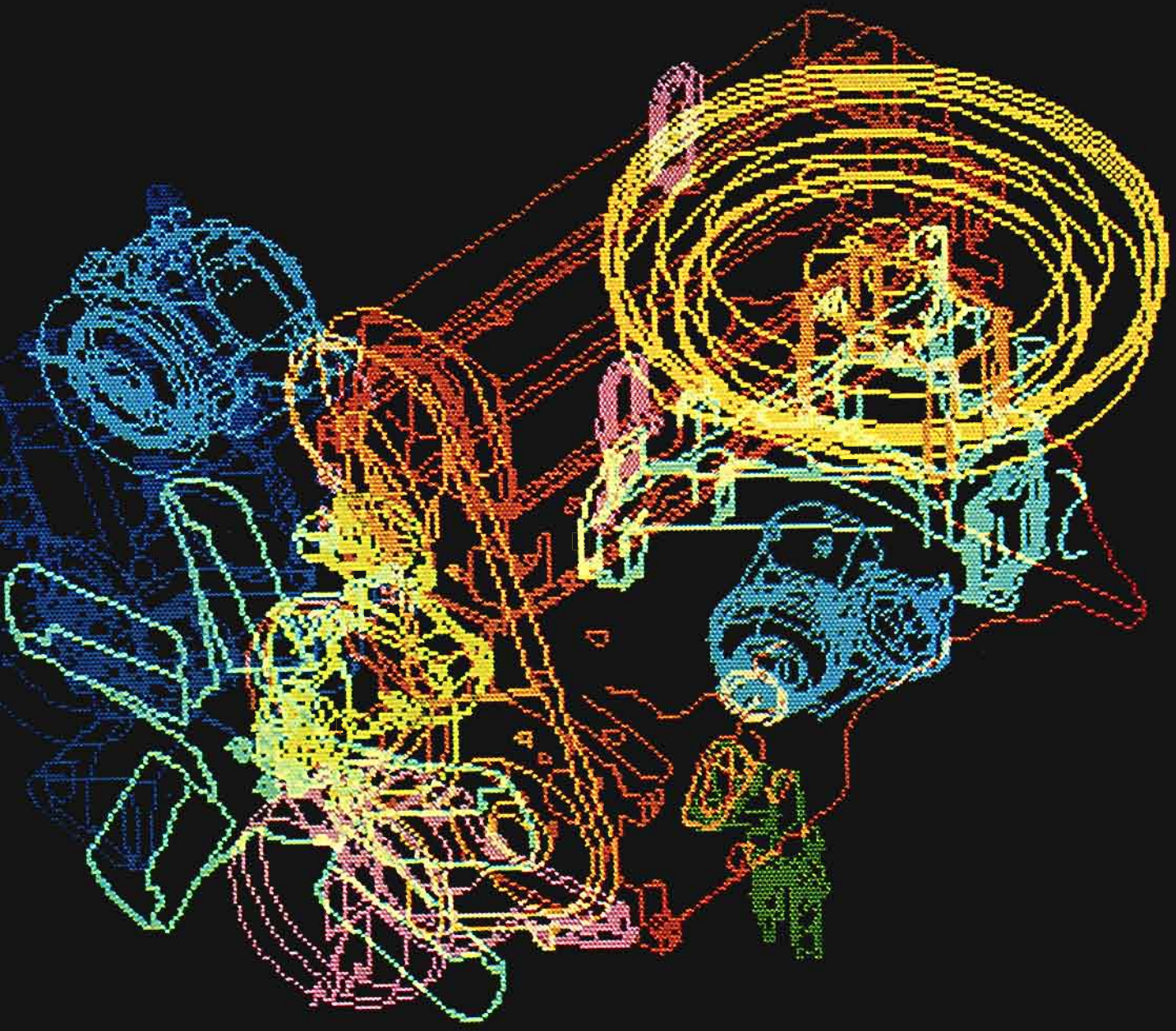

ANALOG DEVICES

Volume 15, Number 2, 1981

Editor's Notes

CAN ANALOG MAKE IT?

A scant two years ago, Analog Devices broke into the 9-digit revenue class. At this year's annual meeting, our President and Board Chairman suggested that, among other goals, by the conclusion of our next five-year planning inverval, our revenues could reach 10 digits, expressed in reasonably stable U.S. dollars, without adversely affecting either our internal climate or our treasured customer relationships.

The above question, impelled by this ambitious goal, called to mind a number of questions of somewhat similar ilk that have arisen at key junctures during the Company's history, most of which have been answered (sometimes resoundingly) in the affirmative. The following examples may provide some encouragement for those who wish us well.

Perhaps the first such question was "Can a new company in the op-amp business survive in the face of established module competition and the coming of IC op amps?" Chalk one up for the affirmative.

Another one was, "Can a successful op-amp company make it in other products (e.g., converters)?" Readers of this publication (and most users of a/d and d/a converters) can attest to the correct answer.

Then came a big one, "Can a successful precision module company make it in precision ICs?" Well, not only are we #1 in precision linear ICs, but we're #5 in *total linears* (including consumer circuits, which we don't make) and gaining fast on #4.

And another big one: "Can a successful component and subassembly company make it in systems?" (a related question is, "Can Analog make it in digital?") Though the jury has only started to consider its verdict, MACSYM Measurement And Control SYsteMs and LTS Linear-circuit Test Systems have given us a flying start.

CAN ENGINEERS MAKE IT?

While perusing a recently published roster, we were interested to note (and you may be, too) that every single member of top management at Analog Devices has at least one engineering degree, including our Treasurer, our Senior Vice President – Finance, and our Vice President – Human Resources.

It may also be worth noting that nearly one-half of this group had contributed technical articles to *Analog Dialogue* earlier in their careers. One might reasonably conclude from their vertical ascent that it pays to publish.

We can't guarantee success, but we would encourage others to test this assertion. Technical authors gain visibility and the perception by their peers of increased professional stature. ▶

Dan Sheingold

COVER PHOTO

The design, displayed on Computervision's Instaview™ raster-scan terminal, was created using the Designer V™ Computer-Aided Design and Manufacturing (CAD/CAM) System.

THE AUTHORS

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(More authors on page 18)

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HYBRID DACS FOR GRAPHIC DISPLAYS

Whether It's Vector Refresh or Raster Scan Fast-Settling, Low-Glitch D/A Converters Are Essential

by Walter Kester and Mark Skillings

The graphic-display oscilloscope can be found in increasingly widespread use in a growing variety of applications that were just wild dreams (if that) just a few years ago. According to Venture Development Corporation, CRT graphic terminal sales will increase fourfold between 1978 and 1983. Today's displays are characterized by high resolution, the promiscuous use of color, and a wide range of hardware and software options.

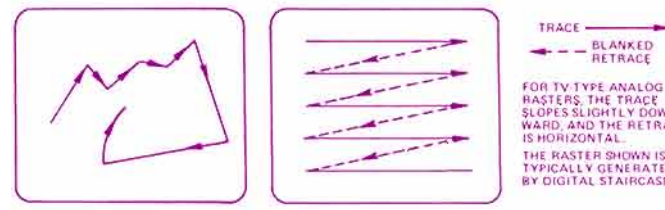
With computer processing, memory, and software widely available at low cost, computer-controlled displays have become popular in two basic forms: The *vector-refresh* (random scan, or calligraphic) display, which plots points or line-segments of randomly programmed length and direction, and the TV-like *raster scan*, which places a large number of closely spaced dots of variable illumination–and color–along a raster of closely spaced horizontal lines every 1/30 or 1/60 or a second.[1] While sales of vector-refresh displays are forecast to grow at about 15% per year, raster-scan displays are expected to grow explosively—tenfold—between 1978 and 1983, at which time they will account for 74% of all purchased graphic displays.

Driven to ever-higher scanning speeds to obtain increased resolution without flicker, the displays require extremely fast information transfer. For example, in a display with 1280 × 1024 fine structure, there are 1.31×10^6 picture elements (pixels). At 60 updates per second, each pixel must be displayed in less than 13ns. For sharp, clean raster-type displays, it is vitally important that the output d/a converter have fast response with imperceptible transient "glitches." For the user (and manufacturer) of such DACs, the very measurement of such performance poses a challenging problem.

In the following pages, we will discuss some of the differences between calligraphic and raster displays, the requirements for DACs, and suggestions as to how measurements may be implemented to verify their performance. We will also discuss the characteristics of a set of new 4-6-8-bit DACs with performance and architecture specifically oriented towards intensity modulation in raster-scan displays (the HDG-0405/0605/0805* series). In the next issue, we will describe a new deglitched 12-bit DAC, well-suited to calligraphic displays and for trace positioning in displays using digitally generated rasters.

ABOUT THE DISPLAYS

Vector-scan graphic displays are very much like ordinary oscilloscopes used in the X-Y plot mode, but the analog information is furnished via DACs instead of from the real world. Figure 1a shows the basic nature of the calligraphic plot. Typically, the beam is deflected to the appropriate values of X and Y at each point, and intensified; adjacent points are close enough together to appear to form a solid line or area (depending on the resolution of the DACs and the CRT phosphors). Figure 2 is a block diagram of a typical vector-scanned graphics application. In some cases, to avoid the use of excessively high-resolution DACs where large numbers of repeated small figures are required (e.g., alpha-numerics), the main DACs are used for positioning the outputs of a pair of ROM-operated fine-structure DACs, which generate the characters.



a. Randomly programmable vector-scan beam path.

b. Repetitive raster-scan beam path.

Figure 1. Display traces compared.

Vector-scan displays generally have considerably better resolution than raster-scan displays. For example, the top-of-the-line vector

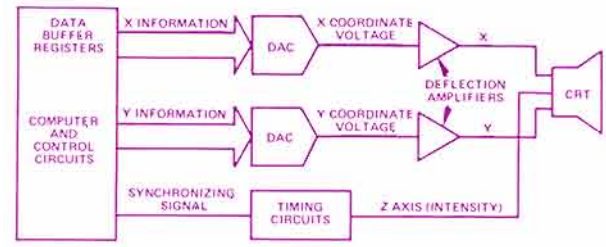


Figure 2. Block diagram of vector-scan display system.

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[1]See pp.81–87, *Analog-Digital Conversion Notes*, Analog Devices, 1977 ($5.95)

*Use the reply card for technical data.

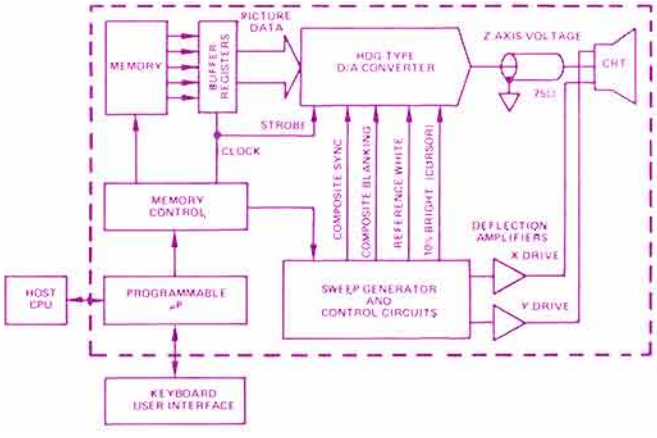
displays use 12-bit DACs with 50ns settling time to yield 4096 × 4096 (16-million-pixel) effective resolution, but color capabilities and gradations of intensity are limited.

The DACs must be monotonic and linear to avoid irregular spacing or actual reversal of direction; dynamically they must be fast and free of transient "glitches," which can cause distortion and loss of sharpness of transitions.

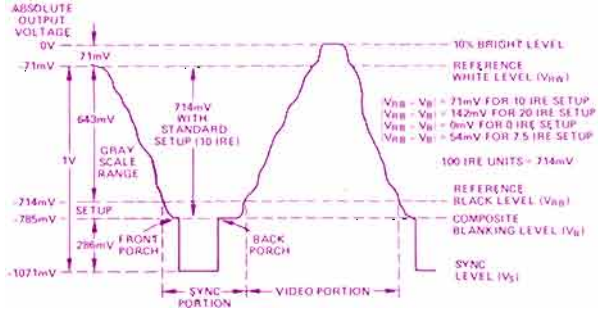
Raster-scan graphic displays are very much like television pictures (and, in fact, often use TV hardware): for each vertical sweep, there is a large number of horizontal scans during which the signal information is modulating the intensity input of the cathode-ray tube (Figure 1b). The major difference is that, in high-resolution displays, there are many more scans, and many more points per scan. The scans are synchronized, so that points occurring at the same time from the start of each sweep are directly above one another, and–if occurring on successive sweeps–will form a vertical line.

Because all points on the raster are scanned on each full cycle, the raster-scan cannot be as fast and sharp as the calligraphic display, especially for plotting simple figures; however the synchronization and standard nature of raster displays make it easier to use the intensity gray scale and to obtain a very great variety of color mixtures and hues, at low hardware cost.

One fast d/a converter is used for each electron gun: a single one for black-and-white displays, three for color. Figure 3a is a block diagram of a typical computer-controlled raster-scan graphic display, using a single DAC. The system consists of a MOS random-access memory buffer for storing display data in digital form, one or more memory controllers for managing the updating of the display and controlling the refresh cycle of the CRT, and a programmable microprocessor for generating display graphics and manipulating the image. The entire system operates as an intelligent peripheral to a host computer; most of the processing associated with image and graphic display is down-loaded to the graphic subsystem.



a. Block diagram.



b. Composite DAC output waveform.

Figure 3. Raster-scan display system.

If the picture resolution is specified as 1024 × 1024, there are 1024 horizontal lines, each having 1024 independent dots, each having its own programmable intensity level. Thus, there are 1,048,576 total pixels. If the picture on the CRT is to be refreshed 60 times per second, then a new pixel must appear on the screen at least every 15.8 nanoseconds (this is exclusive of "overhead time" associated with vertical and horizontal blanking during the sweep retrace portion of the cycle).

The d/a converter controls the Z axis of the CRT, to modulate the brightness of the raster-scan beam. For this example, the DAC must be capable of being updated at the pixel rate corresponding to 15.8ns; it should be capable of settling to a new value in less than 10ns. If a white dot is being plotted on a black background, the DAC output must make a full-scale transition between adjacent pixels. The resolution of the DAC determines the number of finite intensity levels available. Typical DACs for this purpose have resolutions ranging from 4 to 8 bits, corresponding to 16 to 256 levels of gray scale. For color displays, three memories and three DACs are required, one for each color gun of the CRT (red, green, blue).

Figure 3b shows the standard composite intensity waveform over 1½ cycles of the horizontal sweep. The controlled range of the DAC's full scale (0 to −643mV) is from reference white (−71mV) to reference black (−714mV). In the illustration, the intensity is varying from full white to full black. At the beginning of the sync portion, the intensity signal drops to the blacker-than-black "front porch" (−785mV), and then to the extreme black level (−1071mV) during the horizontal retrace. As the next sweep starts, the intensity returns to the "back porch" (−785mV), and, as the first element of the picture is triggered, to the controlled range of the DAC. During this scan, the cursor is displayed at the 10% "brighter than white" level (0mV).

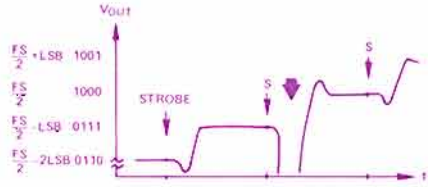
From 3b, it should be evident that it would be most helpful to the system designer if these additional analog functions were available in the DAC. All that would be needed are the appropriate synchronizing levels—the DAC would do the rest. The reader can correctly anticipate that these capabilities, hinted at in Figure 3a, are to be found in the HDG family (page 6).

ABOUT GLITCHES

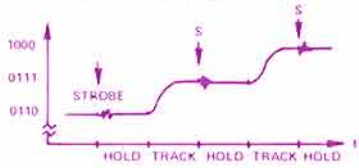
In response to a DAC input change, the output should move quickly and smoothly to the new value. A large transient spike accompanying a small output change (say 1LSB) is intolerable, since it creates a false intensity level (vertical lines, or fuzzy edges) in a raster-scan display, and a distorted waveshape in a vector-graphics display.[2] Such transients, or "glitches," are due to asymmetry in on-to-off and off-to-on times in switches and logic; they are inherent to some degree in all real DACs.

Consider, for example, the worst-case glitch, which can occur at a major 1-bit transition, such a 01111111 to 10000000. If the switches are slower to turn on than to turn off, there will be an intermediate output state where the lesser bits have turned off and the MSB has not yet turned on; thus the output will swing from a level 1 bit less than the MSB (½ full scale) down towards zero, then back up to the MSB level, as Figure 4a shows, producing a large negative spike.

[2] *ibid.*, page 87



a. Major-carry glitch.



b. Track-hold deglitching.

Figure 4. Glitches and deglitching.

Since the glitch is a nonlinear and code-dependent phenomenon, which produces an actual change in the average value of the new code, it cannot be simply filtered. In fact, there are just two basic ways of dealing with it—deglitching, and controlling the waveform to minimize glitch energy.

A deglitched DAC's output amplifier is connected as a track-hold; when the code is changed, the circuit is switched to *hold*; shortly thereafter, when the glitch has settled, the circuit is switched to *track*, and the stable output value is acquired. The output, as shown in Figure 4b, simply switches to the new level; any transients associated with the track-hold function tend to be of low energy, and are well-behaved and filterable in a decent design. The scheme is quite useful; its principal disadvantage is that the track-hold operation delays the acquisition of the new output value, a critical problem for a DAC that must modulate the CRT's intensity axis. This technique becomes difficult for update rates greater than about 20MHz.

The alternative is to minimize the overall magnitude of the glitch, and to further reduce its net area by causing it to be a fast doublet, susceptible to filtering (see Figure 5). Though it is difficult to accomplish in TTL circuits, because of the inherent asymmetry of saturated logic, non-saturating ECL (Emitter-Coupled Logic) is essentially independent of the direction of the logic transition and can be deskewed by small capacitive tweaks.

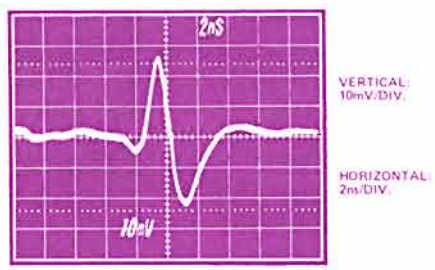


Figure 5. Typical controlled midscale glitch. LSB is 2.5mV.

Glitch "charge," proportional to the area under the plot of voltage vs. time, can be estimated in Figure 5, by approximating the waveforms by triangles, computing the areas, and subtracting the negative area (if any) from the positive area. Thus, the glitch charge in the case shown is controlled to $\frac{1}{2}(26 \times 1.8) - \frac{1}{2}(22 \times 3) = -10$pV-s, an average of 1mV (less than ½LSB) over 10ns.

If a d/a converter has a switching-threshold adjustment for the internal switches, it should be set to equalize the positive and negative glitches for the best compromise between the up-transition (01111111 to 10000000) and the down-transition (10000000 to 01111111). In this way, net glitch charge (often called glitch *energy*) can be minimized. In a well-designed DAC, the net glitch charge can be made much less than 100 picovolt-seconds; in the HDG-0805 family, it is reducible to less than 50pV-s.

ABOUT MEASUREMENTS

You may never have to make these measurements, but it's nice to know how it's done. Even if an engineer is experienced in high-frequency techniques, verifying the performance of (or using) an 8-nanosecond d/a converter presents a significant challenge. It is important that good practice be used; here are a few general pointers:

- The use of a good ground plane (double-sided copper board with ground on one side and conductors on the other) around the device being tested is mandatory! All converter ground pins should be soldered to the ground plane as closely as possible to where they leave the package. Instead of plastic or ceramic sockets (if sockets must be used), use spring-loaded pin sockets for each lead. Insert them through plated holes on the printed wiring board and solder them to pads on the conductor side.
- Decouple all power supply inputs with good 0.1-μF ceramic capacitors connected as closely as possible to the respective pins on the hybrid package.
- Use "microstrip" techniques in routing digital and strobe inputs to the DAC over distances greater than 1 inch.
- Terminate the DAC output with a 75-Ω resistive load as closely as possible to the package.
- Don't use oscilloscope "ground clip leads." Do use "bayonet adapters" on probe tips or "oscilloscope-to-BNC" adaptors. Keep ground impedance between the DAC output and the scope at a minimum.
- Don't use switching-type supplies. They tend to put out several-hundred-millivolt spikes containing components at very high frequencies that are almost impossible to filter out. These spikes tend to get into the grounding system and cause noise in the system for which the DAC or other analog circuitry gets blamed. Use a high-accuracy linear-regulated power supply with noise components of less than 5mV p-p for the −5.2V source.
- Make sure the measurement environment is clean, i.e., free of sources of ambient RFI (and shielded from the nearby TV tower).

The specifications of the HDG-0805 call for a minimum *setup time* of 2.5ns; this is the time the data must remain on the inputs before the strobe is applied. A minimum strobe *hold* time of 1.5ns must be allowed to ensure that the data is latched. The propagation delay (to 50% of final output change from the start of the strobe) is 3ns, and the settling time (from the first LSB of change to the final LSB) is 8ns.

Settling time at the major carry (01111111 to 10000000) can be measured on an oscilloscope with sufficient bandwidth. The major component of delay is the time required for the glitch to settle out.

However, settling time for a full-scale change (255LSBs in 8 nanoseconds) is considerably more difficult to measure. The gain required to measure settling time to 0.4% will overdrive the oscilloscope's vertical amplifier and produce errors. A useful way to avoid this problem is to employ fast window comparators (AM-685, AM-687, SP-9685, or SP-9687) to establish when the response has started (i.e., exceeds 1LSB) and when it is within 1LSB of the final value (T_1 and T_2). The oscilloscope is used only to observe the binary switching of logic levels rather than a graded analog response. Figure 6 shows a typical measurement setup.

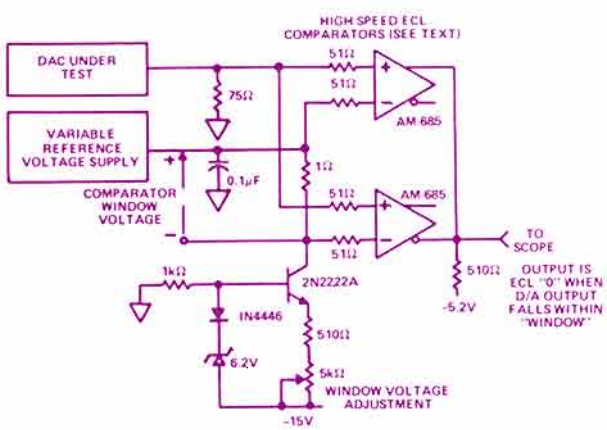


Figure 6. ECL window comparator circuit for measuring full-scale settling time.

To measure full-scale settling time, T_1 and T_2 must be measured. The window is set for 1LSB (2.5mV for the HDG-0805). For T_1, the reference is set at the most positive value that will still leave the comparator output at logic 0 during the time immediately preceding the output transition of the DAC. T_1 is defined as the time the comparator output reaches 50% of its transition following the start of the DAC output transition (Figure 7).

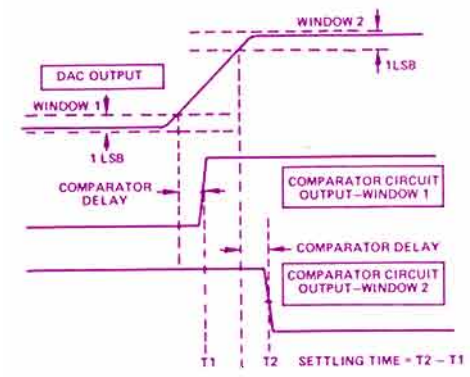


Figure 7. Time relationship of window comparator waveforms in full-scale settling–time measurement.

For T_2, the reference is shifted + until the comparator output returns to logic 0 during the time following the DAC's output transition, and the 50% point of the 1 to 0 transition is the shortest possible time after T_1. $T_2 - T_1$ represents the settling time, as defined above, independently of the fixed delay through the DAC input registers.

Since T_1 is established with both comparators in a state of large overdrive, and T_2 with the comparators in small overdrive, it is desirable to consult the specifications for the specific comparators

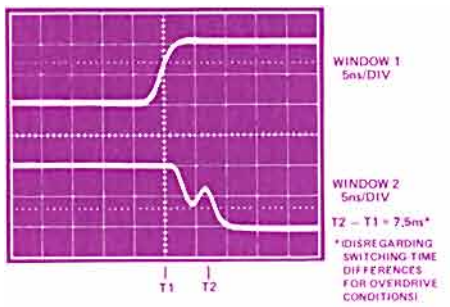


Figure 8. Waveforms for measurement of full-scale settling time. "Glitch" in Window 2 measurement is caused by overdrive conditions.)

being used to see if the difference in comparator response is sufficiently significant to require a correction, and to establish the size of the correction. Figure 8 shows the comparator waveforms for T_1 and T_2 superimposed in a double exposure. The eyeballed settling time is about 7.5ns.

ABOUT THE HDG FAMILY

Models HDG-0805/0605/0405 are 8-, 6-, 4-bit d/a converters specifically designed to meet the needs of most raster-scan systems requiring the resolution of 256, 64, and 16 gray-scale levels. Housed in 24-pin metal hybrid packages with 0.6" double-DIP spacing, they require only a single −5.2V power supply. Figure 9 is a block diagram of the HDG-0805.

Resolution is 8-bits, and full-scale settling to within 1LSB is typically 7ns (8ns max). The output impedance is 75 ohms, and full-scale output current develops 1V p-p video across a 75-ohm load. In order to minimize the glitch, a set of internal ECL registers provides minimum time skew between bits. Typical net glitch charge is 50pV-s. A Glitch-Adjust input is provided to optimize performance.

As Figure 9 shows, the unit provides self-contained digitally controlled sync and blanking capability, compatible with EIA Standards RS-170, RS-330, and RS-343A, to produce composite video waveforms like the one illustrated in Figure 3b. In addition to the 256 levels of gray scale provided by the 8-bit digital input, three additional digitally controlled switches independently provide auxiliary output currents of appropriate magnitude and polarity for blanking, sync, and 10% bright levels.

Because of its small physical size, the HDG-0805 can be located quite close to the CRT's intensity input, eliminating degradation caused by the skin effect associated with coaxial-cable interconnections (but it can drive 75-Ω cables directly if required). The grounded metal package effectively screens out the effects of the high noise environment usually associated with CRT drives.

Although rudimentary monolithic low-glitch d/a converters are available, the HDG-0805 provides, *in a single cost-effective package*, all the circuitry required for 256-level intensity modulation in raster-scan displays, at up to 100MHz video dot rates, for less than $60 in quantity. Even faster, the HDG-0605 (6ns settling, 64 levels) and HDG-0405 (4ns, 16 levels), are priced at only $49 and $42 in 500s.

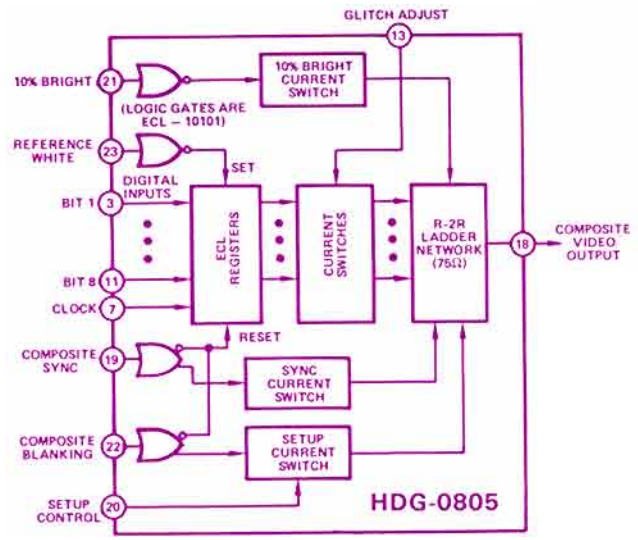


Figure 9. Block diagram of HDG-0805 D/A Converter.

MEASUREMENT-AND-CONTROL SYSTEM WITH MASS STORAGE

MAC02-28 Is a MACSYM 2 in a Rack with 9-Track Mag-Tape Drive It Can Store 10^6 Floating-Point Samples/1000′ of Magnetic Tape

by Robert J. Rogers

Analog Devices MACSYM* Measurement And Control SYsteMs are being used more and more to acquire, reduce, store, display, and output real-time information and to control processes and experiments in laboratory, process-control, and discrete manufacturing applications.

There are a number of features that make this minicomputer-based system powerful and easy-to-use. First, its universal ADIO (Analog/Digital Input/Output) bus accepts a growing set of interchangeable ADIO cards configured for a wide variety of directly connected external inputs and outputs–multi-channel thermocouple measurements, digital switch controls, frequency inputs, etc. Other advantages include the versatile, easy-to-learn-and-use, high-level MACBASIC programming language; inherent multitasking and floating-point; and the stand-alone housing with an ASCII keyboard/display, data-cartridge, real-time clock, and serial communication ports.

The MAC02-28*, an enhanced MACSYM 20 minicomputer-based Measurement And Control SYsteM, was designed to acquire large amounts of data in a short time, usually for later processing. It will gather large amounts of data and store them on 9-track magnetic tape. More than 1 million 4-byte floating-point samples at a continuous throughput rate of up to 400/s can be stored on 1000 feet of tape (and up to 4000/s in burst mode).

Typical applications for which you might use it include energy-management research, jet-engine testing, structural analysis, and automobile engine testing. It also has great potential for use in datalogging, archival storage, and program storage. The system can be interconnected with large mainframe computers, and its industry-standard recording formats foster data portability. It represents an economical way to acquire, store, and retrieve large amounts of data via a computer-based data-acquisition system.

The standard MAC02-28 system includes a 128K byte MACSYM 2 (configured for an external CRT terminal), with an advanced central-processing unit and a switch-selectable 800bpi NRZI or 1600bpi PE format, 18.75 inch-per-second, 9-track ½" tape drive, all mounted in a 6-foot relay rack, with a separate CRT terminal (CRT02), as shown in the photograph. It also includes interconnecting cables, manuals, and a system software package on 9-track tape. Its U.S. price of $29,328 includes installation supervision and assistance by Analog Devices factory-trained personnel.

There is additional space in the relay rack for other pieces of equipment; for example, up to 3 ADIO Expansion Chassis may be mounted in the rack enclosure, increasing to 61 the maximum number of multi-channel ADIO cards that can be used without additional "real-estate" cost. The maximum number of expansion chassis that can be connected to the MAC02-28 is 16, the same as for any MACSYM 2, making it possible to connect up to 256 ADIO cards.

Other options include a dual floppy-disk drive–for more-flexible file management; IEEE-488 capability–which allows the MACSYM 2 to be an intelligent controller, acquiring data from various instruments and recording it on the 9-track tape; a hardcopy printer; and the usual wide variety of peripheral options available for MACSYM systems.

The 9-track (one 8-bit byte plus parity) tape drive is easy to use. Its self-contained controller interfaces to the MACSYM 2 via the peripheral bus extender port; thus the backplane slot normally used for the data-cartridge controller is available for additional communications channels (ACP04). The 9-track tape operates on the same systems and applications software as the data cartridge it replaces; it thus offers greatly enhanced storage capacity and speed with no programming changes.

The MAC02-28 is specified for operation over the 15.5°C to 32°C temperature range at 20% to 80% relative humidity. Power consumption is specified at 985 watts (including the host MACSYM 2 and the CRT terminal). Power supplies are available for 115V @ 50/60Hz or 230V @ 50Hz. In general, the tape drive can also be used with upgraded existing MACSYM systems.

MORE ABOUT MACSYM

The MACSYM 2 system is introduced and described at great length in *Analog Dialogue* 13-1. Articles include a general description, the CPU, ADIO controller and bus, ADIO card library, MACBASIC programming language, and application examples. For a free copy use the reply card. For further information on MACSYM or MAC02-28, call the nearest Analog Devices Systems Sales Office.

* For technical data, use the reply card.

NEW PACKAGE IS THE KEY TO SUPERIOR HYBRIDS

Reliability, Cost, and Performance Are All Improved

Multilayer Slam Package Is Smaller, Minimizes Bond Wiring

by R. P. Knapp and T. R. Narasimhan[1]

The recent dramatic fluctuations in the market price of many of the precious metals used in the manufacture of electronic components have had a significant impact on the electronics industry. From IC packages to switches, from relays to connectors, manufacturers are forced to reconsider the economics of manufacturing methods developed when metals such as gold and silver were but a fraction of their current cost.

Among those industries deeply affected by the price of gold is the high-volume manufacture of hybrid microcircuits. Large numbers of gold wires have been used to connect components to the substrate, and the substrates themselves often use thick gold-film interconnects.

Recognizing the need for cost-effective hybrid packaging, Analog Devices began work on a new concept for hybrid design-and-packaging, in collaboration with some of the key manufacturers of technical ceramics. The result of these efforts is the Slam package technique, which has been successfully implemented in the manufacture of current models of many of our popular hybrids (e.g., AD522, AD2700, AD572)* and forms the basis of many of our new designs (e.g., AD578, AD612, AD2710/2712)*.

TRADITIONAL HYBRID TECHNIQUES

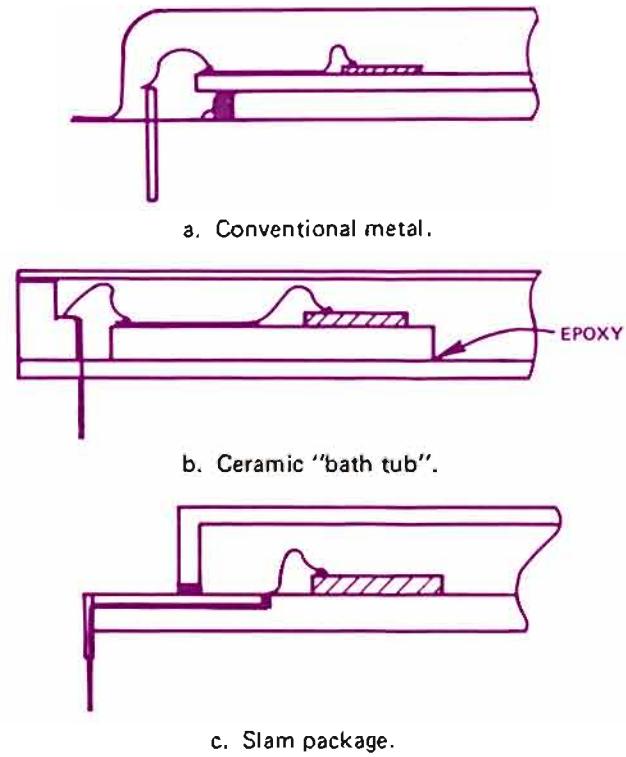
Among the more popular housings used by hybrid-circuit manufacturers are metal or ceramic flat packs and packages employing metal platforms, metal sidewalls, and ceramic cavities. As the cost of the precious metals normally used in these designs increased, packaging cost became a large percentage of the total device cost.

For example, most of these package types require a substrate that utilizes a printed gold-interconnect system. In addition, the substrate *area* is directly proportional to the circuit's size and complexity, since the economics of the thick-film processing techniques used in metallization preclude more than 3- or 4-layer construction. In addition, these package designs call for two-step mounting (components to substrate, and substrate to package), as well as multilevel wire-bond operations. The end result is a packaging system which is relatively costly (more components and processing, lower yields) and has lower inherent reliability (more bond wires) than the Slam technique.

THE SLAM PACKAGE

The Slam package is a multilayer laminated ceramic package; circuit interconnections and lead connections are integrated into the package design. The design eliminates the need for a separate substrate insert with metallized interconnects, and thus makes it unnecessary to secure the substrate inside the package and to bond numerous wires to connect the substrate to the package leads. Figure 1 compares the cross-sections of two popular package types–metal platform and ceramic bathtub–and a Slam-packaged device.

Each layer of the laminated package is made from 10-30-mil ceramic tapes which contain a metallization pattern of tungsten or moly-manganese, which is screened onto the tapes using a conventional thick-film process. Interconnections between the tape layers are made by punching holes, or "vias," through which a metal paste is drawn under vacuum. All vias on the tape are punched simultaneously using a metal die. A package can contain as many as nine layers. The tapes are stacked in order, pressed, and co-fired at high temperature (≅1200°C) to form the Slam package.



a. Conventional metal.

b. Ceramic "bath tub".

c. Slam package.

Figure 1. Cross sectional views of two convential hybrid packaging techniques (a, b) compared to Slam construction (c).

Leads are attached using conventional side-braze techniques, with silver/copper alloy. After the package has been fired, and the leads attached, the package is electroplated with nickel and gold on the pins and on areas of the top layer where conductors and pads have been left exposed with no dielectric. The lid is made of the same material and is generally pressed with a sidewall around the edge, deep enough for components and bond wires.

ADVANTAGES OF THE SLAM PACKAGE

The Slam package offers simpler processing, higher reliability, and better electrical performance than the current alternatives.

Processing Fewer assembly steps are needed, since there is no substrate insert; this eliminates substrate attachment, curing, and visual inspection from the assembly process flow. The integrated lead

[1]This article is drawn from a paper presented by the authors at the 1980 ERADCOM Hybrid Circuit Symposium and published by the U.S. Army Electronics Research & Development Command, Fort Monmouth NJ, as part of the *Proceedings* (not available from Analog Devices). We are indebted to Ed Soron for his invaluable editorial assistance.

*For technical data, use the reply card.

connections eliminate bond wires, equal in number to the leads. Automatic wire bonding is facilitated, because the number of bond levels is reduced (only chip and package levels are needed–the post or pin level is eliminated). Chip carriers can be used, as well as chip-and-wire assembly.

Eliminated are common problems inherent in bonding to thick-film gold metallization, such as weak bond strength, variability of gold thickness, open circuits, bridging, poor reliability, and life-test failures. The controlled plating process that prepares the metallization for bonding is quite consistent and less sensitive to process variations.

Slam devices are easily handled for automatic processing; the side-brazed pins fit easily into IC holding chucks for assembly and handlers for testing, and the devices fit easily into tubes for automatic loading and unloading. Batch sealing processes, such as polymer or solder reflow, can be used instead of brazing or welding.

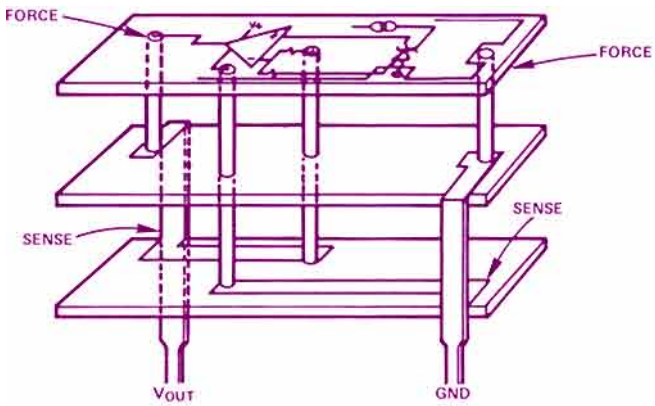


Figure 2. Simplified exploded view of Slam-packaged reference device.

Quality and Reliability Slam packaging is inherently more reliable. There are fewer bond wires; bond integrity is superior to that of thick-film gold; pull strength is consistently higher; and there is virtually no chance of conductor shorting, with 10-30-mil separation of lamination layers, instead of the common 2-mil dielectric thickness.

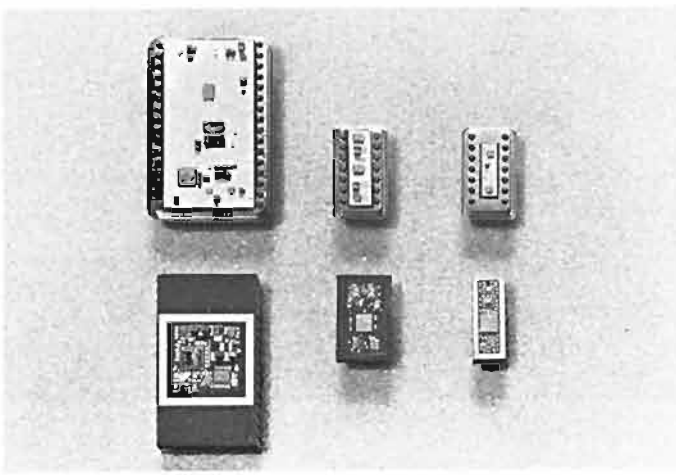


Figure 3. Popular hybrid products in metal and Slam packages. From left, AD572, AD522, AD2700.

The Slam process results in the widely accepted side-brazed package. Hermeticity is inherent, since most of the conductors are buried inside the ceramic package, and the side-brazed construction eliminates possible leaks at metal-to-glass interfaces at the posts in other package types. Compact construction and light weight means that Slam-packaged circuits can withstand higher mechanical stresses. Finally, elimination of the substrate and its interface to the package results in better thermal conductivity from chip to the environment, lowering junction temperatures and improving reliability.

Electrical Performance The direct connection to the package leads results in lower series resistance, reducing voltage drops in the package interconnections. Kelvin connections can be established internally, with the Sense lead contacting the pin and the Force lead on a different layer (Figure 2). Internal crosstalk and noise are minimized by the partitioning of the circuit into layers with up to 30-mil separation; this also reduces stray capacitance. Noise can be reduced by isolation of sensitive circuitry on separate layers away from noise sources within the device.

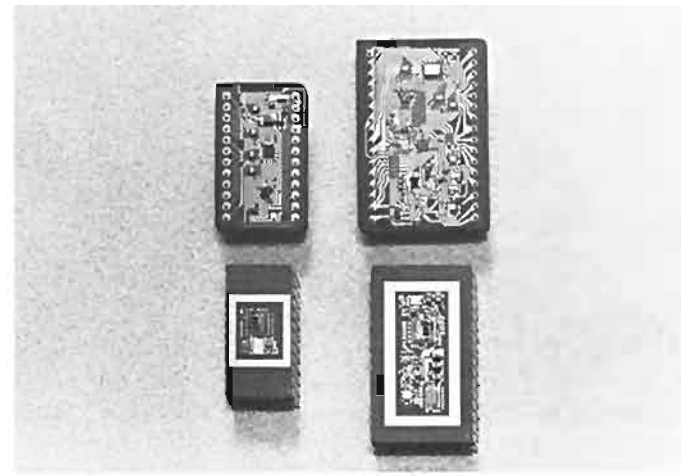


Figure 4. Second-source products: original (above), Slam (below). From left, AD DAC80, AD ADC80.

SLAM–PACKAGED PRODUCTS (Figures 3, 4, 5)

Despite the high tooling cost for Slam packaging, Analog Devices has been able to maintain and improve the price-performance characteristics of the most-popular hybrid designs. Older designs now available in Slam include the AD522* instrumentation amplifier, the AD2700* series of precision references, and the AD572* 12-bit ADC. Slam has made possible low-cost, reliable, high-performance second-source products, such as the AD DAC80/85/87* series, the AD370/71* series, and the AD ADC80*. And finally, most members of the new generation of hybrids from Analog Devices are packaged in Slam, setting new standards of value for devices of their type. Representative examples are the AD578* 3μs true 12-bit a/d converter and the AD2710* high-precision 10V-reference family.

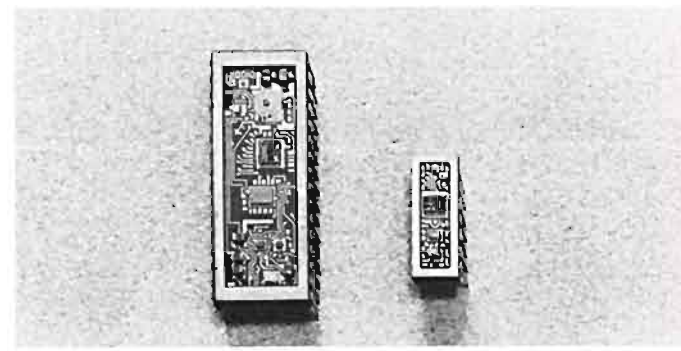
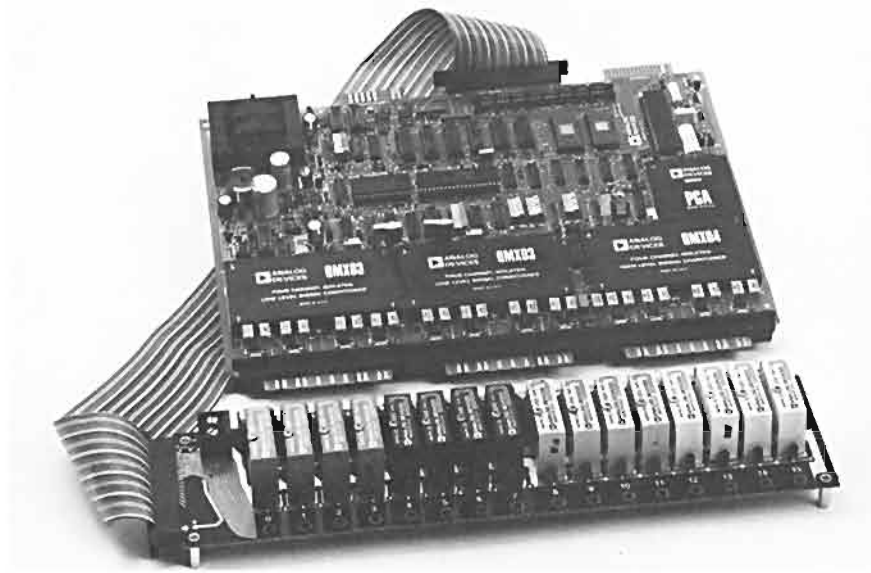


Figure 5. New hybrid products using Slam package: from left, AD578 (see text), AD2710.

REAL-WORLD DIGITAL I/O WITH 2500-V RMS ISOLATION

8 Mix-Match Inputs Sense AC or DC Power
8 Mix-Match Outputs Switch 3-Ampere AC or DC Loads

In the last issue, we described in some detail the µMAC-4000 expandable Single-Board Measurement and Control System*, which provides direct data acquisition from sensors and includes signal conditioning, conversion, and serial communications to any host computer. In addition to its ability to handle analog sensor inputs, it also has 8 channels of both digital input and digital output logic levels. The µMAC-4020, to be described here, provides a means of beefing up the digital I/O to respond to and switch power-level voltages and currents.



The µMAC-4020* is a manifold card which can accommodate up to 8 digital input modules and 8 digital output modules. These plug-in modules provide optically isolated (2500V) interfaces to ac or dc inputs and ac or dc outputs. They can be mixed and matched to meet the needs of the user's application.

By translating high-level signals, such as line voltage, to TTL levels compatible with the µMAC-4000's logic inputs, or translating logic outputs to isolated switch closures at high voltage and up to 3 amperes, the µMAC-4020 subsystem increases the µMAC-4000's ability to monitor ac or dc voltages and control ac or dc loads.

AC I/O INTERFACE

The ac modules switch at zero-crossings to reduce the generation of transients and interference, and they contain RC snubbers to eliminate line-voltage spikes. They can sense or switch ac voltages of 140V or 280V and have current ratings of 3A continuous rms and up to *55A peak*.

DC I/O INTERFACE

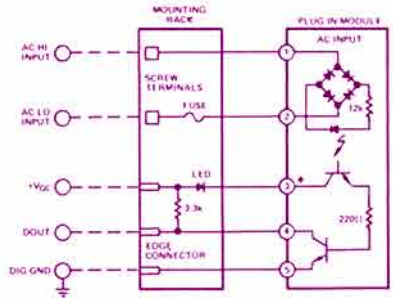
The dc modules incorporate debounce circuitry to provide clean switching. Output modules will switch levels of up to 60V, and input modules will handle 10V to 32V levels. DC output switching can withstand 5A peak surges.

The plug-in modules are physically interchangeable and have threaded inserts which accept hold-down screws that pass through the center of each module to secure it to the manifold. Each I/O module position includes a LED status indicator and a plug-in fuse to protect against miswiring and short circuits. Field wiring is accomplished via a screw-terminal strip on the µMAC-4020 manifold card.

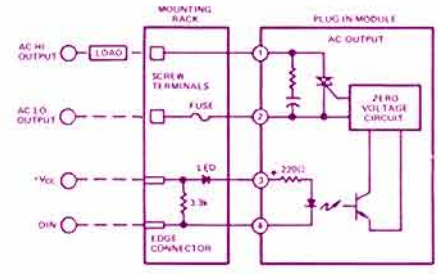
APPLICATIONS

Designed to meet the requirements of industry, the µMAC-4020 provides a means of direct control for motors, solenoid valves, annunciator panels, and numerous other control mechanisms requiring power switching of up to 3 amperes to loads. The ac and dc input modules serve as important elements of the control loop by providing feedback information on the status of actuated heaters, motors, etc.

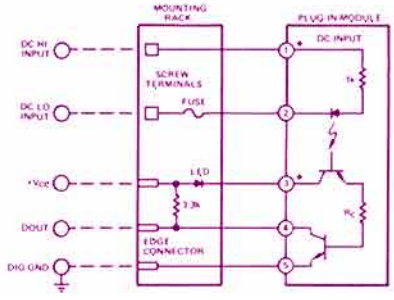
The µMAC-4020 manifold card and its modules are available from stock. The manifold is priced at $139(1–9), and the digital I/O modules range from $22 to $24 each.



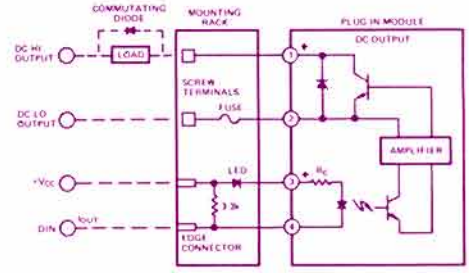
AC Input Module



AC Output Module



DC Input Module



DC Output Module

*For technical data, use the reply card.

THERMOCOUPLE SIGNAL CONDITIONER

Compact 2B50 Isolates, Amplifiers, Filters, and Compensates Reference-Junction Temperature

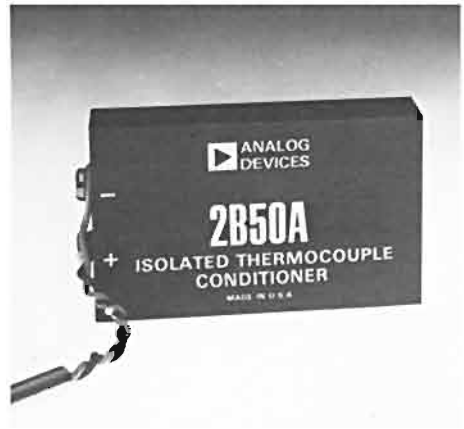
Model 2B50* is a high-performance thermocouple signal-conditioner. In addition to amplification, it provides isolation, filtering, and cold-junction sensing-and-compensation in a single compact package.

Designed for ease of use, it has screw-terminal input connections and jumper-programmable cold-junction compensation, and its gain (50 to 1000 V/V) is set by the choice of a single external resistor. Inherently isolated, the 2B50 is ideally suited for single- or multi-point applications in data-acquisition systems, computer interfaces, and measurement-and-control instrumentation.

An input normal-mode filter network provides protection (to 220V rms) for the low-drift (±1μV/°C max), high-performance amplifier (2B50B), which has less than ±0.01% nonlinearity. Isolated power is available for convenient optional adjustment of the input offset.

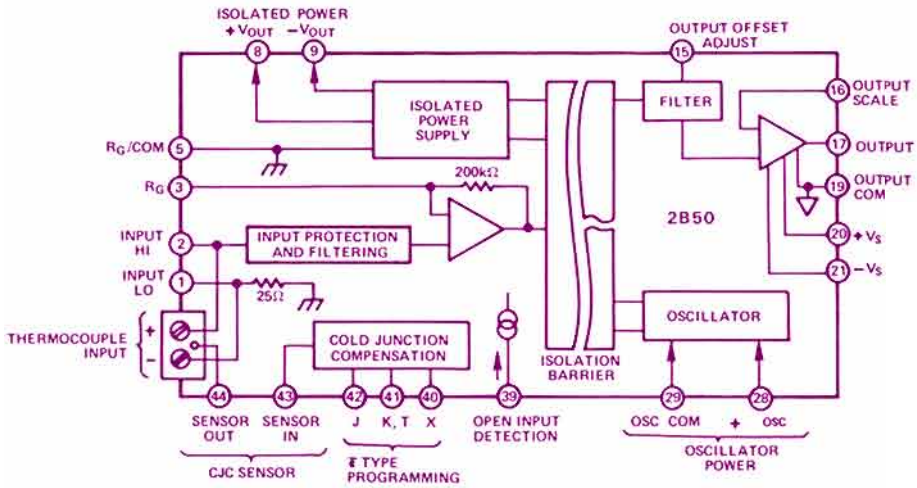
Reference-junction compensation is provided by internal circuitry. An integral cold-junction sensor is provided for direct thermocouple connections; for remote thermocouple termination, an external reference sensor (2N2222 transistor) may be used.

The 2B50 has jumper-programmable precalibrated compensation networks for types J, K, and T thermocouples. A fourth compensation network (X) is resistor-programmable for convenience in compensating other thermocouple types (E, R, S, or B). The module may also be programmed for *no compensation* if it is used as a signal conditioner or isolated amplifier for inputs other than thermocouples.



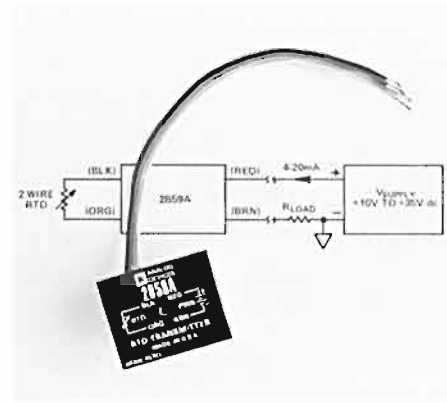
The 2B50 reliably provides input-to-output galvanic isolation of ±1500V peak and high common-mode rejection (160dB min @ 60Hz). Open-input detection, for indicating faulty thermocouples, provides a downscale-limit response.

Full-scale output is ±5V with the output jumpered directly; it may be scaled up to 2× for ±10V full-scale. The 2B50 measures 1.5"×2.5"×0.6" (38×63×14mm³) and is available from stock. Prices for grades 2B50A/B is $86/$103 in 100s.



RTD TRANSMITTER

Small, Low-Cost 2-Wire Input & Output



Model 2B59* is a low-cost temperature transmitter designed to accept an RTD sensor input and produce a 4-to-20mA output proportional to the sensor's temperature. The same two wires that are used for the 2B59's output also provide power from a remote voltage source connected in series with the output load resistance.

The 2B59 is designed to work with 100-ohm platinum and 1000-ohm nickel-iron sensors. Devices with additional input range are under development. Four precalibrated ranges (to within ±0.1% accuracy) are available for temperature measurements from −17.8°C (0°F) to +100°C (+212°F). User-accessible screwdriver adjustments permit zero and span to be adjusted over a ±5% range.

The 2B59 has been specifically designed for temperature transmission at low cost in multi-point energy-management applications. Its small size (1.2"×1.5"×0.5") and ease of interconnection, using conventional wire nuts, allow it to be mounted in standard 2"×4" utility boxes or thermostat boxes for remote temperature sensing. Price is $45 in 100s.

*For technical data, use the reply card.

HIGH-PERFORMANCE DUAL FET-OP-AMPS

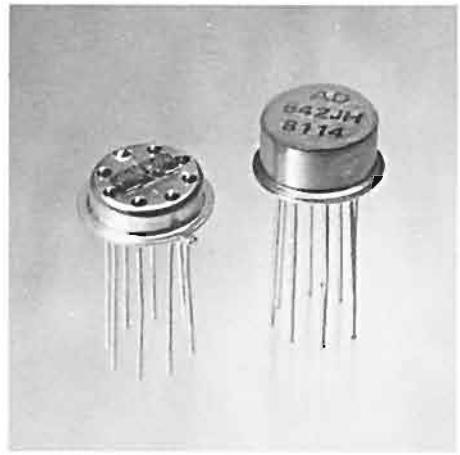
Laser-Trimmed Monolithic AD642L/644L

1mV Max Offset over Temperature

The AD642* and AD644* are dual versions of the popular AD542* and AD544* precision BI-FET operational amplifiers. The two types differ only in that the AD642's amplifiers are optimized for gain, while the AD644 has improved slew-rate and bandwidth specifications.

For example, the AD642J/K/L have maximum offsets of 3.5/2/1mV and gains of 100/110/110 dB *over the temperature range*, while the AD644J/K/L have similar maximum offsets of 3.5/2/1 mV with gains of 86/92/92 dB over the temperature range.

On the other hand, the AD644 has 13V/μs slew rate and 2MHz unity-gain small-signal bandwidth, vs. 3V/μs and 1MHz for AD642. Both families have low warmed-up bias current, e.g., 35pA max for "L"versions.

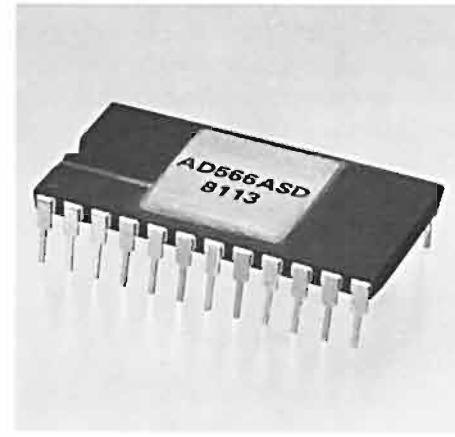


They are packaged in the hermetically sealed TO-99 header with standard dual op-amp pinout. Prices in 100s are: $4.50/$6.75/ $9.50/$18.95 for both AD642J/K/L/S and AD644J/K/L/S families.

12-BIT IC DAC

AD565A/566A Settle Fast

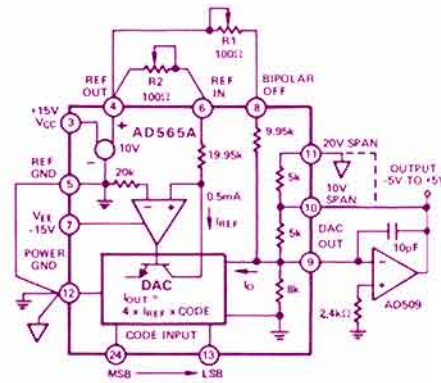
250/300ns Max to ±1/2 LSB



The AD565A and AD566A are the fastest monolithic current-output 12-bit d/a converters available. The AD565A, an improved version of the AD565, is a complete current-output DAC with its own self-contained 10.00V reference; it is pin-compatible with the popular AD563. The AD566A, an improved version of the AD566, is designed to use an external reference and is pin-compatible with the AD562.

True 12-bit converters, these devices are guaranteed monotonic over the operating temperature range. The AD565A chip uses 12 high-precision bipolar current-steering switches, a control amplifier, laser-trimmed thin-film resistance network, and buried Zener reference. Built-in SiCr thin-film precision application resistors scale the external op amp (or analog input when used in a/d conversion). Both devices are guaranteed for operation on ±12-volt supplies.

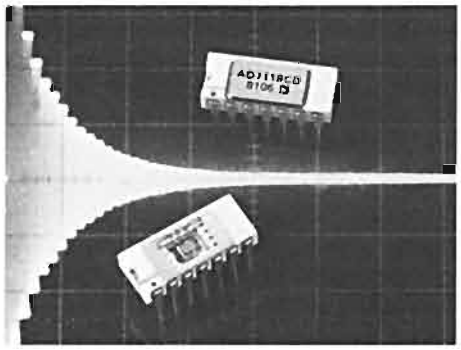
Available for the commercial or MIL temperature range, they are available in J/K/S/T versions. Prices start at $15.95/$12.95 in 100s, for AD565AJ/566AJ.



CMOS LOGARITHMIC MULTIPLYING DAC

85.5dB Dynamic Range, 1.5dB/Bit

Ceramic Package, MIL-Temp Available

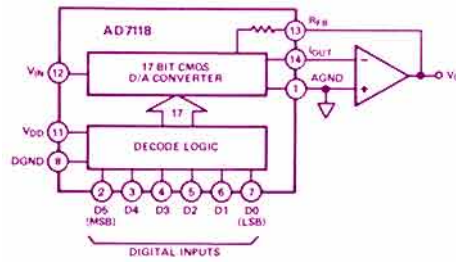


The AD7118* is a monolithic multiplying d/a converter in a 14-pin plastic or ceramic DIP. Accepting a 6-bit digital input, it provides digitally controlled gains from 0dB to −85.5dB, in 1.5-dB increments, for an analog input signal.

Used with an external op amp, it will accept analog input signals of up to ±25V (or the amplifier output range) and provide the digitally set logarithmic attenuation. It is useful for a variety of applications, including digitally controlled AGC systems, audio attenuators, wide-dynamic-range a/d converters, and function generators.

It operates from a +5V to +15V supply, with low power consumption, and does not require Schottky diodes to prevent latchup.

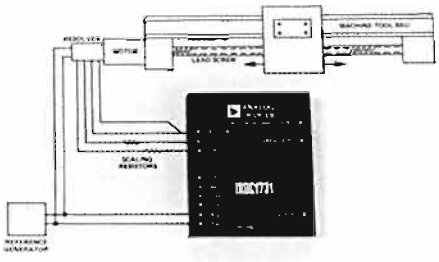
It is available in a choice of accuracy and temperature grades, in plastic and ceramic packages. Devices in ceramic packages are available screened to MIL-STD-883B. Prices in 100s start from $7.50 for AD7118KN (0° to 70°C, plastic).



*Use the reply card for technical data.

RESOLVER-TO-DIGITAL CONVERTER

IRDC1731 Handles Resolvers & Inductosyns
Isolated Inputs, 4000-Count Serial Output



Model IRDC1731* is an Inductosyn- or Resolver-to-Digital Converter that converts resolver-format (sine and cosine) signals into a 4000-count serial output. Inputs may be either from a resolver (4000 counts = 1 shaft revolution) or an Inductosyn slider, via external preamps (4000 counts = 1 pitch of the Inductosyn track).

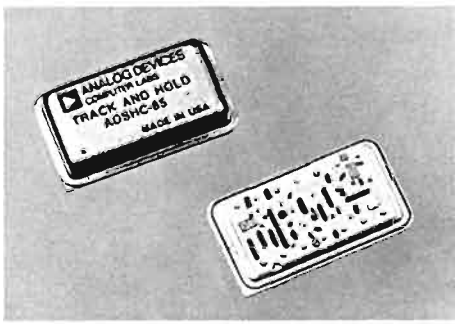
The converter is of the continuously tracking type in a Type 2 servo loop; this has the advantages of zero drift and up-to-date, instantly available data with no velocity error. The system can track at rates up to 100 revolutions/pitches per second.

Even though the signal and reference inputs are transformer-isolated, they can be externally scaled with resistance to accommodate the user's particular voltage levels. Since the IRDC1731 works on a ratiometric, amplitude-comparison principle, any voltage drops between the resolver and the converter do not substantially affect accuracy. The technique also fosters high noise immunity. No external trims or adjustments are required.

The IRDC1731 is well-suited to digital display of Inductosyn or resolver information in robotics or machine-tool axis measurements. The low-profile (0.4"H) module weights only 3.5oz. U.S. prices start at $255 (1–9).

FAST SAMPLE-HOLD

ADSHC-85 Settles to ± 1mV in 300ns
Replaces and Supersedes Other SHC-85s

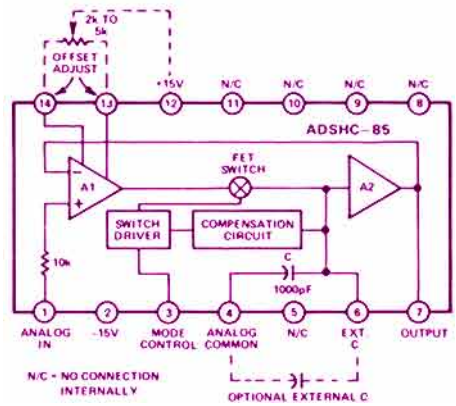


The ADSHC-85* is an improved second-source for this popular sample-hold amplifier in the 14-pin DIP. If you were concerned about the primary source's 500ns "typical" settling time to ± 1mV, you'll find the ADSHC-85's 500ns *max* (300 typical) a reassuring improvement.

Noise and input bias are also significantly better–typically 60μV and 50pA. The ADSHC-85 can be used with optional paralleled external capacitors, or with its own internal capacitor alone; this permits a tradeoff of speed for reduced droop and feedthrough errors.

Two versions of the device are available: the ADSHC-85 operates over the 0° to 70° C range, and the ADSHC-85 ET is specified over the military temperature range of −55°C to + 125°C.

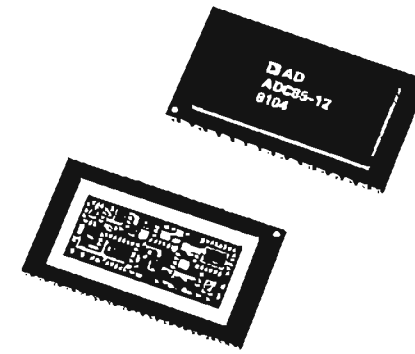
Both versions are available from stock, priced at $95/$129; substantial quantity discounts are available.



*For technical data, use the reply card.

FAST 12-BIT ADCs

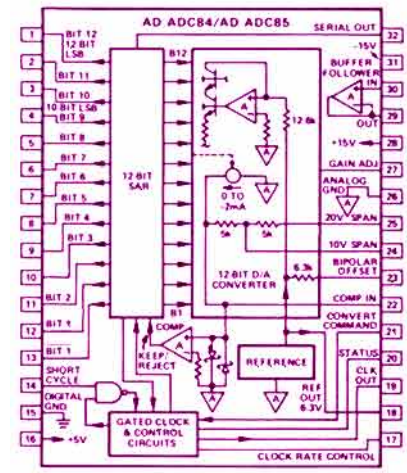
AD ADC84/85 Convert in 10μs
MIL-Temp, 883 Available



AD ADC84/85 series devices* are high-speed low-cost 10- and 12-bit successive-approximation hybrid a/d converters that require no external components to perform a conversion.

Their most important performance characteristics include maximum linearity error of ±0.0125% at 25°C, gain tempco below 15ppm/°C, low power dissipation (880mW), and conversion time less than 10μs. No-missing-codes are guaranteed over the operating temperature range.

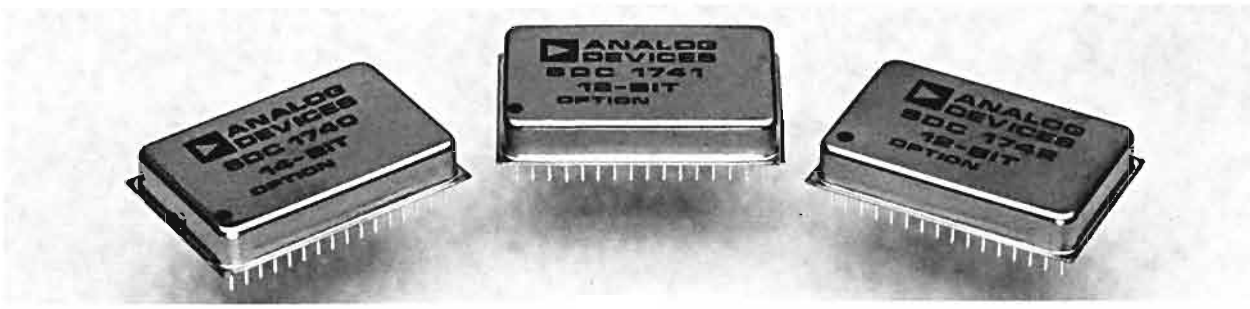
Employing the industry-standard pinout, The AD ADC85 directly replaces other devices of its type with significantly improved performance. In addition, its substantially lower chip count means high reliability. "Z" models are available for operation on ± 12V supplies, and MIL-STD-883B processing is available. Prices start at $55.75 (100s) for 12-bit devices.



ADVANTAGES OF 3-STATES IN SYNCHRO CONVERSION

Track the Input Signal Continuously without Opening the Loop
Digital Multiplexing is Sometimes Easier than Analog

by Steve Bloom



Conventional tracking-type synchro-to-digital converters run into settling-time problems when the input angle has changed during an "INHIBIT." When the data is placed on three-state latches instead, the worst-case throughput delays can be as little as 30 nanoseconds. In addition, multiplexing is made easier. A new microtransformer-isolated hybrid-circuit 14-bit SDC, with MIL-STD-883B screening available, will solve a number of these problems simultaneously.*

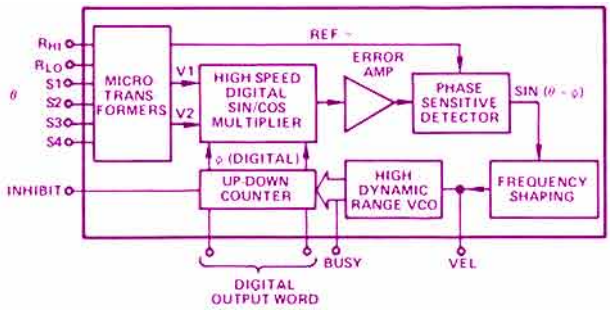


Figure 1. Typical Type II tracking synchro-to-digital converter.

Figure 1 is a block diagram of a conventional tracking s/d converter. The voltage-controlled oscillator (VCO) causes the up-down counter to produce an increasing or decreasing digital output, as needed, to balance the sensed error. During readout, when the *inhibit* line stops the count, by opening the loop, the error increases. When tracking resumes, there will be a finite settling time while the servo loop catches up, as much as 150 milliseconds for a worst-case change of ± 179.99°!

As Figure 2 shows, the loop can be freed to seek its null continuously if the counter is buffered by a set of latches and three-state switches. The information in the counter is always up-to-date.

Besides making it easier for the SDC to interface with an existing data bus, Figure 3 shows that digital on-the-bus multiplexing of SDCs with independent excitation frequencies and voltages becomes an easy matter. This simple scheme compares favorably with the complex system needed for analog multiplexing of SDCs shown in Figure 4.

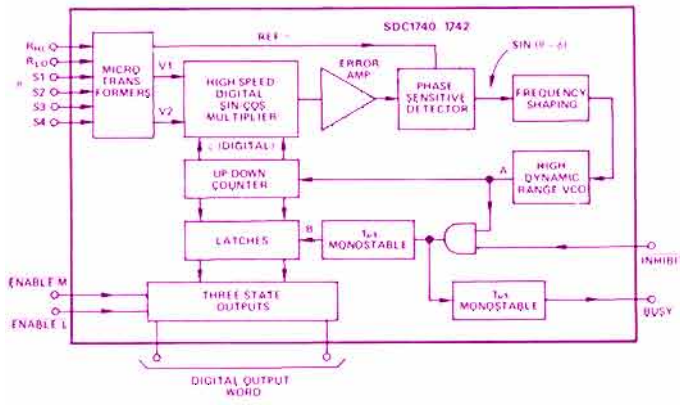


Figure 2. Tracking SDC with three-state bus communication.

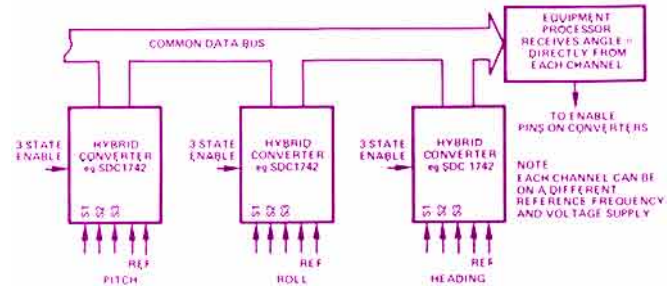


Figure 3. Multiplexed SDCs on a common bus.

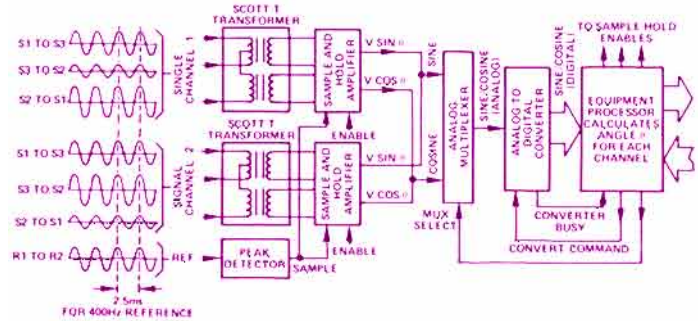


Figure 4. Complex analog multiplexing scheme using successive-approximation conversion.

*The data-transfer problem is discussed at length in pages 52–55 of *Synchro & Resolver Conversion*, 1980, 192 pp., edited by Geoff Boyes, available from Analog Devices @ $11.50, P.O. Box 796, Norwood MA 02062. For technical data on the popular 12-bit Model SDC1742, and on 14-bit Model SDC1740—when available—use the reply card.

Application Note

USER PROTOTYPE FAMILY BOARD

For Testing "Anything" with the LTS-2010 Tester Family
You Configure the Test in the Privacy of Your Own Lab

Figure 1. Photograph of the LTS-2010 and Family Board.

The LTS-2010 computerized test system for linear devices was introduced in *Dialogues* 14–3 (1980)* and 15–1 (1981)*. Its basic architecture is that of a *universal* tester: precision sources and measuring circuitry, controls, computer, memory, and communications facilities for humans and machines. To this are added specialized hardware and software (for example, family boards, device socketry, and program disks) to test specific classes of devices, and–within those classes– specific device types.

A key feature of this near-universal tester is the plugin *family board*, a drawer-like module that slides into the system console (Figure 1). Interfacing between the device under test, the precision measurement sources and circuitry, and the digital I/O and control circuits, it provides the special functions necessary to test a family of devices (e.g., op amps, ADCs, DACs).

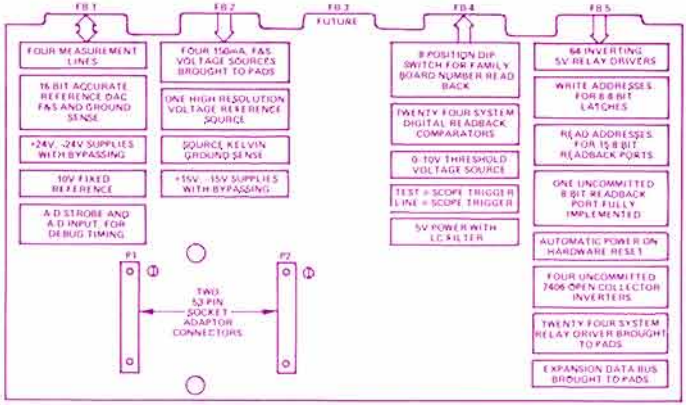


Figure 2. Services available on the board.

Although an increasing number of standard family test boards is being made available, they can never fully exploit the global testing capabilities of the LTS-2010. For specialized applications, where custom test circuitry is necessary, the LTS-2400 User Prototype Family Board is available. As Figure 2 shows, the available facilities include 2 socket adaptor connectors for the device under test, a DIP switch to identify the board, and a number of relay drivers, digital comparators, open-collector inverters, etc., and the services provided by the console, available at the edge connectors.

As an example of a simple application of this board, Figure 3 shows a scheme which has been used for testing and sorting resistors to better than 0.02%. The resistance of RUT is determined by applying a precisely known voltage and measuring the resulting dc current. The voltage applied, via Kelvin connections, is the difference between the LTS-2010's +10V reference and the (negative) output of the reference DAC. On the board, the force voltages are buffered by unity-gain followers (Z23, Z24), and the sense voltages are brought directly back to the console.

The current is measured by means of the voltage it develops across a 0.01% resistor (R6 . . . R9). The appropriate resistance range is established automatically, via software. The voltage is amplified by Z25, a precision instrumentation amplifier, and returned to the console for measurement. The LTS-2010 program for performing the measurement and grading the resistors–including calibration–is written in BASIC.

Range Selection

$\overline{DB1}$	$\overline{DB0}$	Selected Resistor	Range
0	0	R6	100k – 1MΩ
0	1	R7	10kΩ – 100kΩ
1	0	R8	1kΩ – 10kΩ
1	1	R9	100Ω – 1kΩ

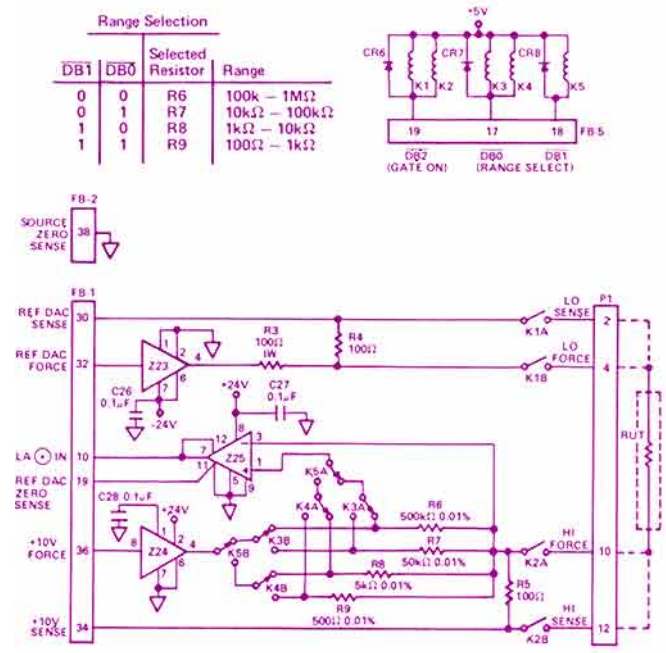


Figure 3. Circuit for resistor-test application.

*For technical information on LTS-2010 computer-based testers or copies of *Analog Dialogues* 14–3 and 15–1, use the reply card.

Application Brief

BEHIND THE SWITCH SYMBOL

Use CMOS Analog Switches More Effectively When You Consider Them as Circuits

by Jerry Whitmore

CMOS analog switches are widely used to make or break circuits in such applications as multiplexing and function switching. Ideally, they have zero resistance when closed, infinite resistance when open, no leakage, instantaneous glitch-free response, and no parasitic capacitance. While these assumptions are reasonably valid for low-frequency applications at moderate impedance levels, the good designer will always challenge them, to establish what errors may be introduced and even to determine whether the circuit configuration is viable.

SWITCH CIRCUITS

Figure 1 is a reasonable approximation of the circuitry in a single-pole dielectrically isolated CMOS switch (e.g., AD7510DI or AD7590DI series*). The dielectric isolation makes possible protection against latchup and overvoltage to ±25V beyond the supplies. Note that, for one polarity, conduction is via an N-channel FET; for the other polarity, it is via a P-channel FET. The two types are not perfectly symmetrical.

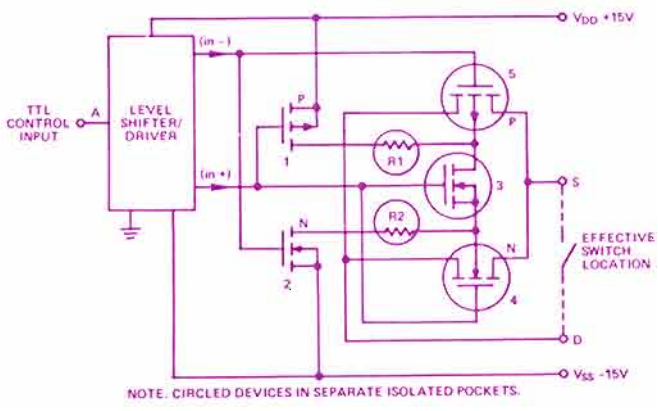


Figure 1. Typical output switch circuitry of the AD7590DI Series.

Figure 2 is an equivalent circuit of a pair of adjacent switches. The parameters are defined in Table 1. There are three principal categories of error one should be concerned about: low-frequency errors due to resistances and current leakage (switch open or closed), high-frequency and signal-transient errors due to stray capacitances (switch open or closed) and dynamic errors due to switching transients while the state of the switch is changing. Because of the present limitations of space, we shall for now consider just the first category, since it answers the most urgent question, "How well does the switch actually work for low-frequency signals?"

Although the leakage currents of the P- and N-channel transistors (devices 4 and 5 in Figure 1) might appear to tend to cancel, they don't, since the P channel is three times larger than the N channel.

*For technical data, use the reply card.

Table 1. Nomenclature

C_{DS}:	Open-switch capacitance
C_S,C_D	Source, drain capacitance
R_{ON}	Series on resistance
S,D	Source, drain; electrically interchangeable
C_{SS},C_{DD}	Capacitance between any two corresponding switch terminals
I_{LKG}	Leakage current of back-gate diode

Because of the size mismatch of the reverse-biased source-or-drain-to-back-gate diodes, plus the differing lot-to-lot variations in breakdown voltage of the diodes, it is difficult to predict leakage or its tempco. However, maximum values at 25°C and over temperature are specified and 100% tested.

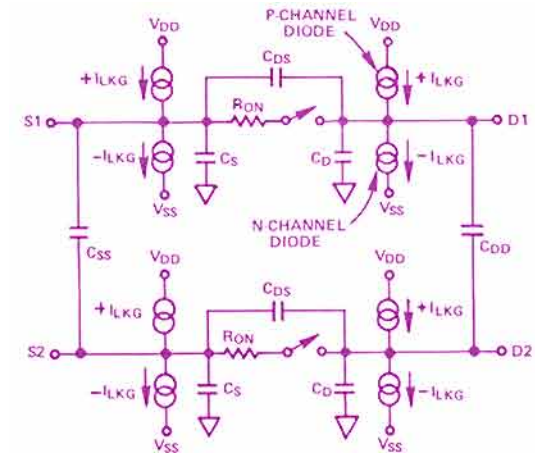


Figure 2. Equivalent circuit of a pair of adjacent switches.

Figure 3 shows the factors affecting dc performance for the *on* switch condition and how the various parameters affect the output voltage. Figure 4 shows typical curves of R_{ON}, as they appear on the product data sheet. They indicate how R_{ON}, is affected, as a function of input voltage, by supply voltages and by temperature, R_{IN} is lower and less signal-dependent at the higher supply voltages and lower temperatures.

How to minimize the influence of variable R_{ON} on circuit accuracy: Figure 5 shows a problem circuit–an inverting amplifier with four switched inputs. R_{ON}, in series with the 10-kilohm input resistor, affects the circuit gain. Even if it is compensated for at one level of suply voltage and analog input voltage, the input's variations will cause the gain to change and degrade the gain accuracy.

The most obvious solution–if the amplifier doesn't have to invert or act as a precision attenuator–is to use the amplifier in a nonin-

verting mode, as shown in Figure 6. Since there are no resistors in series, there is no effect on gain.

Another solution (Figure 7) is to connect the quad switch at the amplifier's summing point. Then the switch sees only millivolts–rather than volts–of signal variation, minimizing the variation of R_{ON} with signal. This solution can impair bandwidth, since capacitance C_S may require a capacitor in parallel with the feedback resistor for compensation. Also, I_{LKG}, flowing through the feedback resistor, may cause significant error, depending on the accuracy requirements. ($\Delta V_{OUT} = I_{LKG} \times R_F$).

Another possible solution is to use larger values of input and feedback resistance (Figure 8). Then the ΔR_{ON} variations will be small compared to the 1-megohm load. However, bandwidth will be affected by the larger R-C time constants.

Figures 7 and 8 do not compensate for the effects of variation of R_{ON} with temperature. A circuit that provides good compensation (Figure 9) uses one of the switches, wired *on*, in series with the feedback resistor. Its R_{ON} will tend to track that of the other switches on the same substrate with temperature; thus the feedback and input resistances will tend to track quite well, keeping the gain constant.

The principal dc effect in the switch *off* condition is that of I_{LKG} ($I_{D\ OFF}$ or $I_{S\ OFF}$), which will bias the output of a circuit by $I_{LKG} \times R_L$. Polarity of the error is determined by the dominant leakage polarity of a given switch.

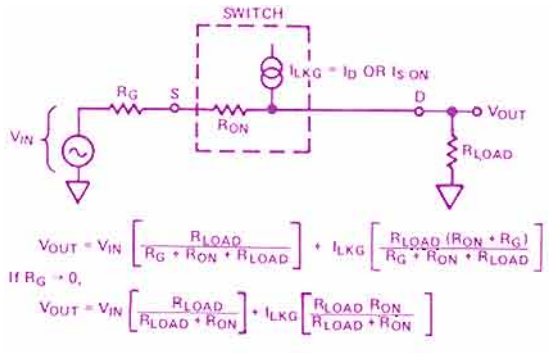
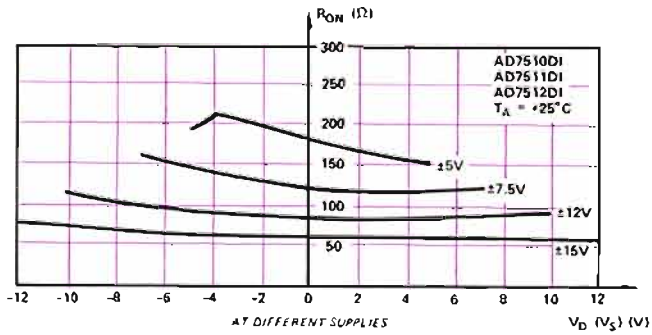
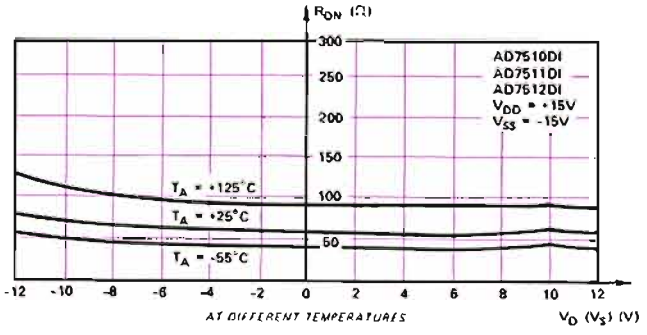


Figure 3. Effective circuit of switch in the ON condition.



a. R_{ON} vs. V_D (V_S), as a function of $+V_{DD}$, ($-V_{SS}$.)



b. R_{ON} vs. V_D (V_S), as a function of temperature.

Figure 4. R_{ON} vs. input voltage as a function of supply voltage and temperature.

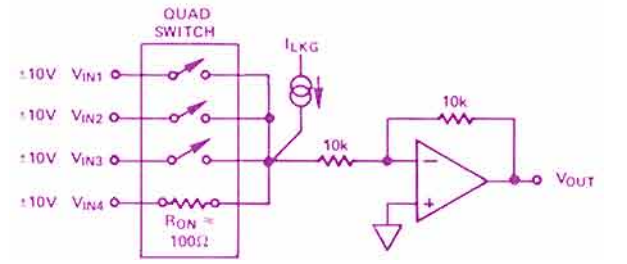


Figure 5. Unity-gain inverter with switched input.

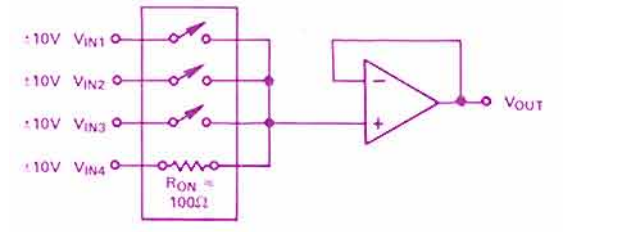


Figure 6. Noninverting solution.

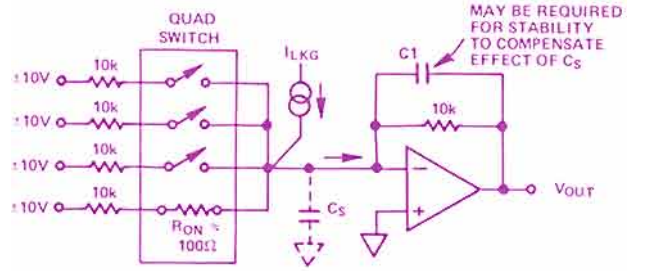


Figure 7. Connecting switch at the summing point.

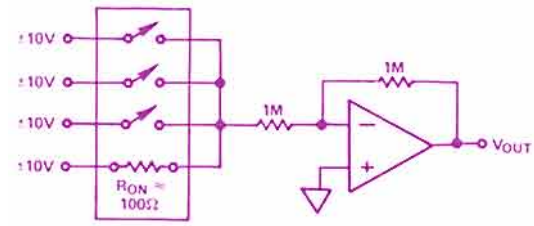


Figure 8. Using larger values of resistance.

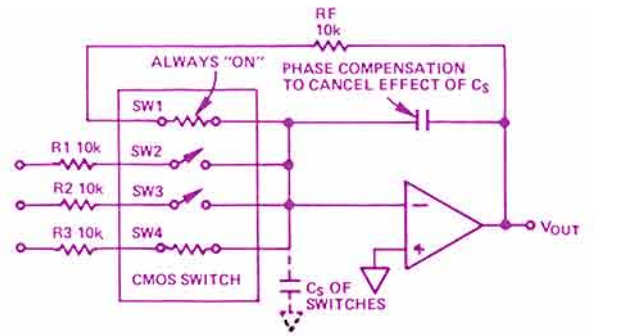


Figure 9. Switch in series with feedback resistor to compensate gain.

Across the Editor's Desk

The following communication has been received from Phil Burton and John Wynne, of AD-BV, Limerick, Ireland:

MICROPROCESSORS AND AD7581

The AD7581*, described in *Dialogues* 14-3 and 15-1, is an 8-bit, 8-channel monolithic CMOS a/d converter with 8×8 dual-port bus-addressable random-access memory. The converted value of each analog input appears at a separate memory location. *Dialogue* 15-1 showed examples of interfacing it with 6800 and 8085-type microprocessors. Here's how to connect it to some other microprocessors as a memory-mapped I/O device.

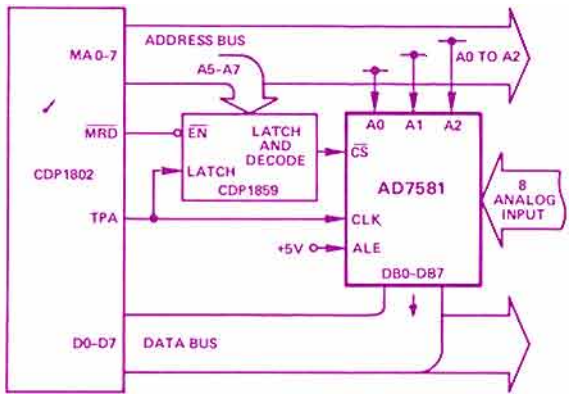
Z80: Simple Method Connect CLK (pin 15) of AD7581 to $\overline{M1}$ (pin 27) of Z80. Strap ALE (pin 16) of AD7581 to V_{DD}. The rest of the connections are as for a ROM with a single CS input.

One clock pulse is received by the AD7581 for each instruction executed by the Z80. Although the a/d conversion rate is slow, the method works with Z80s of any speed. If the application uses any of the Z80 Memory-Block Search or Move instructions, the conversion rate is slowed down considerably. The AD7581 requires 640 clock pulses to complete a/d conversion of the signals on all 8 channels.

Z80: Advanced Method Drive the AD7581's CLK (pin 15) from $\overline{MREQ}$ (pin 19) of the Z80 via a fairly high-speed inverter, e.g., 74LS04. The clock frequency to the converter will vary, depending on the Z80 instruction, but it will be between ½ and ⅓ of the Z80's clock frequency. As with the simple method described above, ALE (pin 16) of the AD7581 should be strapped high and the part operated as a ROM.

The advanced method may cause the AD7581 to place invalid data on the data bus at the beginning of the READ cycle; however, the data will settle in time for the Z80 to read the correct data. This hookup may be used only where the Z80 clock frequency is less than 2.4MHz. Faster Z80s can be used if $\overline{MREQ}$ is divided down to an acceptable lower frequency.

COSMAC CDP1802 The CDP1802 has an 8-bit address bus multiplexed between the address high byte and low byte. TPA is a clock which occurs every machine cycle. Its rising edge precedes by 600ns the point at which the CPU expects valid data on the data bus at maximum CPU clock frequency; it is an ideal clock source for the AD7581. The falling edge of TPA indicates when the high byte is valid on the address bus; therefore it is used to drive the 4-bit address latch in the CDP1859 (see Figure). $\overline{MRD}$ is low during memory read cycles; it is used to enable the address-decode logic.



* For technical data, use the reply card.

6802/6809 The AD7581's 8 bytes of RAM are simply incorporated into the 6802/6809 memory map. Updating each of the analog input channels takes place in a way that is completely transparent to the system CPU; however the clock source must be chosen so that an update cannot occur just as the CPU is reading data. Therefore, the diagram for these µPs is similar to that for the 6800 (*Dialogue* 15-1, page 13, Figure 2a), except that, for the 6802, E is connected to the AD7581's CLK; for the 6809, Q is connected to the AD7581's CLK, R/W is connected to the 74LS138's EN, and BA is connected to EN.

Notes for Users of Other µPs All the internal action of the AD7581 is initiated by the rising *edge* of the CLK input. By 200ns after the rising edge, most of the "action" is over, and stable data is available in the internal memory. If the AD7581 is operated at above the specified 1.2MHz, the first effect that may be noted is a loss of accuracy, and codes may start being missed, since the maximum clock rate is dictated by the conversion process, not the internal logic. *General note:* Pin BOFS of AD7581 should be connected to AGND, if not used, to minimize crosstalk and comparator settling time.

MORE AUTHORS

(Continued from page 2)

Dr. T.R. Narasimhan (page 8) is Manager of Engineering at ADI's Microelectronics Division, Wilmington, Massachusetts, where he is responsible for design and development of hybrid circuits and technology. He has a Ph.D. degree from Nova Scotia Technical College, in Canada. Prior to joining Analog Devices, he was Director of Hybrid Engineering at ILC Data Device Corporation.

Steve Bloom (page 14) is Synchro Products Engineer, providing domestic technical support for products of ADI's Memory Devices Division. After studying for his B.S.E.E. degree at Purdue University, he worked at ILC Data Device Corporation in Engineering and Sales. He has published an article on the MIL-STD-1553 digital data bus. His present activities include technical training and future-product definition.

Jerry Whitmore (page 16) is Marketing Manager at Analog Devices B.V., in Limerick, Ireland. Earlier, he was an Applications Engineer at ADI Microsystems. He obtained his basic engineering background at E. Montana College. Prior to joining ADI, he served in the U.S. Navy, then at Zeltex, where he gained varied and relevant experience in op-amp and converter development.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE (Volume 15, Number 1, 1981) . . . *Single-Board Measurement And Control System*: μMAC-4000 . . . *Two-Wire Temperature Transmitters*: 2B52, 2B53, 2B57, 2B58 . . . *6-Bit ADCs Convert in 10/20 Nanoseconds*: Monolithic AD5010KD/6020KD . . . *Stable, High-Accuracy 10.0000V References*: AD2710 Family . . . *8-Bit 8-Channel DAS Stores Conversion Results*: AD7581 (see also opposite page ←) . . . and these New Products: High-Speed Sample-Holds (ADSHM-5 and ADSHM-5K) . . . HOS-100 Fast Follower (Slews at 1000V/μs Minimum, 125MHz -3dB Bandwidth) . . . Flexible Tester Programmable in BASIC (LTS-2010) . . . Six New MACSYM I/O Interface Cards: Thermocouple Interface; Isolated Digital I/O; IEEE-488; Analog Input; Digital Output; Interrupts . . . True RMS-to-DC Monolithic A/A Converter (AD636) . . . Hybrid 12-bit ADCs in Hermetic DIP (AD5200 Series) . . . Application Brief: *High-Speed Software-Controlled Gains*, using the AD612/614 Hybrid Programmable-Gain Amplifiers . . . Worth Reading: A New Book: *Synchro and Resolver Conversion*, edited by Geoffrey Boyes. 192 pp., $11.50, from Analog Devices, P.O. Box 796, Norwood MA 02062, in the U.S. . . . Signal-Conditioning-Product Guide: *How to Optimize the Transducer-to-Computer Interface in Data-Acquisition Systems* (Free) . . . *Designer's Guide to High-Resolution Products* (18 pp. - Free) . . . plus Editor's Notes, Across the Editor's Desk, Authors, Potpourri, etc.

NEW DATA SHEETS . . . An updated data sheet on the AD544 fast monolithic Trimmed Implanted FET-Input Op Amp is now available (11/80) with more performance data and applications . . . A data sheet describing peripherals for MACSYM is available: It describes two CRT terminals, a teleprinter terminal, an X-Y plotter, floppy-disk drives, serial impact printers, and a CRT monitor . . . Data sheets on the new high-resolution quad-12-bit-DAC voltage and current output cards for MACSYM (AOCØ1 and AOCØ2) are available. The AOCØ2 offers two current-transmitter options.

FREE APPLICATIONS INFO . . . *Macsymizer*, a MACSYM Users' Newsletter, is available free to anyone interested. The first issue (Vol. 1, No. 1) includes programs for solving linear equations with MACSYM 2, time-of-day testing, and square-rooting. Also discussed are low-pass filtering, running concurrent tasks in MACBASIC, and inexpensive data storage and transportation, with MACSYM 2 and cassette tape. A number of new products are described, and information on MACSYM 2 training courses is made available. In addition, there's lots of useful miscellany: descriptions of available application notes, new software releases, and manuals. Write on letterhead to *MACSYMIZER*, c/o MACSYM Marketing, Analog Devices, Inc., 4 Norwood Technology Center, Norwood MA 02062 . . . Our Component Test Systems Group has been industriously building up a library of programs for testing linear devices: op amps, DACs, voltage regulators, and comparators, using LTS2000 and LTS2010 computer-based benchtop testers (*Analog Dialogue 14-3*). Included are both BASIC and menu-type programs. For information on programs to test your favorite linear device(s), get in touch with your Analog Devices field sales office.

TECHNICAL TIPS . . . Did you know? The AD7581, in addition to its ease-of-use with microprocessors and ability to provide 8 channels of analog input information upon demand, is also latch-up proof, because its analog inputs are buffered by resistors (unlike some popular 8-channel devices now on the market that have been compared with it) . . . Mysterious offsets in op amps — it's been said before and is worth repeating: Unexplained drifts in low-frequency dc op-amp circuits may be caused by rectification of high-frequency signals that may somehow have gotten into the input stages of the (precision) op amp, and are invisible to dc instrumentation. Use an oscilloscope to track them down! Where do they come from? Anywhere! Your friendly local TV tower, your noisy power line, a high-frequency source sharing your power supply, perhaps even an oscillation in the amplifier itself! Or perhaps it's coupled from a nearby computer of high-frequency source - if you didn't bother to shield the circuit . . . The AD558 *complete* 8-bit IC μP-compatible single-supply DAC is a little slower on the downswing than on the upswing. If you're looking for top speed in both directions, all it takes is a little pulldown current.

NEW PATENT . . . 4,250,445: *Band-Gap Voltage Reference with Curvature Correction*, by A. Paul Brokaw, was issued recently.

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