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Analog Computation with Magnetoresistance Multipliers

Novel technique multiplies and divides in same package, achieves up to 0.1% accuracy for total cost less than \$350 and provides electrical isolation between input and output signals.

By R. M. Gitlin President, American Aerospace Controls, Inc.

This article describes a little-known technique for multiplying, dividing and otherwise manipulating AC and DC signals using flux-variable resistors (magnetoresistors) in a novel bridge configuration. The basic magnetoresistance bridge* forms a four-quadrant multiplier, but with the aid of operational amplifiers, provides 0.1% linearity in squaring, square-rooting, modulating, mixing, demodulating, rectifying, and related applications.

One particular version of the unit, which will be described here, develops an output proportional to kAB/C, where A, B, and C are three independent variables. The unit simplifies many mathematical functions by simultaneously multiplying and dividing, and makes a phase-stable modulator, or electrically isolated amplitude control, for precision AC reference voltages.

Particular merits of magnetoresistance multipliers include their natural compatibility with off the shelf operational amplifiers, as well as their simplicity, versatility, and high linearity and temperature-stability when feedback is applied.

In essence, the magnetoresistance multiplier is a solid-state analog of electromechanical multipliers based on servo-driven potentiometers. Naturally, the solid-state unit affords considerably better bandwidth than its electromechanical counterpart; it also costs less, requires less space, is virtually maintenance-free, and operates on a fraction of the power. It also permits 1% accuracy over a 100°C temperature range for less than \$350 total parts costs.

Frequencies to 1 MHz can be applied to the multiplier's bridge circuit providing careful capacitive trimming is used, while an upper limit for coil inputs is about 1 kHz. Coil frequency can be extended in special units by use of ferrite cores, or by resonating the coil over specific narrow-band frequency ranges.

MAGNETORESISTANCE

Magnetoresistance is a fundamental phenomenon allied to the Hall effect, and present in many materials, but exhibiting greatest sensitivity in bismuth and such semiconductors as indium arsenide and indium antimonide. Indium antimonide has the highest flux-sensitivity, but present production techniques require 0.02" thick ceramic substrates and yield only modest zero-flux resistivities. On the other hand, bismuth provides a better overall compromise because thin-film layers can be deposited on 0.002" mylar substrates to make flexible sandwich elements capable of slipping into 0.005" air gaps. Optimum resistance levels for bismuth magnetoresistors are around 1000 ohms, with 0.1 watt dissipation.

Typical bismuth magnetoresistors undergo roughly 10% resistance change for 5 kilogauss flux-density variations. Although this might seem a small resistance swing for most uses, careful design of the multiplier's magnetic circuit turns this 10% change into a ±60 dB dynamic signal range. Output level at null is limited by noise, second harmonics, drift, etc., to about 200 microvolts, while the full 10% resistance swing develops roughly ½ volt output from a magnetoresistance bridge excited at 10 volt.

ANALOG COMPUTATION, Continued.

Temperature effects are mostly confined by the bridge configuration to sensitivity-loss at high temperature. Open loop multipliers use negative coefficient thermistors for temperature compensation, while double-bridge units virtually eliminate temperature effects by enclosing the bridge within a high gain feedback loop.

MAGNETORESISTANCE VS. HALL

Magnetoresistance elements have several advantages over Hall elements in multiplier and transducer applications. In the first place, it's a pretty rare Hall multiplier that can develop 500 millivolts output. Secondly, the bismuth magnetoresistor's optimum resistance level of 1000 ohms makes it completely compatible with inexpensive off-the-shelf operational amplifiers. (e.g. Analog Devices Model L114A at \$35). By contrast, Hall elements often require 500 milliamps drive current at ½ volt or so, which is far from a convenient level.

Further subtle advantages of magnetoresistors are two-terminal rather than four-terminal connections, inherent drift compensation through the balanced bridge configuration, and self-cancelling of induced voltages by opposed connection of magnetoresistance leads.

A disadvantage of the magnetoresistive element is its nonlinearity: resistance increases as the square of applied flux density over normal densities encountered in transducer work. However, this very square-law effect is harnessed by the multiplier's quarter-square principle to achieve a theoretical straight-line transfer function.

OPERATION

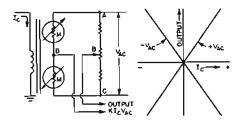


Figure 1. Simplified Multiplier Circuit
Coil input unbalances magnetoresistance bridge, develops output
which is product of bridge excitation and bridge unbalance.

A simplified open-loop multiplier is shown in Fig. 1. Inputs are applied to bridge terminals AC and to coil input E. Output, which is proportional to bridge unbalance, is taken from bridge terminals BD. The bridge is unbalanced when the magnetic field set up by coil drive current alters the values of the magnetoresistance bridge arms. The magnetic circuit

is arranged so that increased magnetic field increases the resistance of one bridge arm and simultaneously decreases the resistance of the other.

Although output is proportional to bridge unbalance, it is also proportional to the amount of voltage applied across terminals AC. In other words, multiplier output is proportional to the product of bridge unbalance (i.e. current I), and bridge excitation, (V_{AC}).

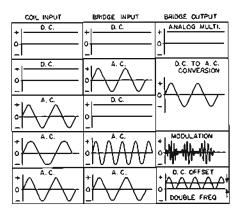


figure 2. Applications for Multipliers
Waveforms show possible outputs for various combinations of
AC and DC inputs.

Four fundamental operations: multiplying, dividing, squaring, and square-rooting can be based on the multiplier as shown in Fig. 3. Here, the multiplier is represented as an ideal "black box," with operational amplifiers forming part of the mathematical functions. In practice, additional operational amplifiers are required to linearize core and bridge characteristics, and also to match input signals to bridge

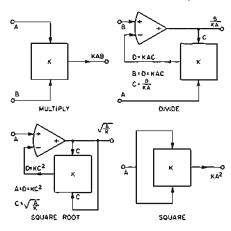


Figure 3. Basic Multiplier Operations When used with op amps, magnetoresistance bridge impliments four basic operations.

and coil impedances. Modulators, mixers, correlators, demodulators, phase sensitive rectifiers, and many other applications are based on one or another of these basic circuits.

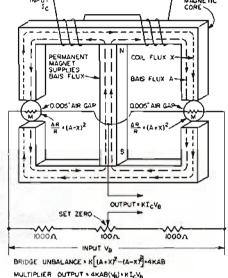
The primary function of the multiplier's magnetic circuit is to produce a linear unbalancing of the bridge in response to one set of input signals. Since the magnetoresistance elements are used in adjacent bridge arms, the magnetic circuit must produce push-pull unbalancing by increasing one magnetoresistor value while decreasing the other.

The magnetoresistor responds to an increase in flux by increasing resistance in a square-law relationship, regardless of the polarity of flux increase. Hence, special trickery is needed to provide polarity-sensitive unbalancing wherein one bridge arm increases resistance while the other decreases, and vice versa.

Figure 4.

Magnetoresistance
Bridge With
Permanent
Magnetic Bias
Coil Ilux and bias
flux added in one
air gap, subtract in
other to produce
push-pull bridge

unbalance.



A novel magnetic circuit using permanent-magnet biasing, Fig. 4, solves the problem and linearizes the transfer characteristic in the process. Magnetic flux, X, produced by coil current I, adds to the bias flux A in one air gap, and subtracts from the same value of bias flux in the other. In this way, one magnetoresistance bridge arm increases in value according to the square-law relationship $(A+X)^2$, while the other decreases according to $(A-X)^2$. The net bridge unbalance is proportional to the difference between these changes, hence follows the "quarter-square" relationship $(A+X)^2-(A-X)^2=4AX$. If bias flux is constant (supplied by a permanent magnet), multiplier output is a linear function of flux density, X, hence varies approximately linearly with coil current.

DOUBLE BRIDGE

The previous discussion concludes that the multiplier output varies linearly with coil current. This is only true so long as the multiplier uses magnetic cores with ideal characteristics. Magnetic material like this is pretty hard to come by; so in practice, hysteresis and nonlinearities limit the open loop multiplier's accuracy to about 2%.

Nevertheless, core nonlinearities can be "straightened out" with feedback. Or at least they can be removed from the transfer function by enclosing them in a high gain feedback loop. The actual feedback circuit, Fig. 5, is based on a double bridge multiplier using one bridge for feedback and an identical, closely matched bridge to develop output signals.

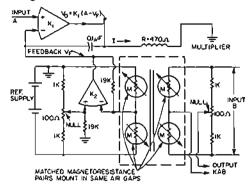


Figure 5. Double Bridge Multiplier for High Accuracy Feedback linearizes magnet and magnetoresistance circuit, unbalances both bridges in response to input A.

So long as the feedback loop remains closed, the left-hand bridge will unbalance in sympathy with input A regardless of core hysteresis or temperature effects in the bridge.

For example: if increased input produces a momentary difference between feedback V_i and input A, the amplifier's high gain will turn this difference $(A-V_i)$ into increased drive voltage for the magnetic coil. The new level of drive voltage, $K_1(A-V_i)$, then increases coil current, hence bridge unbalance, until equality between V_i and A is restored. Actual discrepancy between input and feedback is a few hundred micro-volts, depending upon amplifier gain and DC drift.

This method of feedback controlled bridge unbalancing is used in the double bridge multiplier by making an accurate match between the two magnetoresistance bridge arms sandwiched in each air gap. In this way, feedback controlled unbalance in the left-hand bridge is accurately duplicated by the right hand bridge. Consequently the two bridges track each other with at least 0.1% linearity and 0.01% temperature coefficient for wide ranges of temperature and flux density.

MULTIPLIER-DIVIDER

A versatile analog operational unit based on the double-bridge multiplier is shown with actual component values and operational amplifier types in Fig. 5. Outputs from this multiplier depend upon three independent variables A, B, and C according to the relationship V_o=kAC/B. This configuration

ANALOG COMPUTATION, Continued.

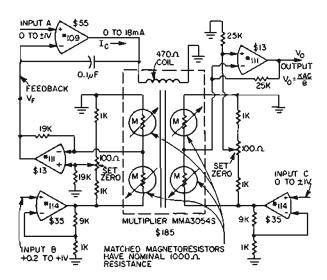


Figure 6. High Accuracy Multiplier — Divider Circuit Double bridge configuration simultaneously produces four-quadrant multiplication and two-quadrant division. Output is electrically isolated from inputs. Bridge accommodates up to 1 MHz inputs using fast op amps.

works simultaneously as a four-quadrant quarter-square multiplier and a two-quadrant divider, accommodating 0 to $\pm 1V$ inputs for terminals A and C, and $\pm 0.2V$ to $\pm 1V$ input for terminal B. The output of 500mV or so is amplified to convenient levels by the amplifier K5.

Customers have reported overall accuracies to 0.05% for narrow temperature ranges and using highest stability operational amplifiers. However, for the configuration shown in Fig. 6, with amplifiers totaling less than \$160, accuracies to 0.5% for 50°C temperature span are more reasonable. Cost of components for the complete package, with Model MMA3054S listed at \$185, is then less than \$350.

Simultaneous multiplying and dividing in one analog package is very convenient for handling flow equations, where expressions such as PRESSURE X DIFFERENTIAL PRESSURE ÷ TEMPERATURE must be manipulated, (Fig. 6). This calculation is performed with one unit, instead of using a separate analog multiplier and a divider which would otherwise be required.

The double bridge multiplier also makes an excellent modulator for controlling an AC carrier with a DC or low frequency input to the coil. (Input B is usually constant) Output from the right-hand bridge is electrically isolated from the coil input and,owing to the bridge's wide bandwidth, permits carrier-frequencies up to 1 MHz to be modulated with very low phase shift.

NEW PRODUCTS

Model 401 Modular Power Amplifier Develops 40 Watt Output From Single +28 Volt Power Supply



Designed to drive torque motors, deflection coils, M-G sets, servo valves and other high power transducers. Model 401 with fixed gain of 20 is intended to be preceded by a high gain operational amplifier in a wide variety of servo applications. Unique circuitry accepts single ended input signal and delivers a ± 20 V output swing—all from a single ± 28 V supply.

SPECIFICATIONS

±20V
2 amps
20V/V
5kHz
25K
- 45 to + 70°C
3.9"×3.9"×3.2"
\$275.00

Model 180A/B Chopperless Differential Amplifier with 0.75 \(^{\cup}\) C and



1.5 µV/°C maximum voltage drift.

Now you can get drift performance of chopper stabilized amplifiers for one half the price and in one third the size. New Model 180 also offers advantages of lower noise, higher input impedance and the versatility of differential inputs. You can build a low level voltage follower with 1000 Megohm input impedance or a differential amplifier with 100db CMRR and 1µV noise.

Unlike most differential amplifiers, special dual input transistor circuit of the 180 is virtually immune to offset errors due to thermal gradients. Warm up drift is typically less than 5μ V.

SPECIFICATIONS

SPEC	THEATIONS
Voltage Drift, max.	0.75μV/°C(B) and 1.5μV/°C(A)
Long Term Stability	y 5µV/day
Bias Current, max.	±2nA @ 25°C
Offset Current Dri	
Input Impedance	$2M\Omega$ & $1000M\Omega$
DC Gain	3×10 ⁵
Output Rating 🦼	±10V @ 2.5mA
Noise, p-p	(.01 to 1Hz) 1µV & 5pA
Common Mode	
R e jection	100,000
Price (1-9)	\$80. (A), \$110. (B)

Single Amplifier Current Sources

By BILL MILLER Applications Engineer Analog Devices, Inc.

The high gain and low offset drift of present day differential operational amplifiers permit their use in circuits which approach the performance of an ideal current source. High open loop gain results in a very small potential or a "virtual short" between the amplifier's input terminals. In this manner, a control voltage (E₁) may be applied across a resistor (R₁) which, due to amplifier nulling action, will result in the flow of a proportional load current (I_L) elsewhere in the circuit.

The circuits shown at right take advantage of the near short circuit (null) that exists between the amplifier input terminals. Except for the Howland circuit which utilizes positive feedback to approach infinite output impedance, the circuits are self-explanatory. (For more details on fundamental op amp theory request copies of Analog Device's "Operational Amplifiers, Parts I, II and IV.")

In each figure, the equations for load current vs. input and for amplifier output voltage and current are given to enable design within the amplifier's output limitations.

The circuits of Figures 3, 4, 5 and 6 are subject to common mode error which is dependent on input voltage level. For Ei greater than 5 volts common mode error may be substantial; but for a fixed reference voltage, the resulting error can be viewed as a gain error which can be calibrated.

Input offset voltage will add algebraically with E₁. The ratio of the maximum input offset voltage over the temperature range of interest to E₁ offers a direct method of calculating voltage offset errors.

By the same token, input offset current will, in general, add algebraically with the input current li, (E₁/R₁). The same ratio as above but in terms of offset current and input current yields the error due to this factor. It is important that the source impedance of E_i for the non-inverting configurations of figures 3 and 4 be low since the input offset current flows through the source impedance producing an additional input voltage offset error.

The illustrations presented are working circuits, but the chief intent has been to offer numerical examples as guide lines. The circuit values can be changed over a considerable range.

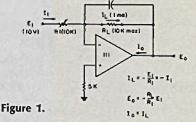
Page 5

FLOATING LOAD, INVERTING **ADVANTAGES**

- 1. Simplicity
- 2. No common mode error

DISADVANTAGES

- 1. Input source must supply current equal to load current
- 2. Floating load



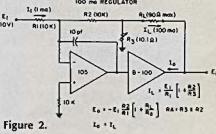
FLOATING LOAD, INVERTING, WITH CURRENT GAIN

ADVANTAGES

- 1. Circuit exhibits current gain; hence source current may be much less than load current
- 2. Remote adjustment capability via R3
- 3. No common mode error

DISADVANTAGES

- 1. Increased drift gain
- 2. Load is floating



20 mg REGULATOR

10 0

IL (20ma)

RL (450 a mox)

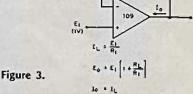
FLOATING LOAD, NON-INVERTING

ADVANTAGES

- 1. Simplicity and ease of adjustment
- 2. Input Source (E1) very lightly loaded

DISADVANTAGES

- 1. Common mode errors must be considered
- 2. Load is floating



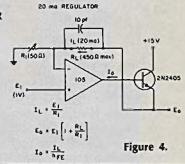
"INBOARD" EMITTER FOLLOWER

ADVANTAGES

- 1. Same as Figure 3
- 2. Large output current at low cost

DISADVANTAGES

- 1. Load impedance floating and output is uni-directional
- 2. Common mode errors must be considered



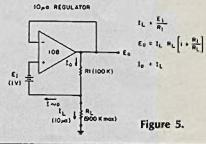
HIGH IMPEDANCE, GROUNDED LOAD, FLOATED REFERENCE

ADVANTAGES

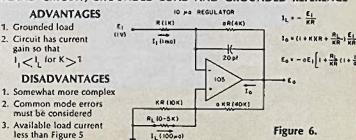
- 1. Simplicity and ability to supply high impedance loads
- 2. Load is grounded
- 3. Larger percentage of output voltage across load than Figure 6

DISADVANTAGES

- 1. Separate floating 2. Common mode errors
 - reference supply required must be considered



HOWLAND CIRCUIT, GROUNDED LOAD AND GROUNDED REFERENCE



DISADVANTAGES

- 1. Somewhat more complex 2. Common mode errors
- must be considered 3. Available load current less than Figure 5

1/</L for K>1

1. Grounded load

gain so that

Operational Integrators

By RAY STATA, Vice President and Co-founder Analog Devices, Inc.

Modern solid state operational amplifiers make remarkably good integrators. Almost any degree of accuracy can be achieved depending on the choice of the amplifier and the feedback capacitor. A great deal of literature exists^t which discusses integrator error in analog computers and this subject will not be covered here. But we shall review the non-ideal characteristics of operational amplifiers (and to some extent capacitors) which limit the performance of integrators in instrumentation circuits. This we hope will help the reader make a better choice of amplifiers for his particular application.

tKorn and Korn, Electronic Analog and Hybrid Computers - McGraw Hill,

An ideal operational amplifier for integrator applications would have infinite open loop gain and input impedance and zero offset voltage and current (that is, $e_0 = 0$, when $e_1 = 0$). For this case, Figure 1 shows the characteristics of an ideal integrator.

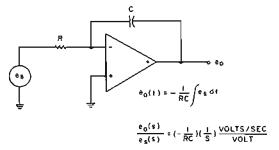


Figure 1. Ideal Operational Integrator

The gain (or characteristics time) of the circuit is given by 1/RC, which is to say that the output will change by (1/RC) volts/sec for each volt of input signal. The input impedance as viewed from the source voltage, e_s, is determined by the value for R.

OFFSET AND DRIFT ERRORS

By far the greatest source of error in integrators is due to offset and drift of the amplifier. An equivalent circuit is given in Figure 2 from which we can predict the errors due to offset. For the moment we shall assume that open loop gain, A, and open loop input impedance, R_{d} , are infinite.

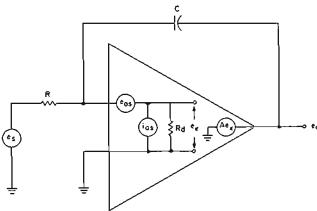


Figure 2. Equivalent Circuit for Integrator

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$e_{os} = E_{os} + \frac{\Delta e_{os}}{\Delta T} \Delta T + \frac{\Delta e_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta e_{os}}{\Delta t} \Delta t$$

$$i_{os} = I_{os} + \frac{\Delta i_{os}}{\Delta T} \Delta T + \frac{\Delta i_{os}}{\Delta V_{s}} \Delta V_{s} + \frac{\Delta I_{os}}{\Delta t} \Delta I_{s}$$

$$at$$

$$25^{\circ}C \text{ pa}/^{\circ}C \qquad pa/\% \qquad pa/day$$

As shown the offset voltage, e_{os} , and the offset current, i_{os} , can be calculated for any temperature, supply voltage and time period from the drift coefficients of the amplifier. It is usually possible to adjust the initial offset voltage and current, E_{os} and I_{os} , to zero by some biasing network.

The simplest way to analyze offset errors is to refer them to the source voltage as shown in Figure 3. In this case offset current is multiplied by R and becomes a voltage source. When viewed at the

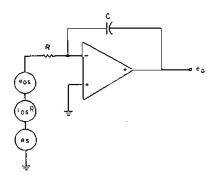


Figure 3. Offsets Referred to the Input

input, the offsets cannot be distinguished from the input signal and hence introduce a basic error in the integration of the signal. The percentage error would be, % error = $(e_{os} + i_{os}R)$ 100/ \bar{e}_s , where \bar{e}_s is

the time average of the input signal over the integration period. Notice that R should be as small as possible to minimize offset errors for a given amplifier. But remember that R also sets the input impedance for the integrator.

When referred to the input, the analysis of offset errors is not much different for an integrator than for an inverting DC amplifier. More detailed information is given on this subject in an Analog Devices' application note entitled "Part IV, Offset and Drift in Operational Amplifiers."

In some applications it is necessary to refer the offset error to the output in order to derive meaningful results. In this case the output error is a drift rate which is given by,

$$\frac{de_o}{dt} = \frac{e_o + Ri_o}{RC} = \frac{e_o}{RC} + \frac{i_o}{C}$$

Again, we see that output drift rate is minimized by using the smallest value for R and the largest value for C. This follows since the drift rate due to offset voltage is fixed by the gain of the circuit (1/RC) whereas the drift rate due to offset current is reduced by using a larger C.

The practical limits on the choice of R and C are as follows:

- 1. Source impedance sets a minimum value on input impedance which is equal to R.
- 2. The physical size, price and quality are all serious problems in using large value capacitors particularly when greater than 1 to $5\mu f$.

For differential input amplifiers, the error due to offset current is generally reduced by balancing the impedance as seen from each input to ground. For the circuit in Figure 3 this would amount to inserting a resistor from the plus input to ground equal to R. Due to the input symmetry of a differential amplifier, offset current at each input tends to be equal and tends to track with temperature and thus the drift error is reduced by balancing impedances.

ERRORS DUE TO FINITE GAIN, INPUT IMPEDANCE AND BANDWIDTH

The open loop gain response for most operational amplifiers can be represented by the graph in Figure

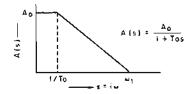


Figure 4. Typical Open Loop Gain Response

4. If we go back to Figure 2 and assume that the amplifier has to gain response of Figure 4 and an open loop input impedance, R_d, then the exact expression for integrator gain would be:

$$\frac{e_{\circ}(s)}{e_{1}(s)} = \underbrace{\begin{bmatrix} -1 \\ RCs \end{bmatrix}}_{ideal} \underbrace{\begin{bmatrix} 1 \\ 1 + \underbrace{\begin{pmatrix} 1+T_{\circ}s \\ A_{\circ} \end{pmatrix} \begin{pmatrix} 1+\frac{1}{R_{P}Cs} \end{pmatrix}}_{error due to finite gain and bandwidth}$$
(1)

where $R_p = R_d R / R_d + R$ (parallel sum)

Equation (1) can be simplified if we assume that $A_0 >> 1$ (a very safe bet):

$$\frac{e_o(s)}{e_i(s)} = \left[\frac{-1}{RCs}\right] \left[\frac{1}{1 + \frac{s}{\omega_i} + \frac{1}{A_o R_p Cs}}\right] \text{ for } A_o > 1$$
(2)

where $\omega_i \approx A_0/T_0$ is the amplifier unity gain bandwidth.

HIGH FREQUENCY ERRORS DUE TO FINITE BANDWIDTH

Finite amplifier bandwidth imposes some limitation on the ability of the integrator to respond to instantaneous input changes. The transient behavior at t=0 can be predicted by examining the behavior of equation (2) at high frequencies. In this case equation (2) becomes:

$$\frac{e_o(s)}{e_s(s)} = \frac{-1}{RCs} \left(\frac{1}{1 + s/\omega_s} \right) \text{ for } s > \frac{1}{A_o R_p C}$$
(3)

This is the equation for an ideal integrator except for a time lag which is inversely proportional to the unity gain bandwidth, ω_1 . To illustrate the error due to finite bandwidth, consider the response of (3) to a step function input as given by (4) and Figure 5.

$$e_{o}(t) \approx \frac{1}{RC} \left(t^{-1/\omega_{1}} \right) \quad \text{for } e_{s}(t) = -\mu_{-1}(t)$$

$$(4)$$

$$\frac{1}{\omega_{0}}$$

$$\frac{1}{\omega_{0}}$$

$$\frac{1}{\omega_{0}}$$

$$\frac{1}{\omega_{0}}$$

Figure 5. Step Response of Integrator at t = 0

Note that the time lag depends only on amplifier open loop bandwidth, wi, and is independent of the values for R and C.

LOW FREQUENCY ERRORS DUE TO FINITE GAIN

The behavior of an integrator over long time periods can be predicted by the low frequency response of the circuit. In this case, where s<<on, equation (2) becomes:

$$\frac{e_{\circ}(s)}{e_{\circ}(s)} = \left[\frac{-1}{RCs}\right] \left[\frac{1}{1 + \frac{1}{A_{\circ}R_{\rho}Cs}}\right] = -\frac{A_{\circ}R_{\rho}/R}{1 + A_{\circ}R_{\rho}Cs}$$
(5)

Insight is gained into the operation of integrators at low frequencies by realizing that (5) is equivalent to the response of an ideal integrator with an infinite gain and input impedance amplifier, but with a feedback resistor A_oR_p in parallel with the feedback capacitor as shown in Figure 6.

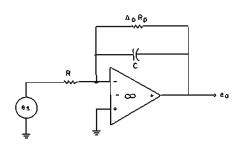


Figure 6. Integrator Low Frequency Equivalent Circuit

To illustrate more clearly the effect of low frequency errors, consider the response of (5) to a step function input as given by (6) and Figure 7.

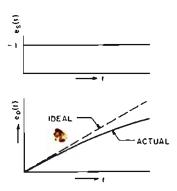
$$e_o(t) = \frac{R_o A_o}{R} (1 - e^{-U A_o R_D C})$$
, for $e_i(t) = -\mu_{-i}(t)$

Expanding (6) into a power series we have:

$$e_{o}(t) = \frac{t}{RC} - \frac{t^{2}}{2A_{o}(R_{p}C) (RC)} + - - -$$

The first term in this series is the response for an ideal integrator, while the second term is the principle error component which grows as the square of time.

In summary low frequency integrator errors are inversely proportional to finite open loop voltage



· Figure 7. Step Response Showing Low Frequency Error Due to Finite Gain

gain. This follows from the fact that with finite gain the error voltage is not zero, as usually assumed, which tends to reduce input current as the output grows.

INTEGRATOR HOLDS ERRORS

One important use of integrator circuits is to precisely remember or hold a voltage potential. Finite amplifier gain causes a fixed integrator output voltage to droop.

Intuitively it is apparent from Figure 6 that the effective leakage resistance, AoRp, due to finite voltage gain and input impedance tends to discharge any fixed voltage stored across the feedback capacitor.

To develop a quantitative expression for this error, assume that the circuit in Figure 6 has the initial condition $e(o) = E_o$ and that $e_s = o$. In this case, the output voltage is simply:

$$e_0(t) = E_0 e^{-t/AoRpC}$$

By expansion this becomes:

$$e_o(t) = E_o - E_o \left[\frac{t}{A_o R_p C} - \frac{t^2}{2(A_o R_p C)^2} + - - - \right]$$
(7)

The first item of (7) is the output of an ideal integrator, while the terms in the brackets represent the errors due to finite gain. Figure 8 shows integrator hold error.

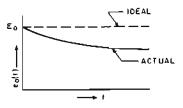


Figure 8. Integrator Hold Error

It is interesting to note that minimum error is obtained in hold operation when the input resistor is open circuited rather than short circuited. In this case the equivalent circuit is shown in Figure 9.

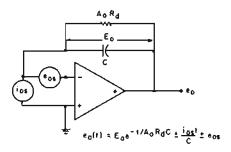


Figure 9. Hold Circuit with Input Open

Note that the equivalent feedback leakage resistor is determined only by the open loop input impedance and gain (A_oR_d). Further, the output drift rate is determined only by the offset current. Voltage offset appears at the output as a fixed offset.

FEEDBACK CAPACITOR

The performance of operational amplifiers have now reached the point where the quality of the feedback capacitor can limit the accuracy in the most precise

applications. Therefore a brief discussion of capacitor limitations will be helpful in precise integrator design.

The chart in Figure 10 shows the salient characteristics for various types of high quality capacitors. This data was compiled with the assistance of Southern Electronics Corporation, Burbank, California, a capacitor manufacture who specializes in high quality capacitors for integrator applications. An application note from this company entitled "Capacitor Talk" gives more information on the interpretation of capacitor specifications.

In analog computers where scale factor accuracy is important it is common practice to enclose the feedback capacitor in a temperature controlled oven. In this case long term stability of capacitance value for polystyrene and mylar capacitors is about 0.1% per year.

tnsulation Resistance — One important limitation for integrator capacitors is insulation or leakage resistance. The specification used to define this limitation usually is expressed in megohms - microfarads, which is equivalent to the time in seconds for a fixed voltage stored on the capacitor to discharge to 63% of its initial value. As a general rule the maximum insulation resistance is about two times the value for a one microfarad capacitor, which establishes the limit for insulation resistance of small capacitor values.

			_	-			
Dielectric	Mylar	Metalized Mylar	Poly- carbonate	Metalized Poly- carbonate	Polystyrene	Teilon	Metalized Tellon
Temperature Range Hi Temp (°C) Lo Temp (°C)	+125 -65	+125 -65	+125 -65	+125 -65	+85 -65	+ 200 - 65	+200 -65
Temperature Coefficient -65°C to 25°C (%) 25°C to Hi Temp (%)	-6 十12	-6 +12	−1.5 ±0.5	−1.5 ±0.5	+0.9 -0.6	+1.9 -3.7	+ 0.5 -1.0
Dielectric Absorption % @ 25°C	0.1	0.1	.05	.05	.02	.01	.02
Dissipation Factor @25°C (%) @ Hi Temp (%)	0.3 1.2	0.5 1.7	0.1 0.07	0.2 0.6	0.02 0.04	0.01 0.02	0.1 0.2
Insulation Resistance @ 25°C ($M\Omega$ - μ f) @ Hi Temp ($M\Omega$ - μ f)	2x10 ⁵ 3x10 ²	5x10⁴ 1x10²	4x10 ⁵ 1.5x10 ⁴	2x10 ⁵ 15x10 ²	1x10 ⁶ 7x10 ⁴	1x10 ⁶ 1x10 ⁵	5x10 ⁵ 2.5x10 ⁴
Approximate Size for 50Vdc cubic inch/µf (uncased)	.12	0.06	.19	0.09	.44	1.1	0.39

Figure 10. Comparison of Capacitor Specifications

The effect of insulation resistance can be represented in Figures 6 and 9 as another resistance in parallel with A_oR_p or A_oR_d and the issuing equations are modified accordingly. The insulation resistance of the very best capacitors is about 10^{12} ohms. By comparison a chopper stabilized operational amplifier will have open loop input impedance, R_d , of 10^6 ohms and open loop gain, A_o , of 10^8 giving an equivalent resistance of 10^{14} . Even an inexpensive differential amplifier will have equivalent leakage resistance of 10^{10} to 10^{11} ohms. Thus we see that the capacitor and not the amplifier usually sets the limit on performance in this regard.

Dielectric Absorption — One of the single most important dynamic errors of integration is due to dielectric absorption. This error results from the fact that when a capacitor is charged or discharged not all of the dielectric polarization takes place immediately. Consequently there can be an appreciable residual voltage with a relatively long time constant. The specification given for this parameter is the residual voltage expressed as a percentage of the applied voltage measured approximately one second after the capacitor is discharged. Polystyrene and tef-Ion are mostly used for precision integrators since these materials have small but measurable errors due to dielectric absorption. For additional information on analyzing this source of error you should refer to "An Analysis of Certain Errors in Electronic Differential Analyzers II—Capacitor Dielectric Absorption," P. C. Dow, IRE Trans. on Electronic Computers, Vol. EC-7, pp.17-22, March, 1958.

Dissipation Factor, which is related to dielectric absorption, can be termed the sum total of all the losses in the capacitor and is expressed as the percentage ratio of the effective series resistance to the reactive capacitance, or as the tangent of the loss angle. Dissipation factor is important in AC integrators or in analog computers where repetitive integration is performed.

LEAKAGE RESISTANCE

In the highest performance integrators, leakage resistance to the summing junction or across the feedback capacitor can play a large role in the attainable performance. It is extremely important to shield the summing junction and its leads from leakage paths to potentials other than ground. For example, offset current, which is one of the principle limitations to good integrator performance, in a good chopper amplifier is about 10⁻¹¹ amps. The insulation resistance required to keep the leakage current from the 15VDC supply voltage less than 10⁻¹¹ amp would have to be greater than one mil-

lion megohms. The insulation resistance of most wire and connectors fall short of this requirement. However, by properly shielding the summing junction and its leads, leakage currents from active sources are shunted to ground, effectively creating extremely high insulation resistance from these potentials to the summing junction.

By the same token leakage resistance of the clamping circuits across the feedback capacitor used to reset the integrator should not be overlooked when calculating the effective leakage of a feedback capacitor. For example, the leakage resistance of a computer grade capacitor is typically 10¹² ohms, which may be negligible compared to the leakage resistance of a relay or a solid state switch.

AC INTEGRATORS

In some applications it may be desirable to integrate AC signals over a reasonably long time and it may not be possible to reset the output to zero periodically. In this case the DC offset problem can be alleviated in part by bounding the DC closed loop gain as shown in Figure 17.

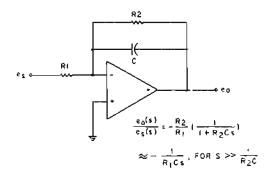


Figure 11. AC Integrator

The closed loop response for this circuit is shown in Figure 12.

For frequencies greater than $1/R_2C$ the response approaches that of an ideal integrator with gain of $1/R_1C$. For example, for signal frequencies, ω_s , a decade away from the corner frequency, $1/R_2C$, the gain error is only .5%.

The advantage of bounding the DC gain with R_2 is that the amplifier output will not drift into saturation. Instead the output will assume a DC value of $e_o = -R_2/R$, ($e_{ot} + R_{ilos}$). This output will limit the dynamic range for AC output signals; but, by choosing an amplifier with sufficiently low offsets, satisfactory operation can be obtained for many AC integrator applications.

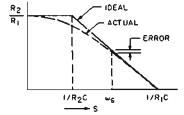
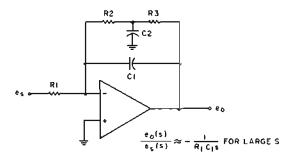


Figure 12. Gain Response for AC Integrator

For integration of very low frequency AC signals, the DC gain requirements of the previous circuit are so large as to cause saturation of the output. In this case the following circuit allows the DC gain to be reduced.

The lowest frequency which can be accurately integrated is limited by the size for C_2 . The general expression for the corner frequencies ω_1 and ω_2 are rather complex and as a practical matter can only be determined by trial and error calculations. The lowest signal frequency, ω_1 , should be at least ten times greater than ω_2 .



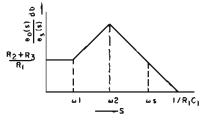


Figure 13. Low Frequency AC Integrator

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OPEN LOOP GAIN

Open loop gain, A, is defined as the ratio of output voltage to error voltage between inputs as shown in Figure 1. Usually gain is specified only at DC, but in

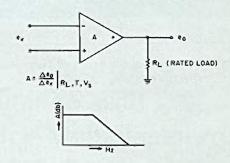


Figure 1. Definition of Open Loop Gain

many applications such as AC amplifiers the frequency dependence of gain is also important. Open loop gain changes with load impedance (R_L), ambient temperature and supply voltage. As a rule, open loop gain will not change more than a factor of 10 between rated load and no load conditions. Most operational amplifiers have a positive gain temperature coefficient of about 0.5 to 1%/°C and gain changes with supply voltage at about 2%/%. Analog Devices specifies all open loop gains at rated load, 25°C and rated supply voltages.

TEST CIRCUIT

A practical circuit for measuring open loop gain over a range of frequencies is shown in Figure 2. The voltage divider on the negative input boosts the sen-

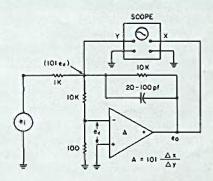


Figure 2. Open Loop Gain Test Circuit

sitivity of the error voltage by 100 times which makes it possible to measure gains of several million. At low frequencies open loop gain is constant so that DC gain can be measured by a low frequency signal (about 5Hz). The voltage divider may not be necessary for low gain amplifiers (below 20,000) and it is not recommended for measuring gain at high frequencies where open loop gain is less. At very best, noise pickup is a problem for measuring high

GLOSSARY OF DEFINITIONS

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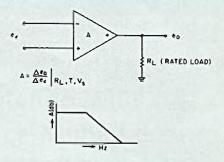


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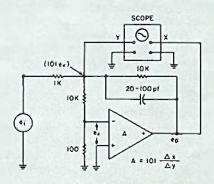


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gains and care must be taken to adequately shield the test circuit.

At high frequencies the amplitude of the output voltage must be reduced to avoid exceeding the slewing rate of the amplifier. For this reason the output voltage should be adjusted, so that e_a (peak) < Slew Rate/ ω_i .

SIGNIFICANCE OF GAIN

Operational amplifiers are rarely used open loop. Instead negative feedback is used around the amplifier to improve the accuracy of the circuit. This introduces a second term, closed loop gain (G), which is defined as the gain of the circuit with feedback. The simple inverting amplifier in Figure 3 illustrates this point.

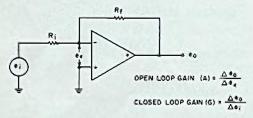


Figure 3. Closed Loop Circuit

Linearity, gain stability, output impedance and gain accuracy are all improved by the amount of feedback. Figure 4 graphically illustrates the relation between open loop gain and closed loop gain.

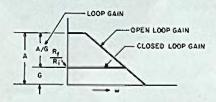


Figure 4. Determination of Loop Gain

The excess of open loop gain over closed loop gain is called loop gain. (Subtraction of dB is equivalent to arithmetic division.) The improvement of open loop performance due to feedback is directly proportional to loop gain. As a general rule for moderate accuracy, open loop gain should be 100 times greater than the closed loop gain at the frequency, or frequencies, of interest (that is loop gain = 100). For higher accuracy, loop gain should be 1000 or more. To illustrate, we recall that open loop gain stability for most operational amplifiers is about 1%/°C. With loop gain of 100, closed loop gain stability would be 100 times better or 0.01%/°C. Likewise, closed loop output impedance would be 100 times less than open loop output impedance with a loop gain of 100.

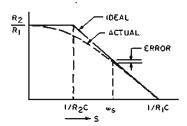
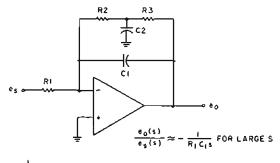


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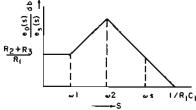


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